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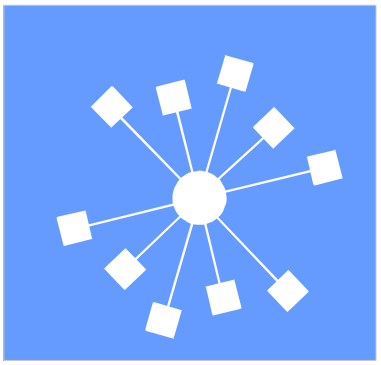

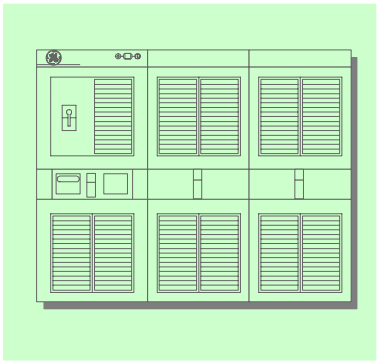

SPEEDTRONIC Mark V LM Turbine Control

Function Manual, WINSYS Edition

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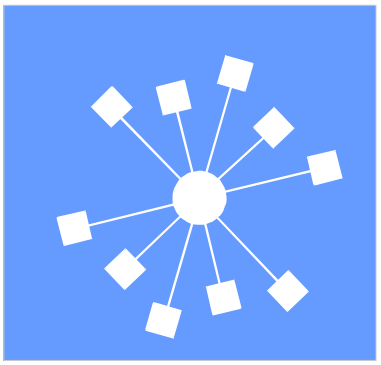

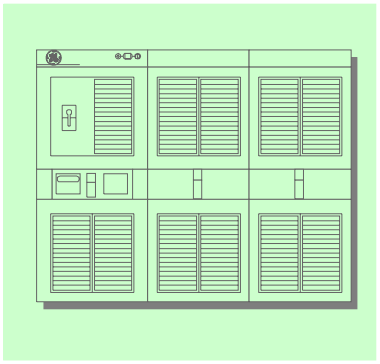

SPEEDTRONIC Mark V LM Turbine Control

Function Manual, WINSYS Edition

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Safety Symbol Legend

Warning

Indicates a procedure, condition, or statement that, if not strictly observed, could result in personal injury or death.

Caution

Indicates a procedure, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.

Attention

Indicates a procedure, condition, or statement that should be strictly followed in order to optimize these applications.

Note Indicates an essential or important procedure, condition, or statement.

Warning

To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify any programmable machine.

Caution

The example and setup screens in this manual do not reflect the actual application configurations. Be sure to follow the correct setup procedures for your application.

Symbol	Publication	Description
	IEC 417, No. 5031	Direct current
	IEC 417, No. 5032	Alternating current
	IEC 417, No. 5033	Both direct and alternating current
	IEC 617-2, No. 02-02-06	Three-phase alternating current
	IEC 417, No. 5017	Earth (ground) TERMINAL
	IEC 417, No. 5019	PROTECTIVE CONDUCTOR TERMINAL
	IEC 417, No. 5020	Frame or chassis TERMINAL
	IEC 417, No. 5021	Equipotentiality
	IEC 417, No. 5007	On (Supply)
	IEC 417, No. 5008	Off (Supply)
	IEC 417, No. 5172	Equipment protected throughout by DOUBLE INSULATION or REINFORCED INSULATION (equivalent to Class II of IEC 536)
	ISO 3864, No. B.3.6	Caution, risk of electric shock
	ISO 3864, No. B.3.1	Caution

Contents

Contents — Continued

Contents — Continued

Chapter 5 Control Engine

Chapter 6 General I/O Capacities and Specifications

Contents — Continued

Contents — Continued

Contents — Continued

Contents — Continued

Notes

Chapter 1 Overview

Definition and Scope

This document provides information about the Mark V LM turbine controller. The information includes receiving, handling, and installation of the controller, a summary of its basic operations, a description of the printed wiring boards, applications and specifications of the I/O, and information on renewal parts and troubleshooting.

This chapter provides the following information:

Equipment Overview

This section provides a basic overview of the equipment involved with the Mark V LM controller. These include communications, the operator interface, and the controller itself.

Mark V LM Controller

GE Turbine Control Systems have been produced for several decades and have enjoyed widespread acceptance in both new unit and retrofit applications. The Mark V LM represents the latest in a line of microprocessor-based control systems designed specifically for controlling turbines. The Mark V LM is used on aeroderivative gas turbines.

Unit control and protection is accomplished by using the Mark V LM in combination with sensors and devices mounted on the unit and its auxiliaries.

Printed wiring boards and terminal boards in a Mark V LM controller are contained in or are mounted on **cores** (see Figure 1-1). Cores are sheet-metal housings that can have stationary and movable printed circuit board holders called card carriers. The cores have a maximum of five printed circuit boards mounted on the card carriers. In addition, up to four I/O terminal boards can be mounted on a single core. The combination of boards contained in each core is dependent on the application.

<R> = Control and communication processor

<R1> – <R3> and <R5> = Control processor I/O cores

<P1> = Protective core

<PD> = Power distribution core

<Q11> and <Q51> = digital I/O cores

Figure 1-1. Mark V LM Controller Layout

Operator Interface

The primary operator interface consists of a color monitor, keyboard, cursor positioning device (CPD), printer(s), and central processing unit (CPU). The interface is connected to the Mark V LM controller via an ARCNET cable. The devices can be located in the installation's central control room or a turbine's control compartment.

One operator interface can be used to control multiple turbines; also more than one operator interface may be used to control a single turbine. The operator can thereby select the units he wishes to monitor or issue commands to. All operator interfaces are capable of issuing commands to a unit at any time while communicating with Mark V LM controllers. For the purposes of this manual, it is assumed that the operator interface is controlling a single turbine and driven device.

Using the operator interface, commands may be issued to the turbine and driven device (for example, START, STOP, COOLDOWN ON, AUTO, RAISE SPEED/LOAD, and so on). Displays may be accessed to view the status of the turbine and driven device (for example, ALARMS, WHEELSPACE TEMPERATURES, VIBRATION FEEDBACK, and so on). The associated printer(s) enable the operator to manually select and copy any display, to automatically log selected parameters, and to log alarms.

The operator interface performs no control or protection functions of the turbine and driven device; it is a means of issuing commands to the Mark V LM controller and monitoring unit operation. Removing power from or re-booting the HMI, or disconnecting and reconnecting the Stagelink ARCNET cable between the Mark V LM controller and HMI (while the turbine and driven device are operating) will have no effect on the Mark V LM controller or unit operation.

Communications

Information is communicated, shared, and acted upon in the Mark V LM Control System via three separate networks. The one external network, the Stagelink, is the primary means of communication between the operator interface and the Control Engine located in the <R> core of the controller. This link uses ARCNET configuration.

The COREBUS is a separate ARCNET communication network internal to the Mark V LM controller. The function of the COREBUS is to provide a communication link between the I/O control processors (<R1>, <R2>, <R3>, <R5>) and the Control Engine (<R>).

The third internal network is known as the I/O network (IONET). The IONET is a serial communications network that is connected in a daisy chain configuration. The purpose of the IONET is to transfer signals from the digital I/O cores (<Q11>, <Q51>) and the protective core (<P1>) to the I/O control processors. There are two separate IONETs, one connecting <Q51> and <R5> and one connecting <Q11>, <P1>, and <R1> (see Figure 1-1.).

Stagelink

The Stagelink consists of a coax cable that is terminated at both ends with BNC connectors. It runs from the ARCNET interface board in the operator interface, to <R> in the controller. The ARCNET interface board is a high impedance source that enables the operator interface to communicate on the Stagelink. Connection to the Stagelink hardware requires the use of a "T" type BNC connector. This device also permits the Stagelink to continue to further processors on the network. It is necessary to terminate the cable of the last operator interface on the link with a 93-ohm termination resistor on the open connection of the "T" type BNC connector. See Chapter 10 of this manual for connectivity rules.

The Stagelink connection on the <R> core is an active three-port repeater (see Figure 1-2). This device consists of three ports (two external and one internal). The internal port communicates from the processor to the external ports. Either external port receives a signal, amplifies it, and then passes it to the <R> core and the other external port. Similarly, a signal originating in the core is amplified and sent out both external ports. Loss of communication with the <R> core results in an interruption of data flow on the Stagelink. Two Stagelink connections are located on the AAHA1 board in the <R> core.

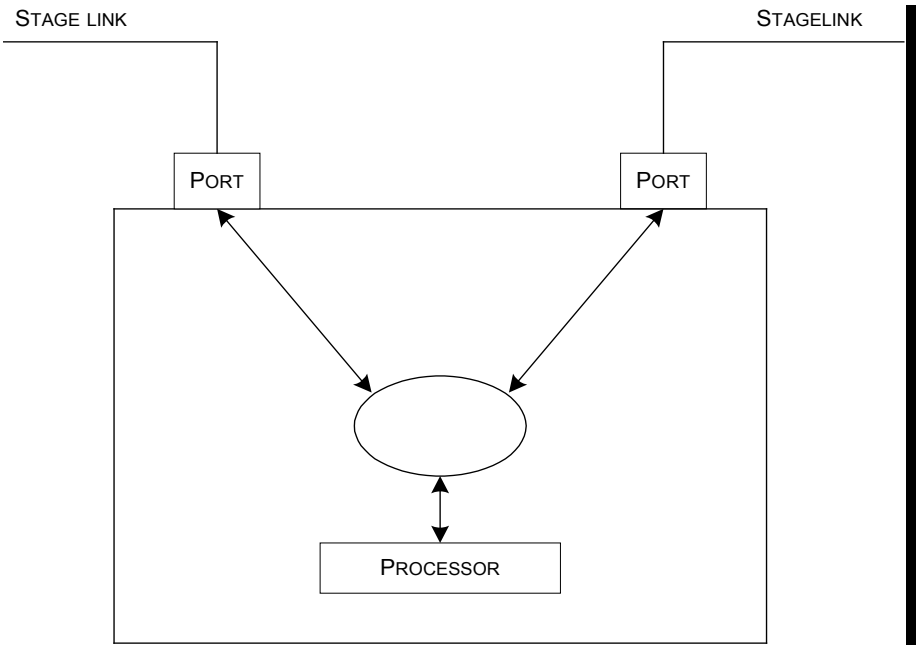


Figure 1-2. Three Port Active Repeater

COREBUS

The COREBUS is an ARCNET communication network linked between the control engine <R> and the I/O engines <R1>, <R2>, <R3>, and <R5> (See Figure 1-1.). The COREBUS has two main purposes: BMS and IO communications between Control Engine and I/O Engines. The IO Engines are daisy-chained to the Control Engine <R5>-<R1>-<R2>-<R> and another connections <R3>-<R>. The COREBUS connections are on:

- QTBA in <R1>, <R2> and <R3>
- CTBA in <R5>
- AHAA2 in <R>

The BMS, or Basic Messaging System, is the backbone of the system that allows basic message packets to be transmitted from the control engine to the various I/O engines. Supported by the BMS is the UDM, or User Defined Memory system. The UDM is what allows the controller to send a message to one of the I/O cores, asking it for a memory allocation.

The COREBUS also handles input/output traffic between the control engine and the I/O cores. Every 10 milliseconds (known as a frame), the I/O cores transmit a packet of the data to the control engine, which stores them all in the database. Included among <R1>'s data is information transmitted from the TCEA boards and TCDA board over the IONET. This information can come in the form of high speed data (once per frame) or low speed data (spread across 4-8 frames). Once every frame, towards the end of the frame, the control engine transmits all the output data in one packet across the COREBUS. Each I/O core receives this packet, then takes the information that it needs from it.

IONET

The IO Network (IONET) is a serial communication network between an IO Engine and the TCDA and TCEA boards that may be present. Data exchange occurs between the STCA board and the TCDA boards in the digital cores (<Q11>, <Q21> or <Q51>) and the TCEA boards located in <P1>. However, the physical IONET connections are made to the TCQC board in <R1> and R2> or to CTBA in <R5>. Information transmitted over the network is address-specific. As a result, data is sent to either the TCDA or TCEA boards according to their hardware jumper address settings. See Appendix A for hardware jumper setting information.

The IONET boards are linked in a daisy chain configuration as shown for each of the following cores:

- <R1> IONET is <R1>TCQC-<P1>TCE1-<P1>TCE2-<P1>TCE3-<Q11>TCDA. The TCEA board designations are also known as TCEA-X, TCEA-Y and TCEA-Z, respectively.
- <R2> IONET is <R2>TCQC-<Q21>TCDA. <Q21> is an optional digital core available for external connection to the Mark V LM controller.
- <R5> IONET is <R5>CTBA-<Q51>TCDA.

3PL

A direct analog IO communication path between the STCA and Analog IO boards is provided in each IO core on the 3PL ribbon cable. 3PL is a 34-conductor ribbon cable that connects the STCA in location 1 with the IO boards in location 2 and location 3, if a board is present in location 3.

The 3PL boards are linked in a daisy chain configuration as shown for each of the following cores:

- <R1> 3PL is STCA-TCQA-TCQE.
- <R2> 3PL is STCA-TCQA.
- <R3> 3PL is STCA-TCQA.
- <R5> 3PL is STCA-TCCA-TCCB.

How to Get Help

If help is needed beyond the instructions provided in the system documentation, contact GE as follows:

"+" indicates the international access code required when calling from outside the USA.

GE Industrial Systems
Post Sales Service
1501 Roanoke Blvd.
Salem, VA 24153-6492 USA

Phone: + 1 888 GE4 SERV (888 434 7378, United States)
+ 1 540 378 3280 (International)

Fax: + 1 540 387 8606 (All)

Note Please have the GE requisition or shop order number and the equipment serial or model number available to exactly identify the equipment when calling.

Chapter 2 Receiving, Handling, and Storage

Introduction

This chapter is a general guide to the receiving, handling, and storage of a Mark V LM controller. It is organized as follows:

Receiving and Handling

Caution

Immediately upon receiving the system, place it under adequate cover to protect it from adverse conditions. Packing cases are not suitable for outdoor or unprotected storage.

Shock caused by rough handling can damage electrical equipment. To prevent such damage when moving the equipment, observe normal precautions along with all handling instructions printed on the case.

GE inspects and packs all equipment before shipping it from the factory. A packing list, which itemizes the contents of each package, is attached to the side of each case of the equipment.

Upon receipt, carefully examine the contents of each shipment and check them with the packing list. Immediately report any shortage, damage, or visual indication of rough handling to the carrier. Then notify both the Transport Company and GE Industrial Systems. Be sure to include the serial number, part (model) number, GE requisition number, and case number when identifying the missing or damaged part.

If assistance is needed, contact GE as instructed in Chapter 1, *How to Get Help*.

Storage

Caution

Packing cases are not suitable for outdoor or unprotected storage.

If the equipment is not installed immediately upon receipt, it must be stored properly to prevent corrosion and deterioration. Use these guidelines:

1. Place the equipment under adequate cover with the following requirements:
   a. Keep the equipment clean and dry, protected from precipitation and flooding.
   b. Use only breathable (canvas type) covering material – do not use plastic.
2. Unpack the equipment as described on the following page, and label it.
3. Maintain the following environment in the storage enclosure:
   a. Ambient storage temperature limits from -20 °C to 55 °C (-4 °F to 131 °F).
   b. Surrounding air free of dust and corrosive elements, such as salt spray or chemical and electrically conductive contaminants.
   c. Ambient relative humidity from 5 to 95% with provisions to prevent condensation.
   d. No rodents.
   e. Avoid temperature variations that cause moisture condensation on the equipment.

Caution

Moisture on certain internal parts can cause electrical failure.

Preventing Condensation

Condensation occurs with temperature drops of 15 °C (27 °F) at 50% humidity over a 4-hour period, and with smaller temperature variations at higher humidity.

If the storage room temperature varies in such a way, install a reliable heating system that keeps the equipment temperature slightly above that of the ambient air. This can include space heaters or panel space heaters (when supplied) inside each enclosure. A 100-watt lamp can sometimes serve as a substitute source of heat.

Caution

To prevent fire hazard, remove all cartons and other such flammable materials packed inside units before energizing any heaters.

Unpacking

Recommended: *Do not completely unpack the equipment until it is placed as near as possible to its permanent location.*

- If the equipment has been exposed to low temperatures for an extended period, do not unpack it until it has reached room temperature (location where drive/exciter will be mounted).
- Use standard unpacking tools, including a nail puller.
- When unpacking, check the contents of each case against the packing list. Report any shortage to GE.
- Carefully remove the packaging and move the equipment from its container, still observing all lifting and handling guidelines.
- While unpacking, inspect for damage that may not have been detected at the time of receipt.
- Wipe off any particles of packing materials or foreign substances that may be lodged in or between the parts.
- Small parts (such as bolts and screws) are packed in special containers to keep them together, but may become separated. For this reason, carefully inspect the packing material for loose parts before discarding it.

Document and report equipment damage to GE.

➢ **Do the following if equipment damage is discovered while unpacking**

1. Stop unpacking immediately and report this finding to the carrier (transportation company).
2. Photograph the damage (photographs may be needed later in processing the claim).
3. File a claim with the carrier.
4. Contact the local service office of GE Industrial Systems for assistance.
5. When identifying missing or damaged parts, be sure to include the following information (refer to the nameplate):
   - Serial number
   - Part (model) number
   - Drive/exciter code
   - GE requisition number
   - Case number

Time Limitations

The above specifications apply to shipping and storage of up to one year. Longer times may require additional treatment. For warranty information, refer to Chapter 9 of this document.

Notes

Chapter 3 Installation and Initial Powerup

Introduction

This chapter contains environmental, mounting, and electrical guidelines for installing the Mark V LM controller. It also includes basic circuit checks needed after installation and before start up. Before installation, consult and study all furnished drawings. These should include arrangement drawings, connection diagrams, and a summary of the equipment.

This chapter is organized as follows:

Operating Environment

The Mark V LM controller is suited to most industrial environments. To ensure proper performance and normal operational life, the environment should be maintained as follows:

Ambient temperature (acceptable): 0 °C (32 °F) to 45 °C (113 °F)

Ambient temperature (preferred): 20 °C (68 °F) and 30 °C (87 °F)

Note Higher ambient temperature decreases the life expectancy of any electronic component. Keeping ambient air in the preferred (cooler) range should extend component life.

Relative humidity: 5 to 95%, non-condensing.

Environments that include excessive amounts of any of the following elements reduce controller performance and life:

- Dust, dirt, or foreign matter.
- Vibration or shock.
- Moisture or vapors.
- Rapid temperature changes.
- Caustic fumes.
- Power line fluctuations.
- Electromagnetic interference or *noise* introduced by:
  - Radio frequency signals, typically from portable transmitters used near the equipment or its wiring.
  - Stray high voltage or high frequency signals, typically produced by arc wielders, unsuppressed relays, contactors, or brake coils operating near control circuits.

The preferred location for the Mark V LM controller would be in an environmentally controlled room or in the control room itself. The controller should to be mounted where the floor surface allows for attachment in one plane (a flat, level, and continuous surface). The mounting hardware is provided by the customer. Lifting lugs are provided and if used, the lifting cables must not exceed 45° from the vertical plane. Finally, the controller is equipped with a door handle which can be padlocked for security.

Interconnecting cables can be brought into the controller from the top or the bottom via removable access plates. Convection cooling of the controller requires that conduits be sealed to the access plates. Also, air passing through the conduit must be within the acceptable temperature range, as listed above. This applies to both top and bottom access plates.

Cabling, Wiring, and Power Sources

This section covers the basic electrical information involved with the Mark V LM controller. All installations should meet the requirements of both the National Electrical Code and any applicable local codes. Use these codes to determine such factors as wire size, insulation type, conduit sizing, and enclosures.

Warning

Danger of electric shock or burn. Before handling and connecting any power cables to the equipment, make sure that all input power is turned off. Then check voltage levels on the wiring to ensure that it is not carrying hazardous voltages.

Spacing

The following requirements ensure correct distance between cabling and wiring:

- **Signal** wiring and **power** wiring may cross at right angles with a minimum 1-inch separation.
- Avoid parallel runs between signal level wires and power or control wires. If signal wires must be run parallel with control or power wires:
  - For distances up to 4 feet, maintain a minimum separation of 3 inches.
  - For distances over 4 feet, add 1/4 inch of additional spacing for every foot of additional distance.
- Within pullboxes and junction boxes, use grounded barriers to maintain the level separations.

Power Sources

The Mark V LM controller can accept power from multiple power sources. Each power input source (example: the dc and two ac sources) should feed through its own external 30 A 2-pole thermal magnetic circuit breaker before entering the Mark V LM controller. The breaker ratings are 250 V and 30 A with a minimum withstand of 10,000 A. The breaker should be supplied in accordance with EN61010-1 section 6.12.3.1 and marked as CE.

Power sources can be any combination of a 125 V dc source and/or up to two 120/240 V ac sources. Each core within the controller has its own power supply board, each of which operates from a common 125 V dc controller distribution bus. For further detail on the controllers power distribution system, refer to Appendix C.

Table 3-1. Power Source Requirements

Voltage		Frequency		Current Draw (Typical)
Nominal	**Tolerance Range**	**Nominal**	**Tolerance Range**	
125 V dc	100 to 144 V dc (see Note 5)	N/A	N/A	7.0 A dc (see Note 1)
120 V ac	108 to 132 V ac (see Note 6)	50/60 Hz	47 to 53 Hz	7.0 A rms (see Notes 2 and 4)
240 V ac	200 to 264 V ac	50/60 Hz	57 to 63 Hz	3.5 A rms (see Notes 3 and 4)

* Current draw is measured at nominal voltage

Notes on Table 3-1:

1. Add .5 A dc continuous for each 125 V dc solenoid powered.
2. Add 6.0 A RMS for a continuously powered ignition transformer (2 maximum).
3. Add 3.5 A RMS for a continuously powered ignition transformer (2 maximum).
4. Add 2.0 A RMS continuous for each 120 V ac solenoid powered (inrush 10.0 A).
5. Ripple not to exceed 10 volts peak-to-peak.
6. Total Harmonic Distortion not to exceed 5.0%.

Equipment Grounding

Within the Mark V LM controller, each controller is equipped with a single control common wire which connects to the controller control common ground bar, abbreviated as CCOM. The control common ground (CCOM) bar along with the shield bars are connected to the controller ground bar located at the bottom of the controller through the controller's steel structure. The controller ground bar must be attached to earth or grid ground with a minimum #4 AWG copper cable. This connection is a controller ground for safety and helps eliminate electrical noise.

Warning

Although the controller itself is metal and grounded, it is an unacceptable practice to use it as a grounding point in place of an earth or grid ground.

Power-Off Checks

All Mark V LM controllers are factory-tested and operable when shipped to the installation site. However, final checks should be made after installation and before starting the equipment.

This equipment contains a potential hazard of electrical shock or burn. Power is provided by the Mark V LM controller to various input and output devices. External sources of power may be present in the Mark V LM controller that are *not* switched by the control power circuit breaker(s). Before handling or connecting any conductors to the equipment, use proper safety precautions to insure all power is turned off.

Controller Inspection

Inspect the controller components for any damage which might have occurred during shipping. Check for loose cables or wires, connections or loose components such as relays or retainer clips. Report any damage that may have occurred during shipping to GE Industrial Systems - Product Service.

The ground lug in the bottom of the Mark V LM controller must be connected to a suitable ground point, preferably plant ground grid.

Board Inspections

The following steps should be performed in order to inspect the printed circuit boards in each core:

- Inspect the boards in each core checking for loose or damaged components. Verify all plug in relays are firmly connected into their sockets.
- Check to see that each board is held firmly.
- Check ribbon cables and wire harnesses. Verify all ribbon cables are securely connected.
  - If it is necessary to unplug the connector, use the pull tabs on each ribbon cable to remove them. DO NOT pull directly on the ribbon cables or wires.
  - Note the orientation of the ribbon cable or wire harness "trace". (Trace is the colored wire on the edge of the ribbon cable, or the "odd"-colored wire on the edge of the wire harness.)
  - Check each wire harness power cable for proper location, checking the cable ID tag against the connector ID printed on the board and the drawings.

Ribbon cables and wire harnesses are always oriented with the trace connected to pin 1 of the receptacle. Refer to the core drawings for more information. Incorrect connection could damage board(s).

Many ribbon cable connectors are not keyed. Use caution when connecting them. The connectors which do not fit into a receptacle must be aligned properly leaving no pins exposed.

- Verify that the board hardware jumpers match the on-line hardware jumper screen located on the operator interface that is supplied with the Mark V LM Control System and move the jumper(s) if necessary. The jumpers in the digital output circuits can provide power to an external device from the Mark V LM (solenoid output) or they can be configured as "dry" contacts (power provided by an external source). Verify each digital output has only one source of power. If any questions arise, contact GE Industrial Systems - Product Service.
- Use appropriate caution while replacing each board carrier when the core inspection is complete. Avoid binding, pinching, or chafing the ribbon cables and wire harnesses. Prior to closing the core door, push in the two silver retaining clips at the lower front corners of the core to lock the board carriers in place.

Wiring and Circuit Checks

The following steps should be completed in order to perform a check of the wiring and circuits of the Mark V LM controller.

- Check that all incoming wiring agrees with the elementary drawings supplied with the controller, and is complete and correct.
- Check that incoming power is the correct voltage and frequency.
- Make sure that the incoming wiring conforms to approved wiring practices, as described previously (Section 3-3.).
- Check that all electrical terminal connections are tight.
- Make sure that no wiring has been damaged or frayed during installation. Replace if necessary.

Controller Initial Energization

The following steps should be followed before energizing the Mark V LM controller for the first time:

- Verify no grounds exist in the control wiring.
- Verify only one ground exists in the controller by lifting the braided conductor and capacitor that connect CCOM to the controller ground. Measure with an ohmmeter between the CCOM bus and controller ground. If the ohms measured are low, resolve any extra grounds before continuing. Be sure the ground reference jumper in the <PD> core is in the correct position.
- Reconnect the ground braided-conductor and capacitor.

Caution

Failure to check and resolve grounds on field-connected wiring and cabling can cause damage to either Mark V LM turbine control system components or field devices, or both.

Do not connect the output of a battery charger directly to the Mark V LM turbine controller without the battery being connected to the charger; serious damage can result to the Mark V LM power supplies.

- Verify polarity and voltage of dc and/or ac supplies. If the battery system is referenced to ground, verify in accordance with plant drawings.
- Apply power to the controller cores one at a time while monitoring source voltage. (Turn one on, check voltages, turn it off. Turn on next one, etc.) If a ground exists, resolve before continuing.
- Verify LEDs and fuses in the <PD> core. See Appendix C of this manual.
- If desired or necessary, the voltages of the individual power supplies can be checked using Table 3-2.

Table 3-2. Power Supply Voltages and Testpoints

Core	Board	AC or DC	Nominal	Positive or "Hot" *	Negative or Neutral [1]	Regulated	Acceptable Range	Fuse Number or Comment
PD	--------	dc	125	ST-DCHI	ST–DCLOW	No	100 – 144	User Supplied
		ac	120/240	ST-AC1H	ST–AC1N	No	108 – 132/200/264	User Supplied
		ac	120/240	ST-AC2H	ST–AC2N	No	108 – 132/200/264	User Supplied
R1	TCPS	dc	+15	TP-P15	TP-DCOM	Yes	14.25 – 15.75	--------
R2		dc	-15	TP-N15	TP-DCOM	Yes	-15.75 – -14.25	--------
R3		dc	+24	TP-+24V	TP-DCOM	No	21.6 – 32	FU1 -5A
R		dc	+5	TP-+5V	TP-DCOM	Yes	4.75 – 5.25	FU3 - 8A
R5		dc	-24	TP--24V	TP--24V	No	-32 – -21.6	FU2 - 1.5A
P1	TCEA	dc	-15	TP-N15	TP-COM	Yes	-15.75 – -14.25	--------
		dc	+15	TP-P15	TP-COM	Yes	14.25 – 15.75	--------
		dc	+5	TP-P5	TP-COM	Yes	4.75 – 5.25	--------
		dc	+24	TP-P24	TP-COM	No	21.6 – 32	--------
		dc	+24	TP-P24A	TP-N24A	No	21.6 – 32	--------
		dc	+335	PL-JW1	PL-JW2	No	300 – 375	--------

*TP = Testpoint; PL = Plug; ST = Screw Terminal.

Operator Interface Installation and Startup

The operator interface for a Mark V LM controller is called a Human-Machine Interface (HMI). It consists of a PC with color monitor, keyboard and Central Processing Unit (CPU). The CPU contains an ARCNET interface board, RS-232 ports, parallel port, cursor positioning device, and a printer. An ARCNET cable called Stagelink is the communication path between a Mark V LM and HMI. Communication with a Distributed Control System (DCS) can be accomplished with MODBUS protocol over a serial communication link through LDDS's or modems. Alarm and event logging is accomplished using a dot matrix printer. Optionally, additional dot matrix printer(s), laser printer(s), and/or color printer(s) may be supplied. Alarms, events, and/or normal printing functions can be directed to one or more printers connected to the operator interface.

Note The auxiliary components of an operator interface such as printer(s), LDDS(s), and Ethernet board(s) may not be the same for all HMIs on a particular site.

The items below briefly describe how to set up and HMI. More detailed information may be available in the HMI manual or the HMI drawings provided with the site-specific documentation.

- Connect required components to CPU with the cables provided.
- Verify settings of any switches and hardware jumpers prior to applying power to the operator interface. Most of these are preset before shipping.
- Configure the monitor.
- Note the manufacturer, model number and serial number of the ARCNET interface board. This board is factory preset and settings should not be changed.
- If an Ethernet interface board is provided, it has preset hardware jumpers. These should only be checked when troubleshooting the Ethernet communication network.
- Connect the operator interface components to the site ac power and energize.
- Configure the operator interface per the instructions in the HMI manual.
- Verify the HMI is functioning properly.
- Configure the printer.
- Install requisition and product specific software on the HMI per the instructions provided.

Controller Processor Startup

This section outlines how to start the Mark V LM Controller. At least one operator interface must be started up to complete the following steps.

- Energize the <R>, <R1>, <R2>, <R3> and <R5> cores and verify their IO states.
- Verify the Stagelink ID of the controller with the drawings supplied. This is set on the PANA daughterboard on the LBC586P Control Engine board in the <R> core. Set the Stagelink address as described in paragraph 3-8.
- Establish ARCNET communication with the HMI by connecting the Stagelink cable to the AAHA1 board in the <R> core. A 93-ohm termination resistor must be connected to the Stagelink at the last HMI on the network.
- Verify Stagelink communications using the operator interface displays. If no valid data is displayed, the ARCNET communication has failed. Verify the following is correct:
  - Cable and connector integrity.
  - Tee adapter and 93-ohm termination resistor are installed on the last HMI in the network.
  - Stagelink ID and LAN Unit Number (LUN) match. The LUN is located on the Configuration file on the operator interface that tells the interface what the Stagelink ID(s) are for the units it is looking at.
  - Verify the switches and jumpers on the ARCNET interface board are correct.
  - Perform an ARCWHO on the operator interface to verify what units are seen on the Stagelink. If the network is experiencing problems, the message *The network is unstable* displays.
- Download configuration files to the Mark V LM per the installation instructions provided.

Stagelink Settings

Each node on the Stagelink must have its own unique Stagelink ID. The <R> core and HMI have limitations on which Stagelink IDs may be used. Stagelink IDs are expressed in hexadecimal format, with the HMI Stagelink ID range being from 01 to 2F in hexadecimal format, beginning with 2F.

The HMI Stagelink IDs are set using DIP switches located on the ARCNET board in the HMI. The Mark V LM Control Engine Stagelink ID is set by rotary switches on the PANA daughterboard mounted on the LBC586P board located in the <R> core. The PANA board has four rotary switches across its upper edge. The pair on the left is to set the Stagelink ID. The pair on the right is to set the Control Engine COREBUS ID.

The rotary switch dials have a small arrow pointing to the number selected, which is perpendicular to the slot provided for an adjustment screwdriver. The Stagelink setting may need to be changed from what was set at the factory if there are multiple Mark V LM Controllers on a single Stagelink network. The COREBUS address is set at the factory and should not need to be adjusted during installation.

Notes

Chapter 4 Hardware Description

Introduction

This chapter describes the Mark V LM hardware and describes the functions of the printed wiring boards (PWB), terminal boards (TB) and their interconnections. Appendix B shows the cable interconnections within the controller, while Appendix D shows the signal flow diagrams for input and output signals. Chapter 5 describes how the Control Engine processes these signals for control and monitoring functions.

This chapter is presented as follows:

Core Structure

More detailed PWB and TB descriptions are provided in sections Printed Wiring Boards and Printed Wiring Terminal Boards in this chapter

The Mark V LM controller consists of several **cores.** Cores are sheet metal housings with Printed Wiring Board (PWB) holders called card carriers. A core can have a maximum of five boards mounted in the card carriers. In addition, up to four high-density IO terminal boards can be mounted on a single core. The combination of boards in a core is dependent upon the function the core is designed to carry out. See Figure 1-1 for a picture of a typical Mark V LM core layout.

Note The terms card and board both apply to the printed wiring boards. In this manual, *board* is the preferred term. However, *card* is used in some drawings and terms if it is pre-established nomenclature – for example, card carrier.

Control Engine Core

The Control Engine core, or <CE> is the main control processor that is used to protect, monitor, and control the unit and to communicate with HMI. This core is commonly known as <R> and contains a Pentium® CPU to process the application software. It contains the following printed wiring boards:

UCIB – Motherboard where the LBC586P and μGENI boards are mounted. Contains a 196 processor that translates serial pressure transducer signals from the TCSA board for the LBC586P. Location 1.

LBC586P – Daughterboard on the UCIB that contains a Pentium processor. The PANA board for ARCNET communications is mounted as a daughterboard on the LBC586P. Location 1.

PANA – The ARCNET driver for internal communications with the I/O cores. Mounted as a daughterboard to the UCIA board. Location 1.

TCSA – Contains decoders for serial communication between the XDSA board on the fuel skid and the UCIB for Dry Low Emissions (DLE) applications. Location 2.

TCPS – Power supply board. Location 5.

AAHA – Board with two BNC connectors for ARCNET™ communication. Two are installed in <R> for Stage Link connection to the HMI and for the COREBUS connections to the I/O Cores. Location 6.

Protective Core

The <P1> core contains triple-redundant protective processors for emergency overspeed detection and trip signal initiation, provide ultraviolet flame detector excitation voltage, and synchronization for generator drive applications. These functions are voted using a “two out of three voting” process, with the voted value used in the protective algorithms and sequencing. <P1> contains the following printed wiring boards:

TCEA – Contains the processor circuitry for critical protective functions. Locations 1, 3 and 5.

TCEB – Expander board for the TCEA boards. Location 2.

TCTG – The board where the fuel valve trip solenoids are located. Location 4.

PTBA – Protective core terminal board. Location 6.

Analog Cores

The analog IO cores are used to read and write analog signals. These cores contain an IO Engine with 486DX processor for communication with the I/O Cards and Control Engine. Processors on the TCQA, TCQC, TCQE, TCCA and TCCB boards scale and condition the analog signals using IO Configuration information. This data is then communicated via COREBUS with the Control Engine in <R> for use in the Control Signal Database (CSDB). After the application software processes the signals, the resulting output signals are then sent back across the COREBUS to the IO cores. The IO cores contain combinations of the following printed wiring boards:

STCA – Motherboard where the UCPB is mounted. IONET master for the digital and protective cores and processes some signals. Provides synchronization check. Location 1.

UCPB – Daughterboard on the STCA. The IO Engine 486DX processor is on the UCPB. It acts as the IO "switchboard" between the Control Engine and the IO Cards and processes some signals. Location 1.

PCM-COM4A – Daughterboard on the UCPB that facilitates serial communication with the FMVED system. Also known simply as PCM. Location 1 in <R2> only. Configuration of this board is described in the FMVED commissioning guide.

TCQA – Analog control IO board that processes LVDT input, pulse rate input, servo output, thermocouple, milliamp (mA) input, mA output, voltage input and seismic vibration signals. Location 2 in <R1>, <R2> and <R3>.

TCQE – LM analog control IO board that processes mA output, RTD, pulse rate input, LVDT input and accelerometer, and vibration signals. Location 3 in <R1>.

TCCA – Analog IO board that processes thermocouple, RTD, mA input and mA output signals. Location 2 in <R5>.

TCCB – Analog IO board that processes RTD, mA input and generator output signals. Location 3 in <R5>.

TCQC – Expander board for the TCQA board and the IONET cable connection interface for <Q11>and <P1> in <R1> and <Q51> in <R5>. Location 4 in <R1>, <R2> and <R3>.

TCPS – Power supply board. Location 5.

QTBA – Terminal Board that contains the IONET and COREBUS communication connections and screw terminations for LVDT excitation, servo outputs, pulse rate inputs and a WATT/VAR transducer input. Location 6 in <R1>, <R2>, and <R3>.

TBQA – Terminal Board with screw terminations for thermocouple inputs. Location 8 in <R1> and <R5>.

TBQB – Terminal Board with screw terminations for voltage inputs, seismic vibration inputs, pulse rate inputs and a mA input. Location 7 in <R2> and <R3>, where the TBQB in <R2> is actually connected to <R1>.

TBQC – Terminal Board with screw terminations for mA outputs, mA inputs and LVDT inputs. Location 9 in <R1>, <R2> and <R3>.

TBQE – Terminal Board with screw terminations for mA outputs, LVDT inputs and accelerometer inputs, vibration inputs and RTD inputs. Location 7 in <R1>.

TBSA – Terminal Board with screw terminations for the DLE gas pressure sensor serial link and Fuel Metering Valve Electric Drive (FMVED) serial link. Location 8 in <R2>.

CTBA – Terminal Board that contains IONET and COREBUS communication connections and screw terminations for mA outputs, mA inputs and shaft voltage inputs. Location 6 in <R5>.

TBCB – Terminal Board with screw terminations for mA inputs and RTD inputs. Location 7 in <R5>.

TBCA – Terminal Board with screw terminations for RTD inputs. Location 9 in <R5>.

Digital Cores

Two digital IO cores, called <Q11> and <Q51>, are installed in the Mark V LM controller. An optional third digital core, called <Q21>, may be connected to <R2>. It must be mounted outside of the Mark V LM controller. These cores communicate with the IO Engine through a serial link called the IONET. The digital I/O cores contain the following printed wiring boards:

TCDA – Conditions the digital IO signals and communicates their status via the IONET. Location 1 in <Q11>, <Q21> and <Q51>.

TCRA – Relay boards for the contact outputs. Locations 4 and 5 in <Q11>, <Q21> and <Q51>.

DTBA – Digital Input terminal board. Location 6 in <Q11>, <Q21> and <Q51>.

DTBB – Digital Input terminal board. Location 7 in <Q11>, <Q21> and <Q51>.

DTBC – Digital Output terminal board. Location 8 in <Q11>, <Q21> and <Q51>. The DTBC in Q11 contains only four relays and is connected directly to TCQE in <R1> for gas manifold blow-off valve control.

DTBD – Digital Output terminal board. Location 9 in <Q11>, <Q21> and <Q51>.

Power Distribution Core

The Power Distribution core, called <PD>, supplies 125V dc to the TCPS power supply boards located in <R>, <R1>, <R2>, <R3> and <R5> for distribution to the analog IO cards. It supplies 125V dc power directly to the TCEA and TCTG boards in <P1>, and to the DTBA, DTBC and DTBD terminal boards in the digital cores. The <PD> core contains the following printed wiring board:

TCPD – Contains the circuitry and toggle switches that distribute 125V dc power to the controller.

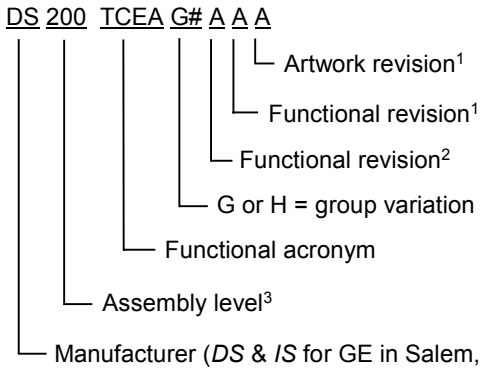
TB1 – 12-point terminal board for connecting ac or DC power to the Mark V LM controller.

TB2 – Four-point terminal board for setting contact input excitation to either 24V dc or 125VC.

Board Identification

An alphanumeric **part (catalog) number** designates a PWB or TB. Two part numbering series are commonly used for these boards at GE Industrial Systems. Most Mark V LM boards are have part numbers beginning with the characters DS200 or DS215. For example, the protective processor board is identified by part number DS200TCEAG#ruu. The characters in the part number provide information about the board, as shown by Figure 4-1. All of these characters are important when ordering or replacing any board. Chapter 9 contains information on spare and renewal parts.

Note The terms card and board both apply to the printed wiring boards. In this manual, *board* is the preferred term. However, *card* is used in some drawings and terms if it is pre-established nomenclature – for example, card carrier.



[1]Backward compatible
[2]Not backward compatible (essentially a new catalog number)
[3]*200* indicates a base-level board; *215* indicates a higher-level assembly or added components (such as PROM or firmware)

Figure 4-1. Sample Board Part Number, DS Series

Board Configuration

The IO boards in the Mark V LM controller are configured using a combination of hardware jumpers and software. Many boards in the Mark V LM controller have hardware jumpers for enabling or scaling input and output functions. Appendix A describes the hardware jumper settings, while the signal flow diagrams in Appendix D show how they affect input and output circuits.

Warning

Potentially hazardous voltages are present in the controller circuits. Do not assume any cable or any circuitry to be without power if one end of that cable could be connected to a power source. To prevent accidental electrical shock, do not touch any circuitry or bare wire without first ensuring that it does not carry electricity.

Caution

To prevent component damage caused by static electricity, treat all boards and devices with static-sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.

Initial Hardware Jumper Settings

The factory sets hardware jumpers to enable normal card operation when manufacturing and testing the controller. For adjustments that are not factory-set, normally those affecting site-specific IO, refer to Appendix A. The hardware jumpers are designated with *J, BJ* or *JP* nomenclature on the boards and diagrams in this manual.

Caution

All hardware jumper settings should be verified before energizing the Mark V LM controller.

Adjusting Replacement Boards

When replacing a board, set the hardware jumper settings on the new board to match the settings on the board being replaced. Chapter 9 provides instructions for replacing a board.

Note Boards being replaced should be kept until the new replacement board arrives. Before returning any board, verify the hardware jumper settings. EPROMs from the old board should be removed and used on the new board.

I/O Board Software Configuration

The IO boards are programmed to scale and condition IO signals using firmware contained in EEPROM and configuration data stored in RAM. The IO configuration for all boards associated with a specific IO Engine is loaded during every reboot/startup of their corresponding IO Engine. Each IO Engine receives configuration data from the Control Engine in the <R> core. The Control Engine maintains the data until changed by a download from the operator interface over the Stage Link. The user sets IO configuration data using the I/O Configuration Editor from the operator interface.

Printed Wiring Boards

This section describes the printed wiring boards used in the Mark V LM controller. The sample hardware document in Appendix B shows the location of each board with its interconnection information.

DS200AAHA – ARCNET Connection Board

The ARCNET Connection Board (AAHA) provides the interface connection for ARCNET cables linking <R> to the IO cores and HMI. Two BNC connections (channels A and B) are provided. One plug connector, the APL connector, is provided for communication with the boards containing the ARCNET drivers in <R>. The APL connector links the AAHA board with the APL or BPL connector on the PANA board. Two AAHA boards are in location 6 of <R>.

One AAHA, labeled AAHA1 in Appendix B, is for the Stage Link between <R> and the operator interfaces. When both BNC connectors on this board are used, either two independent Stage Links can be connected to one controller or another controller can be connected to the Stage Link. The APL connector on AAHA1 connects to the APL connector on PANA.

The second AAHA, labeled AAHA2 in Appendix B, connects <R> to the COREBUS link that allows the Control Engine to communicate to the IO cores. COREBUS is name of the internal ARCNET link for the Mark V LM controller IO communications. The APL connector on AAHA2 connects to the BPL connector on PANA.

AAHA Connectors

2PL – Power from the TCPS board in <R>.

APL – ARCNET connection between the AAHA board and PANA board in <R>.

ARCBNC A – BNC connector for ARCNET communication.

ARCBNC B – BNC connector for ARCNET communication.

EBNC – Typically not used.

EPL – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

AAHA Configuration

There is no hardware or software configuration done on the AAHA board.

DS200PANA – ARCNET LAN Driver Board

The LAN Driver Board (PANA) provides ARCNET communication for COREBUS and Stage Link. Located as a daughterboard on the LBC586P board in <R>, PANA connects to both AAHA boards through its APL and BPL connectors. The PANA board transfers the data to the Control Engine LBC586P processor board through its P1 and P2 bus connectors. One PANA board is in location 1 of <R>.

PANA Connectors

APL – ARCNET communication link to the AAHA1 board.

BPL – ARCNET communication link to the AAHA2 board.

P1 – Bus connection to the LBC586P board.

P2 – Bus connection to the LBC586P board.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

PANA Configuration

Hardware. The four switches on the PANA board are used to set the COREBUS and Stage Link ARCNET addresses for the <R> core. Two are for channel A (Stage Link) and two are for channel B (COREBUS). Hardware jumpers are used to set the interrupt, I/O address and memory address for each ARCNET channel. These settings are all factory-specific to the internal software settings. Hardware jumper settings on replacement boards should be verified that they are configured the same as the hardware jumper settings on the old board. Refer to Appendix A for information on the hardware jumper settings for this board.

Software. There is no software configuration used on the PANA board.

DS200STCA – Turbine Communication Board

The Turbine Communication Board (STCA) functions as the IONET master for the I/O cores. Each of the I/O cores has an STCA board. Signals are read through the various connectors, conditioned and written to the I/O Engine located on the UCPB daughterboard via the bus connectors J1 and J3. The signals are written to the COREBUS connections located on the QTBA or CTBA boards via the JEE connector.

STCA Connectors

2PL – Distributes power from the TCPS board in each I/O core.

3PL – The Data Bus between the STCA and TCQA boards in cores <R2> and <R3>, between STCA, TCQA, and TCQE boards in core <R1>, and between STCA, TCCA and TCCB boards in core <R5>. Conditioned signals are transferred to the COREBUS on the 3PL connector.

8PL – I/O connector to the TCQC boards in cores <R1>, <R2>, and <R3> and to the CTBA board in <R5>. Signals may include the COM1 RS232 output signals, the serial I/O signals, the ac and DC power monitoring signals (TCPD), and an auxiliary pulse rate magnetic pick up signal.

19PL – I/O connector to the TCQC board. The I/O signals may include megawatt, generator, and bus signals, and the magnetic pick up pulse rate signals from the high pressure shafts. Power bus and neutral bus signals may also be carried in this connector (TCPS). The 19PL connector may not be used in every core. Other signals could be carried on this connector.

ARCNET – Interfaces the ARCNET signals from the UCPB daughterboard in the IO cores.

COM1 – RS232 interface signals used for the terminal interface.

FAN – Power connection to the fan that cools the 486DX CPU on the UCPB board.

J1 – Bus connection to the UCPB daughterboard.

J3 – Bus connection to the UCPB daughterboard.

JEE – Communicates between the STCA board and the QTBA or CTBA terminal boards for the COREBUS.

2PLX – Parallels 2PL connections. (Typically not used.)

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

STCA Configuration

Hardware. Hardware jumper JP2 enables the test points for factory test. Hardware jumper JP4 selects the voltage needed for the flash EPROM. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. I/O configuration constants for the pulse rate inputs, compressor stall detector and synchronization settings are entered in the I/O Configuration Editor on the operator interface as described below.

STCA Pulse Rate Input Circuit

The STCA board scales and conditions the pulse rate inputs read from the TCQC board. These signals originate from magnetic pick up devices whose signals are written to the TCQC board by the QTBA, TBQB, and/or PTBA terminal boards. The <R1> core reads the high pressure shaft pulse rate inputs. The pulse rate inputs in each core are independent and are used for different purposes.

STCA Synch Check Circuit

The generator and bus voltage inputs are read from the TCQC board via the 19PL connector. These signals originate on the PTBA terminal board in the <P1> core and are written to the TCTG board in the <P1> core via the JN connector. The signals are then passed through the TCTG board via the JDR/S/T connectors to the JD connector on the TCQA board in the <R1> core. The signals are passed through again to the TCQC board in the <R1> core via the JE connector. The TCQC board provides scaling and conditioning of the signals prior to writing them to the STCA board via the 19PL connector. The synchronizing check (synch check) is done on the STCA board and the results are sent back across the same path to the TCTG board where they are used in conjunction with the automatic sync signals for generator breaker synchronizing commands.

DS200TCCA – Common Analog I/O Board

The Common Analog I/O Board (TCCA), located in the <R5> core, scales and conditions analog signals from the CTBA, TBQA, and TBCA terminal boards mounted in the <R5> core. These signals include 4–20 mA inputs and outputs, RTD inputs , thermocouple inputs, shaft voltage inputs, and shaft current inputs. The signals are written to the STCA board via the 3PL connector.

TCCA Connectors

2PL – Distributes power from the TCPS board in the <R5> core.

3PL – The Data Bus between the STCA, TCCA and TCCB boards in core <R5>. Conditioned signals are carried on 3PL for transferring to the COREBUS.

JAA – Carries the 4–20 mA output signals to the CTBA terminal board.

JBB – Carries the shaft voltage and current signals and 4–20 mA input signals from the CTBA terminal board.

JCC – Carries RTD input signals from the TBCA terminal board.

JDD – Carries RTD input signals from the TBCA terminal board.

JAR/S/T – Carries Thermocouple input signals and cold junction inputs from the TBQA terminal board.

JC – Carries the Power supply diagnostic signals from TCPS.

JEE – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCCA Configuration

Hardware. There are three hardware jumpers – J1, JP2, and JP3 on the TCCA board. J1 is used to enable/disable the serial RS232 port. JP2 is used to disable the oscillator for card test. JP3 is used for factory test. Refer to Appendix A for information on the hardware jumper settings for this board.

Software. I/O configuration constants for the thermocouples, RTDs, mA inputs and outputs, and the shaft voltage and current settings are entered in the I/O Configuration Editor located on the HMI as described below.

TCCA 4 – 20 mA Input Circuit

The TCCA board provides the circuitry for the 4–20 mA input signals. The signals are read from the CTBA terminal board via the JBB connector. The transducer current is dropped across a burden resistor and the voltage drop is read by the TCCA board and written to the I/O Engine via the 3PL connector.

TCCA 4–20 mA Output Circuit

The TCCA board provides the circuitry for driving 4–20 mA outputs to the CTBA terminal board via the JAA connector. These signals are typically used to drive remote instrumentation for monitoring.

TCCA RTD Circuit

The circuitry that supplies excitation to the RTDs from the TBCA terminal board is located on the TCCA board. A steady current is sent through the RTD and when the temperature changes, the resistance changes causing the voltage on the RTD to change. The TCCA board measures, scales, and conditions the voltage signal. The RTD signals are read from the TBCA terminal board by the TCCA board over the JCC and JDD connectors. The TCCA board sends the signals to the I/O Engine via the 3PL connector. The type of RTD is selected using I/O configuration constants.

TCCA Thermocouple Circuit

The thermocouple inputs are read by the TBQA terminal board. The cold junction signals are provided by the cold junction circuitry located on the TBQA terminal board. These values are used by the TCCA board to calculate the cold junction compensation. The TCCA board uses the thermocouple input and compensation value to calculate the actual temperature read by the thermocouple. The I/O Engine reads the value via the 3PL connector. Thermocouple types and curves are selected using I/O configuration constants.

TCCA Shaft Monitoring

The monitoring for the turbine shaft voltage and current is provided by the TCCA board. These signals are read from the CTBA terminal board via the JBB connector. The signals are written to the I/O Engine via the 3PL connector.

DS200TCCB – Common Extended Analog IO Board

The Common Extended Analog I/O Board (TCCB) provides scaling and conditioning for additional analog I/O signals read from the TBCB terminal Board mounted on the <R5> core and the TCEB board in the <P1> core. These signals include 4–20 mA/0–1 mA inputs, RTDs, generator and bus voltage inputs, and the line current inputs. The STCA board receives the scaled and conditioned signals via the 3PL connector.

TCCB Connectors

2PL – Distributes power from the TCPS board in the <R5> core.

3PL – The Data Bus between the STCA, TCCA and TCCB boards in core <R5>. Conditioned signals are carried on 3PL for transferring to the COREBUS.

JHH – Carries the 4–20 mA/0–1 mA input signals from the TBCB terminal board.

JII – Carries the RTD input signals from the TBCB terminal board.

JMP – Carries the potential and current transformer (PT and CT) signals from the TCEB board in the <P1> core.

JKK – Typically not used.

JTEST – Typically not used.

TCQPL – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCCB Configuration

Hardware. The hardware jumpers J1, J2, J3, J4 and J5 are used to provide the generator and bus voltage monitoring functions and the line current monitoring function in the Mark V LM. Hardware jumper J14 is used to connect the RS232 serial port to DCOM. Hardware jumpers J15 and J16 are used for testing purposes. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. I/O configuration constants for the RTDs, mA inputs, the generator and bus voltage and line current settings are entered in the I/O Configuration Editor located on the HMI as described below.

TCCB 4 – 20 mA Input Circuit

The TCCB board provides the circuitry for the 4–20 mA and 0–1 mA input signals. The signals are read from the TBCB terminal board via the JHH connector. The transducer current is dropped across a burden resistor and the voltage drop is read by the TCCB board and written to the I/O Engine via the 3PL connector. Hardware jumpers on the TBCB terminal board are used to select the current range of the input signals.

TCCB RTD Circuit

The circuitry that supplies excitation to the RTDs from the TBCB terminal board is located on the TCCB board. A steady current is sent through the RTD and when the temperature changes, the resistance changes causing the voltage on the RTD to change. The TCCB board measures, scales, and conditions the voltages. The RTD signals are read from the TBCB terminal board by the TCCB board over the JCC and JDD connectors. The TCCB board sends the signals to the I/O Engine via the 3PL connector. The type of RTD is selected using I/O configuration constants.

TCCB Generator/Bus Voltageand Current Input Circuits

The voltage signals from the generator and bus and the current signals from the line, (PT and CT) are scaled and conditioned on the TCCB board. These signals are used by the TCCB to define the phase currents and voltages and to calculate the generator megawatt, power factor, and VARs used for power system monitoring. These signals are read in from the PTBA terminal board, scaled on the TCEB board in the <P1> core and written to the TCCB board via the JMP connector.

DS200TCDA – Digital IO Board

The Digital IO Board (TCDA), located in the digital I/O cores <Q11>, <Q51> and <Q21> if present. TCDA processes digital contact input signals from the DTBA and DTBB terminal boards and contact output (relay/solenoid) signals from the two TCRA boards. The signals are transmitted over the IONET to the TCQC board in <R1>, <R2> if <Q21> is installed and the CTBA terminal board in <R5>.

TCDA Connectors

JP – Distributes power from the TCPS board in the <R1>, <R2> and <R5> cores to the <Q11>, <Q21> and <Q51> cores respectively.

JQ – Connects to the JQR socket on the DTBA board. Carries the contact input signals from the DTBA board to the TCDA board.

JR – Connects to the JRR socket on the DTBB board. Carries the contact input signals from the DTBB board to the TCDA board.

JO1 – Writes the contact output (relay/solenoid) signals to the TCRA board in location four. Not used in <Q11>, since the relays in location 4 are controlled directly by TCQE in <R1>.

JO2 – Writes the contact output (relay/solenoid) signals to the TCRA board in location five.

JX1 – Shielded twisted pair for the IONET signals. The TCDA board in the <Q11> core writes the signals to the JX2 connection on the TCEA board in location five of the <P1> core. The TCDA board in the <Q51> core writes the signals to the JX connection on the CTBA terminal board in the <R5> core.

JX2 – Used for the same function as JX1. Either JX1 or JX2 can be used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCDA Configuration

Hardware. There are eight hardware jumpers on the TCDA board. J1 and J8 are for factory test. J2 and J3 are for IONET termination resistors. J4, J5, and J6 are used to set up the IONET ID for the board. J7 is the stall timer enable. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. I/O configuration constants for the contact input inversions are entered in the I/O Configuration Editor located on the HMI as described below.

TCDA Contact Input Circuits

The TCDA board carries contact inputs from the DTBA and DTBB terminal boards via the JR and JQ connectors. The circuitry in the TCDA board conditions the signals, time tags any change of state, and carries the signals to the IONET via the JX1 (JX2) connector. The contact signal inversions are done through software using I/O configuration constants.

TCDA Contact Output (Relay/Solenoid) Circuits

The contact output signals are carried to the TCRA boards via the JO1 and JO2 connectors.

DS200TCEA – Emergency Overspeed Board

The Emergency Overspeed Board (TCEA), located in the Protective Core <P1>, is used for the high speed protection circuitry and is often referred to as the Protective Processor. The three TCEA boards used in the <P1> core are referred to as the <X>, <Y>, and <Z> processors. These boards each bring in signals for high and low shaft speed, flame detection and automatic synchronization. The signals are scaled and conditioned and written over the IONET to the STCA board in the <R1> core via the JX1 connector located on the TCEA board in location one, (<X>).

The TCEA boards in location three, (<Y>), and five, (<Z>), transfer their information using the JX1 and JX2 connections via <X>. The I/O Engine in the <R1> core uses the data from the three TCEA boards and performs a median select on the three values and the results are transferred across the COREBUS to the Control Engine. The TCEA boards send emergency trip signals to the Turbine Trip Board (TCTG), each TCEA board sends a trip signal to different relays. The three relays on the TCTG board perform a 2/3 vote (relay driver level voting), and the results determine whether the TCTG board trips the unit. Each TCEA board has its own power supply and power supply diagnostics.

TCEA Connectors

J7 – Distributes the power from the <PD> core to each TCEA board.

JK – Carries the signals to the TCEA board from the TCEB board in location two of the <P1> core. JK connects to either JKX, JKY or JKZ connectors on the TCEB board. This board is the Protection Termination Expander Board on which all of the signals are brought in and transferred to the TCEA boards. <X> connects to JKX, <Y> connects to JKY, and <Z> connects to JKZ.

JL – Carries the trip signals to the Turbine Trip Board (TCTG) in location four of the <P1> core. Each TCEA board connects to a different connection on the TCTG board. JL on <X> connects to JLX, JL on <Y> connects to JLY, and JL on <Z> connects to JLZ.

JW – Carries the 335 V dc for the flame detectors to the TCEB board. JW connects to the JWX/Y/Z connectors on the TCEB board. <X> connects to JWX, <Y> connects to JWY, and <Z> connects to JWZ.

JX1 – Daisy chained IONET connectors. JX1 on <X> connects to the JX connector on the TCQC board in the <R1> core. This IONET connection reads/writes all of the <P1> core signals and digital I/O, <Q11>, core signals to the I/O Engine in <R1>. JX1 on <Y> connects to the JX2 socket on <X> allowing it to be on the daisy chain. The JX1 connector on <Z> connects to the JX2 socket on <Y>. Again this allows it to be on the daisy chain. All of the signals are carried from board to board over the daisy chain until they arrive at the TCQC board in the <R1> core.

JX2 – Daisy chained IONET connectors. JX2 on <X> connects to the JX1 connector on <Y>. JX2 on <Y> connects to the JX1 connector on <Z>. The JX2 connector on <Z> connects to the TCDA board in the <Q11> core. This allows the digital signals to follow the daisy chain up the IONET to the <R1> core.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCEA Configuration

Hardware. The TCEA board's hardware jumpers J1 and J31 are used for factory test. J2 and J3 are used for IONET termination resistors. Hardware jumpers J4, J5 and J6 are used to set up the IONET address for each TCEA board. Overspeed trip frequency settings are confirmed using J12 through J21 for the high pressure shaft and J8 through J11 and J22 through 27 for the low pressure shaft. The actual configuration is done through the I/O configuration software. J28 and J29 hardware jumpers cause <Z> to always vote for a trip on emergency overspeed. J30 enables the stall timer. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. The IO Configuration Editor is used to set the base speed and overspeed values for both the high and low pressure shafts and calculates the hardware jumper settings for trip frequency. The pulse rate information from the Ultra Violet (UV) flame detectors is selected and the auto-synchronization permissive values are chosen in the IO Configuration Editor as described below.

TCEA Flame Detection Circuits

Signals from the UV flame detectors are brought into the PTBA board in the <P1> core. These signals are read from the PTBA terminal board via the JVA and JU connectors to the TCEB board and are written to the TCEA board via the JK (JKX/Y/Z) connectors. The signals are scaled, conditioned and the intensity calculated using internal algorithms to determine the flame status. The flame detect signals are used by the Control Sequence Program (CSP) in the <R> core. These signals are sent via the IONET to the I/O Engine, which sends them to the Control Engine. JW (JWX/Y/Z) carries the 335 V dc to the flame detectors.

TCEA Turbine Overspeed Circuit

The I/O configuration constants determine the emergency overspeed trip level settings, and the hardware jumpers confirm the overspeed settings. The shaft speed magnetic pick-ups land on the PTBA terminal board in the <P1> core for the emergency overspeed circuit. The PTBA board parallels the signals to the <R1> core for use in Control Sequence Program for primary overspeed. The TCEA board calculates shaft speed using I/O configuration constants. The TCEA board compares the calculated shaft speeds with the I/O configuration constants trip values to detect an overspeed trip condition.

If a trip condition is detected, the circuit will de-energize the Emergency Trip Relays (ETRs) on the Turbine Trip Board (TCTG) to trip the unit. Hardware jumpers J28 and J29 on <Z> configure <Z> to always call for an emergency overspeed trip. J28 and J29 work in conjunction with the IONET address jumpers J4, J5, and J6 and embedded software. If the IONET address tells the TCEA board it is a <Z> board, the board will always vote for an emergency overspeed trip. This causes the system to have a dual redundant system for the emergency overspeed trip conditions. If either <X> or <Y> call for an emergency overspeed trip, the unit will trip. J28 and J29 must be set the same for <X>, <Y>, and <Z>.

TCEA Automatic Synchronizing Circuit

The bus and generator voltages from the PTBA terminal board are sent through the JV connector to the TCEB board where the JMP connector transferred them to the TCEA board. Embedded software in EPROMs on the TCEA board performs speed matching and voltage matching. The TCEA board sends the permissive to close the breaker after checking for proper generator and line voltages and frequencies and that the differential between the line and the generator is within the limits set by the I/O Configuration constant. The STCA board performs a separate synchronization check function, which sends a logic signal to the TCEA board. This logic must be satisfied to enable a breaker closure.

DS200TCEB – Protective Termination Expander Board

The Protective Termination Expander Board (TCEB), located in the <P1> core, scales the PT and CT signals used by the TCCB board in the <R5> core. These signals are used for the generator and bus voltages and the line current and are landed on the PTBA terminal board. Signals for emergency overspeed and flame detect come from the PTBA terminal board and are passed through the TCEB board to the TCEA boards for processing. The 335 V dc needed for the flame detector devices passes across this board from the TCEA boards, is conditioned, sent to the PTBA terminal board and out to the sensors. The alarm horn for the Mark V LM is also located on the TCEB board.

TCEB Connectors

JKX/Y/Z – Carries the emergency overspeed magnetic pick up signals and flame detection signals to the TCEA boards in locations <X>, <Y>, and <Z> respectively.

JMP – Carries the PT and CT signals to the TCCB board in the <R5> core.

JU – Carries the magnetic pick up and flame detect signals from the PTBA terminal board.

JV – Carries the PT and CT signals from the PTBA terminal board.

JVA – Carries the 335 V dc to the PTBA terminal board for the UV flame detector devices.

JWX/Y/Z – Carries the 335 V dc from the TCEA board and conditions the signal prior to the TCEB board writing the 335 V dc to the PTBA terminal board via the JVA connector.

JPU – Typically not used.

JPV – Typically not used.

JPW – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCEB Configuration

Hardware. There are no hardware jumpers on the TCEB board. The alarm horn jumper is located on the PTBA terminal board.

Software. There is no software configuration for the TCEB board.

TCEB PT and CT Circuit

The PT and CT signals are read via t JV connector from the PTBA terminal board. These signals are stepped down and written to the TCCB board in the <R5> core via the JMP connector where they are used for imbedded functions. Any configuration associated with these signals is done in the <R5> core.

TCEB Flame Detection Circuit

The flame detection signals are read via the JU connector from the PTBA board and passed through and written to the TCEA boards via JKX/Y/Z connectors. Some conditioning is done on the 335 V dc signals passed through the TCEB board prior to being written to the PTBA terminal board. The signals are read on the JWX, JWY, and JWZ connectors, and written to the PTBA board via the JVA connector.

TCEB Emergency Overspeed Circuit

The magnetic pick up signals for emergency overspeed are read from the PTBA board via the JU connector and passed through the TCEB board to the TCEA boards via the JKX, JKY, and JKZ connectors.

DS200TCPD – Power Distribution Module

The Power Distribution Board (TCPD), located in <PD>, distributes the 125 V dc power to the TCPS boards in each IO core, the Control Engine core, and the TCEA boards in <P1> core. The TCPD board provides switches for powering down each core individually. The digital I/O cores (<Q11>, <Q21> and <Q51>) do not receive their power directly from <PD>, these cores get their power from their associated IO core. The DTBC and DTBD (solenoid output power) terminal boards in the digital cores are powered directly from the TCPD board. The 120/240 V ac power for the ignition transformers connected to DTBC is supplied directly from the TCPD board. The CTBA terminal board in the <R5> receives power from the TCPD for <PD> power output monitoring.

TCPD Connectors

J1R – Distributes the 125 V dc power to the TCPS board in the <R1> core.

J1S – Distributes the 125 V dc power to the TCPS board in the <R2> core.

J1T – Distributes the 125 V dc power to the TCPS board in the <R3> core.

J1C – Distributes the 125 V dc power to the TCPS board in the <R5> core.

J1D – Distributes the 125 V dc power to the TCPS board in the <R> core

J7W – Distributes the 125 V dc power to the TCTG board in the <P1> core.

J7X – Distributes the 125 V dc power to the TCEA board in location one ,<X>, in the <P1> core.

J7Y – Distributes the 125 V dc power to the TCEA board in location three, <Y>, in the <P1> core.

J7Z – Distributes the 125 V dc power to the TCEA board in location five, <Z>, in the <P1> core.

J8A – Distributes the 125 V dc power to the DTBC board in the <Q51> core for the solenoids.

J8B – Distributes the 125 V dc power to the DTBD board in the <Q51> core for the solenoids.

J8C – Distributes the 125 V dc power to the DTBC board in the <Q11> core for the solenoids.

J8D – Distributes the 125 V dc power to the DTBD board in the <Q11> core for the solenoids.

J12A – Distributes the 125 V dc power to the DTBA board in the <Q51> core for the wetted contact inputs.

J12B – Distributes the 125 V dc power to the DTBA board in the <Q11> core for the wetted contact inputs.

J15 – Typically not used.

J16 – Typically not used.

J19 – Typically not used.

J20 – Typically not used.

JPD – Distributes power to CTBA in <R5>. Used by <R5> to monitor <PD> ac and DC power output.

JZ1 – Connection for the TCEA boards and contact input power to drop across the external resistors.

JZ2 – Incoming ac from the TB1 terminal board connected through JZ2 to the DACA, (ac to DC converter), via the JZ connector in the DACA box. Used for ac to DC conversion.

JZ3 – Alternate for JZ2 if reduced voltage needed for special contact output circuit (contact output #18 on the DTBC board of the <Q51>).

JZ4 – Auxiliary ac source connection point for applications that require an isolated input for an uninterruptable power source connection(s) and/or switched back up power source. Typically used for a Black Start Inverter.

JZ5 – Standard ac power source connection for the ignition transformers.

J2R – Typically not used.

J2S – Typically not used.

J2T – Typically not used.

J7A – Typically not used.

J12C – Typically not used.

J17 – Typically not used.

J18 – Typically not used.

The hardware document in Appendix B and the diagrams in Appendix C contain more information.

TCPD Configuration

Hardware. The BJS hardware jumper is supplied for isolation of the ground reference on systems with an external reference. When the jumper is in, the ground reference is provided for the external reference systems. Refer to Appendix A for more information on the hardware jumper setting for this board.

Software. There is no software configuration for the TCPD board.

TCPD Switches

The TCPD board has several switches associated with it. Each switch toggles on and off the power for the particular core or board associated with it.

SW1 – Toggles power in the <R1> core.

SW2 – Toggles power in the <R2> core.

SW3 – Toggles power in the <R3> core.

SW4 – Toggles power in the <R5> core.

SW5 – Toggles power in the <R> core.

SW6 – Toggles power on <X> in the <P1> core.

SW7 – Toggles power on <Y> in the <P1> core.

SW8 – Toggles power on <Z> in the <P1> core.

TCPD Power

External 115/230 V ac power and 125 V dc power is brought in via TB1 mounted on the <PD> core and hard wired to the TCPD board. If ac power is provided, it is converted to the 125 V dc in a DACA (ac to DC) via the JZ2 connector. Power is distributed from <PD> to the various cores and boards via the connectors listed above. An optional JZ3 connection is available for applications requiring reduced voltages for contact #18 on the DTBC board in the <Q51> core. The power distributed to the TCEA boards in the <P1> core is additionally conditioned across resistors via the JZ1 connector. If ac power is provided, the JZ5 connector provides ac power to the ignition transformer outputs.

DS200TCPS – Power Supply Board

The Power Supply Board (TCPS) is located in <R> and each of the four IO cores to convert 125 V dc power from <PD> to the voltage levels required. These include, but are not limited to such things as, microprocessor power supply voltages, mA output power supply voltages, RTD power supply voltages, and servo valve current outputs.

TCPS Connectors

2PL – Distributes the power supply voltages to the various boards in a daisy chain fashion.

J1 – Connector that brings in the 125 V dc power into the TCPS board from the TCPD board in the <PD> core.

JC – Distributes power supply voltages for the power supply diagnostics on the TCQC board in cores <R1>, <R2> and <R3> and the TCCA board in the <R5> core.

JP1 – Distributes power supply voltages to the TCDA board in the digital cores <Q11>, <Q21> and <Q51> and to the AAHA boards in the <R> core.

JP2 – Same as JP1. Either JP1 or JP2 could be used.

X1 – CCOM bus connection.

The hardware document in Appendix B contains more information on core power distribution.

TCPS Configuration

There are no hardware jumper or software configurations for the TCPS boards.

DS200TCQA – Analog IO Board

The Analog IO Board (TCQA) scales and conditions many of the analog signals read in by terminal boards mounted on the I/O cores <R1>, <R2>, and <R3>. These signals include the LVDT inputs, servo valve outputs, thermocouple inputs, 4–20 mA inputs and outputs, vibration inputs, relay driver outputs, pulse inputs, voltage inputs, and generator and line signals. Some of the signals are written to the STCA board via the 3PL connector. The generator and line signals are exchanged with the TCQC board via the JE connector. 4–20 mA input signals such as the fuel flow pressure and compressor stall-detect signals are scaled and conditioned on the TCQA board.

TCQA Connectors

2PL – Distributes power from the TCPS board in the <R1>, <R2> and <R3> cores..

3PL – The Data Bus between the STCA and TCQA boards in cores <R2> and <R3> and between STCA, TCQA, and TCQE boards in core <R1>. Conditioned signals are carried on 3PL for transferring to the COREBUS.

JA – Carries the thermocouple inputs and cold junction compensation from the TBQA board connector JAR/S/T for cores <R1>, <R2>, and <R3> respectively.

JB – Carries the 4–20 mA inputs and outputs to/from the TBQC terminal board connector JBR.

JD – Carries trip signals to the TCTG board in the <P1> core from the <R1> core, not used in <R2> or <R3>.

JE – Carries the servo valve driver outputs, relay driver outputs, generator and line signals, and the pulse signals to/from the TCQC board. Carries the power supply monitor inputs.

JF – Carries the LVDT/LVDR position inputs from the TBQC terminal board connector JFR.

JG – Carries the vibration inputs from the TBQB terminal board connector JGR and carries the +/- 10 V dc inputs.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCQA Configuration

Hardware. Hardware jumpers J1 and J2 are used to select the mA output circuits. J5 and J6 are used to configure the mA outputs current range, either 20 mA maximum or 200 mA maximum. J7 is used for the RS232 port for card tests. J8 enables an oscillator. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. I/O Configuration constants for the thermocouples, pulse rates, vibrations, LVDT positions and the 4–20 mA inputs and outputs are entered in the I/O Configuration Editor located on the operator interface as described below.

Pulse Rate Input Circuit

The TCQA board contains the circuitry that scales and conditions the pulse rate inputs read from the TCQC board via the JE connector. These signals originate from the TTL (transistor to transistor logic) and magnetic pick up inputs whose signals are brought into the QTBA and/or PTBA terminal boards. The <R1> core receives the high pressure shaft speed inputs. The pulse rate input circuits on <R2> and <R3> may be used for other signals.

TCQA 4–20 mA Input Circuits

The TCQA board provides the circuitry for the 4–20 mA and 0–1 mA input signals. The signals are read from the TBQC terminal board via the JB connector. The transducer current is dropped across a burden resistor and the voltage drop is read by the TCQA board and written to the I/O Engine via the 3PL connector. Hardware jumpers on the TBQC terminal board are used to select the current range of the input signals.

TCQA 4–20 mA Output Circuit

The TCQA board provides the circuitry for driving 4–20 mA outputs to the TBQC terminal board via the JB connector. These signals are typically used to drive control devices.

TCQA Thermocouple Circuit

Thermocouples are connected to the TBQA terminal board. Circuits also located on the TBQA terminal board provide the thermocouple cold junction reference, which are used by TCQA to calculate the cold junction compensation. The TCQA board uses the thermocouple input and compensation value to calculate the actual temperature read by the thermocouple. The I/O Engine reads the value via the 3PL connector. Thermocouple types and curves are selected using I/O configuration constants.

TCQA LVDT/R Circuit

Linear Variable Differential Transformers (LVDT) or Linear Variable Differential Reactors (LVDR) are used to detect the position of actuators. The position signals are read from the TBQC terminal board via the JF connector. The scaled and conditioned signals are used by the Control Sequence Program (CSP). The excitation signals for the LVDT/R's are written to the QTBA terminal board via the TCQC board. The LVDT/R's are typically used for regulating servo valve outputs.

TCQA Seismic Vibration Circuit

The seismic vibration sensors are terminated on the TBQB terminal board in <R2> and <R3> and read by the TCQA board of the <R1> and <R3> cores respectively. The signals are scaled and conditioned and written to the Control Engine to be used by the CSP for monitoring and protection. Scaling values are selected in the I/O Configurator on the operator interface.

TCQA Generator And Line Circuit

In the <R1> core , the generator and line feedback signals from the Turbine Trip Board (TCTG) pass to the TCQC board through the TCQA board via JD and JE connectors .

DS200TCQC – Analog IO Expander Board

The Analog IO Expander board (TCQC) provides scaling and conditioning for additional analog signals read from the terminal boards of the I/O cores. The TCQC board provides LVDT and LVDR excitation. The IONET termination for <Q11> and <P1> is on the TCQC board in the <R1> core. If the optional <21> is installed, that IONET termination is on the TCQC in <R2>. The mA input for the megawatt transducer signal is scaled and conditioned on the TCQC board and written to the STCA board via the 19PL connector. Pulse rate inputs are scaled and conditioned on the TCQC board. In most applications, the high pressure shaft speed signals and occasionally the liquid fuel flow signals are scaled on the TCQC board and written to the TCQA board via the JE connector in the <R1> core. The TCQC board communicates the generator and line signals with the STCA board via the JE connector.

TCQC Connectors

2PL – Distributes power from the TCPS board in the <R1>, <R2> and <R3> cores.

8PL – I/O connector to the STCA boards in cores <R1>, <R2>, and <R3>. Signals include the COM1 RS232 output signals, the serial I/O signals, the acand DC power monitoring signals (TCPD), and a pulse rate magnetic pick up signal.

19PL – I/O connector to the STCA board. The I/O signals may include the megawatt, generator, bus, compressor stall detection signals, and the magnetic pick up pulse rate signals from the high pressure shaft. Power bus and neutral bus signals may also be carried in this connector (TCPS). Cores <R2> and <R3> may use the 19PL connector for other signals.

JC – Connected to the power supply board TCPS whose signals pass through the TCQC board to the TCQA board via the JE connector and to the STCA board via the 19PL connector.

JE – Writes the power supply monitoring signals to the TCQA board and reads the servo valve outputs and generator and line signals from the TCQA board.

JFF – Writes the servo outputs to the QTBA terminal board.

JGG – Writes the servo outputs and the 15 amp signals, reads magnetic pick up and megawatt transducer signals to/from the QTBA terminal board.

JH – Reads the pulse rate signal and compressor stall signals from the TBQB terminal board.

JJ – Reads the speed signals from the TCQE board in the <R1> core which originated on the PTBA terminal board in the <P1> core.

JX – Connector that terminates the IONET signal from TCEA board in the <P1> core. Used only in the <R1> core.

1PL – Typically not used.

6PL – Typically not used.

17PL – Typically not used.

VARC – Typically not used.

JBU – Typically not used.

ARCPL – Typically not used.

CARC – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCQC Configuration

Hardware. The first 16 hardware jumpers on the TCQC board configure the output current range for the servo outputs. The even numbered jumpers select the feedback scaling, while the odd numbered jumpers select the source output resistance. Hardware jumpers 25 through 36 are for added feedback scaling options for servos one through four, giving them a maximum current range of +/- 240 mA. BJ17 sets the RS232 port for card tests. BJ21 is the stall timer enable. BJ22 is the oscillator enable for factory test. BJ23 and BJ24 are not used. BJ18 and BJ20 limit the P15 and N15 supply to the proximity transducers. Hardware jumpers JP38 and JP39 set the magnetic pick up gain for liquid fuel flow signals in some applications. Refer to Appendix A and the paragraphs below for information on the hardware jumper settings for this board.

Software. There is no software configuration for the TCQC board.

TCQC Servo Valve Regulator Output Circuits

Current from the TCQA board is scaled by the TCQC board jumpers and sent to position the servo valves. Hardware jumpers on the TCQC board are used to configure the reference feedback and output current range. The TCQC board contains the servo clamp relay and the suicide relays. Energizing the suicide relays drives the signal to ground by passing the servo valves. This allows the servo valve to drift to the bias position. Energizing the servo clamp relays applies a positive current to the servo valve. A signal from the CSP that is written to the TCQA board and then sent to the TCQC board will energize the suicide relays. An emergency signal that is written directly to the TCQC board via the TCEA board will energize the servo clamp relays.

TCQC Pulse Rate Input Circuit

The high pressure shaft pulse rate signals are read from the TCQE board via the JJ connector. The TCQE board signals originate on the PTBA board in the <P1> core. The high pressure shaft signals are written to the TCQA board via the JE connector to be scaled and conditioned and then are written to the STCA board via 3PL. The pulse rate inputs from both the magnetic speed sensors and the TTL type sensors that are landed on the TBQB terminal board pass through the TCQC board via the JH connector. Additional magnetic pick up pulse rate signals are available on the QTBA board and are read by the JGG connector. Some of the signals landed on the PTBA terminal board could be landed on the QTBA terminal board and should not be used on both. The corresponding screws on the QTBA terminal board are not available if the signals are also landed on the PTBA terminal board.

TCQC Generator And Line Feedback

The signals for generator and line feedback pass through the TCQC board where they are scaled and conditioned prior to being written to the STCA board via the 19PL connector. These signals originate on the TCTG board in the <P1> core, pass through the TCQA board and are written to the TCQC board via the JE connector. The STCA board uses these signals for the synch check function.

TCQC IONET Circuit

The termination of the IONET for the <R1> core is on the TCQC board in <R1>. The signals from the TCDA board in the <Q11> core and the <X>, <Y>, and <Z> boards in the <P1> core are daisy chained on the IONET via the JX connector. These signals are written directly to the STCA board via the 8PL connector.

TCQC LVDT/LVDR Excitation Circuit

The TCQC board excites the LVDT/R's via the QTBA terminal board over the JFF connector at 3.2 Khz and 7 V rms.

TCQC 4–20 mA Input Circuits

The TCQC board provides the circuitry for two mA input signals. The first mA input signal is read from the TBQB terminal board via the JH connector. This signal is typically the compressor stall detection signal. The second mA input signal is read from the QTBA terminal board via the JGG connector. This signal is typically the megawatt transducer signal. These signals are written to the STCA board over the 19PL connector.

DS200TCQE – LM 6000 IO Processor

The LM 6000 IO Processor Board (TCQE) scales and conditions additional analog I/O signals and is located in the <R1> core. These signals include LVDT/LVDR inputs, 4–20 mA outputs, LM vibration inputs, proximitor vibration inputs, proximitor position inputs, RTD inputs, and magnetic pick up and TTL pulse rate inputs. The 3PL connector communicates the data from the TCQE board to the STCA board. This board is used for all LM applications.

TCQE Connectors

2PL – Distributes power from the TCPS board in the <R1> core.

3PL – The Data Bus between STCA, TCQA, and TCQE boards in core <R1>. Conditioned signals are carried on 3PL for transferring to the COREBUS.

JJ – Connector for writing the high pressure shaft speed signals to the TCQC board.

JJQ – Connector that reads the high and low pressure shaft speed signals from the PTBA terminal board in the <P1> core.

JLL – Reads the LVDT/R inputs and the RTD inputs from the TBQE board. Writes the 4–20 mA outputs to the TBQE board.

JO – Relay control signals used for the Load Coupling Shear and LP Shaft Shear protection are written to the TCRA board in location four of the <Q11> core for solenoids connected to the DTBC board.

JQQ – Reads the LM vibration inputs, proximitor vibration inputs and pulse rate speed sensor inputs from the TBQE terminal board.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCQE Configuration

Hardware. Hardware jumpers JP1 and JP3 are the oscillator enables for factory test. JP8 is for the stall timer. JP2 is the RS232 port enable for factory test. JP4 and JP6 configure the mA outputs. Hardware jumpers JP5 and JP7 are used to select the mA outputs current range, either 20 mA maximum or 200 mA maximum. Refer to Appendix A for information on the hardware jumper settings for this board.

Software. I/O Configuration constants for the RTDs, pulse rates, 4–20/200 mA outputs, proximitor, vibration, accelerometer, and the LVDT/LVDR positions are entered in the I/O Configuration Editor located on the operator interface as described below.

TCQE LVDT/LVDR Circuit

Linear Variable Differential Transformers (LVDT) or Linear Variable Differential Reactors (LVDR) are used to detect position. The position signals are read from the TBQE terminal board via the JLL connector. These position signals are scaled and conditioned signals for use by the Control Sequence Program, (CSP). The TCQE also performs diagnostics on these signals. The excitation signals for the LVDT/R's are written to the QTBA terminal board via the TCQC board. The LVDT/R's are typically used for regulating servo valve outputs; however these are not associated with the TCQA/TCQC servo systems..

TCQE 4–20 mA Output Circuit

The TCQE board provides the circuitry for driving two selectable 4–20 mA/20-200 mA outputs to the TBQE terminal board via the JLL connector. Diagnostics for these signals are done on the TCQE board. These signals are typically used for control devices. Hardware jumpers are used to select the maximum current output.

TCQE LM Vibration Inputs

The LM vibration inputs are read from the TBQE terminal board via the JQQ connector. The signals are scaled, conditioned and processed using the I/O configuration constants downloaded from the operator interface. The results are written to the STCA board via the 3PL connector.

TCQE Proximitor Vibration Inputs

The proximitor vibration inputs are read from the TBQE terminal board via the JQQ connector. The signals are scaled, conditioned and processed using the I/O configuration constants downloaded from the operator interface. The results are written to the STCA board via the 3PL connector.

TCQE RTD Circuit

The circuitry that supplies excitation to the RTDs from the TBQE terminal board is located on the TCQE board. A steady current is sent through the RTD and when the temperature changes, the resistance changes causing the voltage on the RTD to change. The TCQE board measures, scales, and conditions the voltage signal. The RTD signals are read from the TBQE terminal board by the TCQE board over the JLL connector. The TCQE board sends the signals to the I/O Engine via the 3PL connector. The type of RTD is selected using I/O configuration constants. These inputs are typically used for the LP and HP compressor input temperatures since they can be set up as high precision, (200 Ohm), RTDs in the I/O Configuration Editor on the operator interface.

TCQE Pulse Rate Circuit

The magnetic pick up signals for the low pressure shaft/power turbine speeds are read from the PTBA terminal board via the JJQ connector. Two TTL pulse rate input type speed sensor signals are read from the TBQE terminal board via the JLL connector. These signals are used for LP Shaft Shear protection applications. These signals are typically used for the LP compressor eddy current speed inputs. Two magnetic pick up speed sensors are read from the PTBA terminal board via the JJQ connector and are used for both the Load Coupling Shear and LP Shaft Shear protection applications.

TCQE LP Shaft Shear Circuit

The TCQE board provides application specific LP shaft shear protection. Special TTL type and magnetic pick up pulse rate signals are read from the TBQE and PTBA terminal boards via the JLL and JJQ connectors respectively. The two eddy current sensors are mounted on the LP compressor and the two magnetic pick up sensors are mounted on the LP turbine for monitoring the LP shaft speed. If the ends of the shaft are detected to be running at different speeds, a high speed circuit is used to evacuate the gas from the manifold. This is to protect the unit in case the shaft shears.

TCQE Load Coupling Shear Circuit

The TCQE board provides application specific Low Pressure Shaft Shear protection. The magnetic pick up signals read from the PTBA terminal board via the JJQ connector are compared to the TTL signals to determine if the shaft connecting the LP turbine and LP compressor has sheared. It the difference between these two speeds varies by more that an configurable constant, the gas manifold blow-off valve will be opened to evacuate gas fuel from the engine.

DS200TCRA – Relay Output Board

The Relay Output Board (TCRA), located in the digital cores, contains up to 30 relays, K1 through K30. There are two of these boards in the each digital IO core. The TCRA board in location four of the <Q11> core contains only four relays, which are connected to the TCQE via the JO connector. These relays are used to operate the gas manifold blow off valves in some applications. All other TCRAs contain a full complement of 30 relays. The first 18 relays on TCRA in location four of <Q51> can be configured to provide a power source to operate solenoids. The first 16 of these relays on the TCRA board in location five of both the <Q11> and <Q51> core can be configured this way also. This is done using hardware jumpers on the DTBC and DTBD terminal boards. Two additional contact outputs, (#47 and #48), can be wetted on the TCRA board in location five of either <Q11> or <Q51> using the power connectors J19 and J20. Connectors J19 and J20 bring 120/240 V ac power from the <PD> core to the DTBD board in one of the cores. These signals are typically used for ignition transformers. The signals to open or close the relays are written to the TCRA boards by the TCDA boards in the digital cores. The signals for the TCRA board in location four of <Q11> are from the TCQE board in the <R1> core. The first 18 solenoid outputs in <Q21> cannot be set up as solenoid power sources.

TCRA Connectors

JO – Writes the signals from the TCDA board to the TCRA board in location five for <Q11>, <Q21> and <Q51>. Writes the signals from the TCDA board to the TCRA board in location four of the <Q21> and <Q51> core. Writes the signals from the TCQE board in the <R1> core to the TCRA board in location four for the <Q11> core to control the gas manifold blow-off valve control.

JS1 – Connects relay outputs from TCRA to DTBC/D terminal board.

JS2 – Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS3 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS4 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS5 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS6 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS7 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JS8 -- Connects relay outputs from TCRA to DTBC/D terminal board. TCRA not connected to DTBC in <Q11>.

JOR/S/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCRA Configuration

Hardware. The hardware configuration that powers the relays, or changes them to solenoids, is done at the terminal board level on the DTBC and DTBD terminal boards.

Software. There is no software configuration done on the TCRA board.

TCRA Contact Output Circuits

The relays on the TCRA boards are operated by signals from the CSP and sent to the STCA board over COREBUS to the IO Engines. The STCA boards read the signals and send them to the TCDA boards via the IONET. The TCDA board then writes the command signals to energize the relays via the JO connector. The relay (open/close) is connected to the DTBC and DTBD terminal boards via the JS1 through JS8 connectors.

DS200TCSA – Fuel Skid Interface Board

The Fuel Skid Interface Board (TCSA), located in <R> core, interfaces with the XDSA board on the fuel skid for Dry Low Emissions (DLE) applications. The TCSA board decodes the signals from the high-resolution pressure transducers for the 196 processor on the UCIB board. The signals from XDSA are connected to the TBSA terminal board in position eight of the <R2> core. They are read by the TCSA board via the P3 connector.

TCSA Connectors

2PL – Power from the TCPS board in <R>.

GND – Chassis ground to the 1TB terminal board in <R>.

P3 – Provides 12 V dc power to TBSA and receives pressure signals from TBSA, which interfaces to the XDSA board on the fuel skid.

P4 – Provides 12 V dc power to TBSA, which interfaces to the FMVED motor controller(s).

SER – Writes decoded pressure transducer signals to the UCIB board.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCSA Configuration

There are no hardware jumper or software configurations for the TCSA board.

TCSA Pressure Transducer Interface

The TCSA board signals are read from the pressure transducers by the XDSA board on the fuel skid. The signals from the XDSA board are sent to the TBSA terminal board, which transfers them to the TCSA board over the P3 connector. The TCSA board decodes the RS422 protocol signals and writes them to the UCIB board for processing by the 196 processor. The TCSA board also provides the power for the pressure transducers and FMVED motor controllers.

DS200TCTG – Turbine Trip Board

The Turbine Trip Board (TCTG), in location four of the <P1> core, is used to operate fuel shutoff valves for the turbine. Two types of trip relays are available on the TCTG board for failsafe fuel valve operation. There are primary trip relays (PTRs) and emergency trip relays (ETRs). Communication faults and the CSP operate the PTRs. The TCEA boards in the <P1> core operate the ETRs, which conduct a 2/3 vote for an emergency trip. Hardwire trip pushbuttons will de-energize the 24 V dc supply to both the PTR and ETR relays and initiate a trip. The synchronizing relays are also located on the TCTG board.

TCTG Connectors

J7W – Distributes the 125 V dc power from the TCPD board in the <PD> core.

JDR – Reads the PTR trip signals from the TCQA board in the <R1> core, relays K10, 13, 16, and 19. Reads synchronize commands from the TCQA board in the <R1> core. Reads the generator and bus signals from the PTBA board . JDR, JDS and JDT are all daisy chain connected on the TCTG board.

JDS – Reads the PTR trip signals from the TCQA board in the <R1> core, relays K11, 14, 17, and 20. Reads synchronize commands from the TCQA board in the <R1> core. Reads the generator and bus signals from the PTBA board . JDR, JDS and JDT are all daisy chain connected on the TCTG board.

JDT – Reads the PTR trip signals from the TCQA board in the <R1> core, relays K12, 15, 18, and 21. Reads synchronize commands from the TCQA board in the <R1> core. Reads the generator and bus signals from the PTBA board . JDR, JDS and JDT are all daisy chain connected on the TCTG board.

JLX – Reads the ETR trip signals from <X> in the <P1> core. ETR relays K5 and K8 are fed by the JLX connector. Supplies the 24 V dc protective bus.

JLY – Reads the ETR trip signals from <Y> of the <P1> core. ETR relays K4 and K7 are fed by the JLY connector. Supplies the 24 V dc protective bus.

JLZ – Reads the ETR trip signals from <Z> of the <P1> core. ETR relays K6 and K9 are fed by the JLZ connector. Supplies the 24 V dc protective bus.

JN – Reads and writes signals to the PTBA terminal board in the <P1> core. These signals include the breaker close signal, hardwire trip signals, and the alarm horn signal.

JM – Reads and writes signals to the PTBA terminal board in the <P1> core. These signals include the breaker close signal and the emergency trip signals.

JT – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

TCTG Configuration

Hardware. There is one hardware jumper on the TCTG board. J1 is the Emergency Overspeed servo Clamp Enable jumper for servo valves one through four. This jumper is used to apply 24 V dc to the servo outputs. The actual relay is located on the TCQC board. Refer to Appendix A for information on the hardware jumper setting for this board.

Software. There is no software configuration done on the TCTG board.

TCTG ETR Relay Circuit

The TCEA boards <X>, <Y> and <Z> in the <P1> core generate the trip signals for the ETR relays. The signals are written to the TCTG board via the JLX/Y/Z connectors. The ETR relays perform a hardware level two out of three vote to determine if the unit should be tripped. If two out of three relays call for a trip, by opening and closing a series of related contacts on the TCTG board, the unit will trip. Signals that will trip the ETR relays are high pressure shaft overspeed and rapid deceleration, low pressure shaft overspeed and rapid deceleration and cross trip. The trip signals are then written to the PTBA terminal board via the JM connector.

TCTG PTR Relay Circuit

The trip signals for the PTR relays are driven by the TCQA board based on data generated by the control sequence program (CSP) and are site specific. The site specific CSP generates a trip signal that is written to the I/O Engine in the <R1> core via the COREBUS. The STCA board in the <R1> core then writes the trip signals across the 3PL connector to the TCQA board, which writes the trip signals to the TCTG board in the <P1> core via the JD connector. The PTR relays will also perform a two out of three hardware level vote prior to tripping the unit, even though the same signal was written to all three relays via the <R1> core. Once a PTR trip has been initiated, the CSP generates a cross trip that trips the ETR relays.

TCTG Generator Breaker Close Circuit

The signals to close the generator breaker originate on the STCA board in <R1> and in the TCEA boards in the <P1> core. The TCEA boards use the PT signals from the PTBA terminal board to perform the automatic synchronize calculations and to send the permissive signal to close the breaker. At the same time, the STCA board in the <R1> core performs a synchronizing permissive (synch check) calculation and also sends a permissive to close the breaker. The automatic synchronize signals are two out of three voted on the TCTG board. If two out of three automatic synch signals and the synch check signal has been given by <R1>, then the TCTG board gives the permissive to close the breaker. The K1, K2 and K3 relays will send the breaker close signal to the PTBA board via the JN and JM connectors.

TCTG Manual And External Trip Circuit

Normally closed contact inputs can be hardwired into the PTBA terminal board to initiate a trip when the contacts are opened. Emergency stop buttons are an example of this. These signals are read by the JN connector and written to the TCTG board, where they trip the K22, 23, 24 and 25 relays. These relays are refereed to as the "4's" in reference to an ANSI standard device number for the Master Protective. When the "4's" are tripped, they de-energize the 24 V dc protective bus used by the PTR and ETR relays causing them to initiate a trip. The TCEA board typically monitors the hardwire trip signals 1 through 3 for an emergency stop and will record their event back to the Control Engine.

DS200UCIB – <R> Core Mother Board

The <R> Core Mother Board (UCIB) provides the connectors for mounting the host CPU daughterboard (LBC586P), two µGENI boards, and a flash disk. The UCIB board uses a 196 microprocessor to translate the DLE gas fuel pressures from the TCSA board. These signals are written to the LBC586P board via the J1 and J3 bus connectors. The COREBUS and Stage Link signals written to the PANA board are passed to the LBC586P via the J1 and J3 bus connectors.

UCIB Connectors

2PL(P2) – Distributes power from the TCPS board.

2PLX (P7) – Distributes power from the TCPS board and is daisy chained to the TCSA board.

FAN (P14) – Power connections for the fan used to cool the CPU mounted on the LBC-586 board. Typically not used.

GEN1 (P5) – Serial port connection to the 1TB terminal board for the Genius inputs X1-1, X2-1 and shield.

GEN2 (P6) – Serial port connection to the 1TB terminal board for the Genius inputs X1-2, X2-2, and shield. Typically not used.

J1 – Bus connector that communicates with the LBC-586 and PANA boards.

J2 – Connector for IDE flash drive.

J3 – Bus connector that communicates with the LBC-586 and PANA boards.

J4 – Routes IDE disk signals between the LBC-586 and UCIB boards.

P5 – Serial connection for Genius signals from UCIA board to the µGENI daughter-board.

P6 – Serial connection for Genius signals from UCIA board to the second µGENI daughterboard. Typically not used.

P15 – Power connection for the µGENI board.

P16 – Power connection for the µGENI board.

SER (P1) – Serial connection that reads the signals from the TCSA board.

P8 – Power connector for LBC-586 board.

P9 – Power for floppy disk for use by GE Field Engineers.

P10 – COM1 port connection.

P11 – COM2 port connection.

P12 – Keyboard connection for use by GE Field Engineers.

P13 – Routes COM and keyboard signals between LBC-586 and UCIB boards.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

UCIB Configuration

Hardware. Hardware jumper JP1 is the clock enable. Refer to Appendix A and the hardware jumper screen on the operator interface for information on the hardware jumper settings for this board.

Software. There is no software configuration for the UCIB board.

UCIB Pressure Transducer Interface Circuit

The high-resolution pressure transducer signals from the XDSA board are landed on the TBSA terminal board in <R2> core. The P3 connector on the TCSA board receives the signals, which the TCSA board decodes for use by the 196 processor on the UCIB board. The signals are written to the LBC586P board via the J1 and J3 connectors.

UCIB Genius I/O Circuit

A μGENI board can be mounted on the UCIB board. A μGENI board controls certain types of data transfer between the host (Mark V LM) and Genius bus. The Genius bus connections are made on the 1TB terminal board on the <R> core. The signals are passed by the μGENI board through the serial connector P3 on the UCIB board and written to the LBC586P board via the P5 connector. The μUCIB board, through the P15 connector, powers the μGENI board.

DS200UCPB – IO Engine CPU Board

The IO Engine CPU board (UCPB) is the daughterboard mounted on STCA in the IO Engines. The UCPB board contains an 80486DX processor (CPU), a single inline memory module (SIMM) socket with dynamic random access memory (DRAM), flash erasable programmable read-only memory (EPROM) with ROM BIOS, I/O mapped flash EPROM, two RS-232 serial ports, and an ARCNET driver. One UCPB is installed in each of the IO Engines: <R1>, <R2>, <R3> and <R5>. A PCM daughterboard is installed on the UCPB in <R2> for serial communication with FMVED motor controllers.

The UCPB processor packages the analog and digital IO information and broadcasts it on the COREBUS. The packets are broadcast according to a task schedule. Packets are sets of information grouped according to need and then transmitted for use by other devices. Critical information is broadcast in a “fast packet” at 100 Hz or every 10 ms, while less critical information is broadcast in “slow packets”, which are broadcast at a slower rate than 100 Hz.

When an IO core is rebooted, the IO Engine reads the IO Configuration information from the IOCFG.AP1 file in Control Engine flash and loads it into the DRAM. The IO Configuration is then written across the IONET to the digital IO boards and across the 3PL to the analog IO boards. The TCEA cards must also be rebooted for them to receive their latest .

UCPB Connectors

ARCNET – COREBUS connection that links the I/O cores to the <R> core via the STCA board mounted on each I/O core.

COM1 – Terminal Interface Monitor (TIMN) connection via the STCA board mounted on each I/O core. Allows for external monitoring of data specific to each I/O core. RS232 interface signal connection to the STCA board.

COM2 – Typically not used.

J1 – Bus connection to the STCA board.

J3 – Bus connection to the STCA board.

IDE – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D contain more information.

UCPB Configuration

Hardware. There are three hardware jumpers located on the UCPB board. JP1 and JP3 are used for factory test. JP2 selects the 486 local bus speed. Initiating a hard re-boot by using the power on/off switch for the specific IO core located in the <PD> core is the recommended method for rebooting. The DIP switches are used to set the COREBUS address for a given IO Engine. Refer to Appendix A for information on the hardware jumper settings for this board. The hardware jumpers on the PCM need to be configured as described in the FMVED commissioning guide only if serial communication with a GE Industrial Systems motor controller is required.

Software. The software product for the IO Engine is called TMIA and contains the IO configuration data for the FMVED serial download software, WATT/VAR input and three pulse rate inputs

LBC586P – WinSystems CPU Board

The CPU board (LBC586P) is the central processing unit daughterboard for the control engine. The LBC586P board contains an AMD 586 processor (CPU), a single inline memory module (SIMM) socket with dynamic random access memory (DRAM), flash erasable programmable read-only memory (EPROM) with ROM BIOS, two RS-232 serial ports, and video and keyboard drivers.

In the <R> core, the LBC586P board is mounted on the UCIB motherboard. Data is read in via the J1 and J3 bus connectors to the 586 CPU. The CPU is used to convert fixed point data to floating point for use with the QNX software (Operating System), process the control sequence program (CSP), and to read and write data back to the PANA board for the COREBUS and Stage Link. The Operating System and Mark V LM product software are stored on a flash IDE device mounted on the UCIB.

I/O signals read from the COREBUS are converted from fixed point to floating point values and written to their reserved memory addresses. The Control Signal Database (CSDB), Mark V LM memory locations where all of the control signal values are stored, including the I/O signals, is located on the DRAM of the LBC586P board. The 586 CPU for calculations accesses these signals. Output signals are taken from the CSDB and converted back to fixed point from floating point prior to being written to the COREBUS. The operator interface receives information from the Control Engine via the Stage Link. These values are presented to the user on the operator interface screen, in a report, or sent to another medium.

The CSP, I/O configuration, and Mark V LM table files (instruction files for the controller to save certain signals in reserved memory), are downloaded to the flash IDE device from the operator interface. The CSP and table files are transferred into DRAM when the <R> core is rebooted. The 586 CPU calls the CSP and associated Big Blocks, (hard coded subroutines), from RAM as they are used. Table files reserve memory locations for selected control signals to reside. The CPU copies the signal values into the memory locations.

LBC586P Connectors

Many connectors on the LBC586P card are not used for the Mark V LM application. The following connections are made to the LBC-586 card:

J26 – Bus connector for processor interface to memory and IO on the UCIB and PANA.

J29 – Bus connector for processor interface to memory and IO on the UCIB and PANA.

J18 – IDE interface connector. Ribbon cable connected to J4 on the UCIB.

J7 – Power cable. Connected to P8 on the UCIB.

J3 – Serial and other miscellaneous signals. Connected to P13 on the UCIB.

LBC586P Configuration

Hardware. There are no user customizable hardware jumpers located on the LBC-586 board. All jumpers are set at the factory to their proper positions. Initiate a processor reboot by using the power on/off switch for the <R> core located in the <PD> core.

Software. The software products for the Control Engine are called TMQB and TMCx (where x indicates the engine-specific product software). The configuration for the engine control is the CSP, table files and all of the functions described in Chapter 5.

Printed Wiring Terminal Boards

This section describes the printed wiring terminal boards used in the Mark V LM controller. The sample hardware document in Appendix B shows the locations and interconnection information for these boards.

DS200CTBA - Termination Module

The Analog Termination Module (CTBA) is located in the <R5> core. The CTBA terminal board has the 4–20 mA output, the 4–20 mA input, and the shaft voltage and shaft current connections. The IONET connection to the STCA board and the COREBUS connection to the QTBA board on <R1> are also located on the CTBA board. Mark V LM power source monitoring is connected to CTBA from the TCPD board in <PD>. A bypass relay allows COREBUS to communicate if power is lost to CTBA.

CTBA Connections

8PL – Carries the IONET signals to the STCA board in the <R5> core.

JAA – Carries the 4–20 mA outputs from the TCCA board in the <R5> core.

JAI – Used for the COREBUS connection, if not used then a termination resistor should be attached.

JAJ – Used for the COREBUS connection, if not used then a termination resistor should be attached.

JBB – Carries 4–20 mA inputs and the shaft voltage and current signals to the TCCA board in the <R5> core.

JEE – Communicates the COREBUS signals with the STCA board in the <R5> core.

JPD – Carries the 24 V dc power signal from the TCPD board in the <PD> core.

JX – Communicates the IONET signals with the TCDA board in the <Q51> core.

6PL – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

CTBA Hardware Configuration

BJ1 through BJ14 – Connects the NEG terminal of the respective mA input to DCOM.

BJ15 – Connects the RS232 Monitor Port (TIMN) to DCOM.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200DTBA – Contact Input Termination Module

The Contac Input Termination Module (DTBA) is located in <Q11>, <Q21> and <Q51>. DTBA connects the first 46 contact inputs to TCDA in the same digital core. The inputs can be configured to invert the contact sense in the TCDA IO Configuration to provide failsafe contact input functionality.

CTBA Connections

JQR – Connects the contact input to the TCDA board.

J12 – 125 V dc power connection from TCPD in <PD>.

JY – Connects 125 V dc power to the DTBB board.

JQS/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

CTBA Hardware Configuration

BJ1 through BJ5 – Isolates the contact inputs for test (from the 125 V dc).

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200DTBB – Contact Input Expansion Termination Module

The Contac Input Termination Module (DTBB) is located in <Q11>, <Q21> and <Q51>. DTBB connects the last 46 contact inputs to TCDA in the same digital core. The inputs can be configured to invert the contact sense in the TCDA IO Configuration to provide failsafe contact input functionality.

DTBB Connectors

JRR – Connects the contact inputs to the TCDA board.

JY – Receives 125 V dc power from the DTBA board.

JRS/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

DTBB Hardware Configuration

BJ1 through BJ5 – Isolates the contact inputs for test (from the 125 V dc).

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200DTBC – Contact Output Termination Module

The Contact Output Termination Module (DTBC) is located in <Q11>, <Q21> and <Q51>. DTBC is connected to the 30 relays on the TCRA in location four of <Q21> and <Q51>. Eighteen of the 30 outputs on DTBC in <Q51> can be configured as solenoids using hardware jumpers on DTBC. The DTBC in <Q11> is connected to the four contact output relays on the TCRA in location for of <Q11>. The hardware jumpers on the <Q11> DTBC are specially configured for gas manifold blow-off valve control.

DTBC Connectors

JS1 through JS8 – Reads the relay signals from the TCRA board in location four.

J8 – Receives the power for the solenoids from the TCPD board in the <PD> core.

J15 – Connects to J16 to carry 125 V dc power for contact outputs #16, #17, and #18. Not typically used on the <Q11> core.

J16 – Connects to J15 to carry 125 V dc power for contact outputs #16, #17, and #18. Can only be connected in the <Q51> core. Not typically used on the <Q11> core.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

DTBC Hardware Configuration

P1/M1 through P18/M18 – Solenoid enable for contact outputs #1 through #18 respectively. Both must be in to enable the solenoid power, or both out to disable it. The configuration of the <Q11> DTBC for gas manifold blow-off valve control does not follow this convention, refer to Appendix D for the proper configuration of that terminal board

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200DTBD – Contact Output Expansion Termination Module

The Contact Output Expansion Termination Module (DTBD) is located in <Q11>, <Q21> and <Q51>. DTBD is connected to the 30 relays on the TCRA in location five of <Q11>, <Q21> and <Q51>. Sixteen of the 30 outputs on DTBD in location four of <Q21> and <Q51> can be configured as solenoids using hardware jumpers on DTBD. Two other contact outputs (#47 and #48) can be used for ignition transformers if J19 and J20 are connected and the factory-installed wire jumpers are removed.

DTBD Connectors

JS1 through JS8 – Reads the relay signals from the TCRA board in location five.

J8 – Receives the power for the solenoids from the TCPD board in the <PD> core.

J19 – Connects to J20 to carry 125 V dc power for contact outputs #47 and #48. Connected in <Q11> and <Q51>, not connected in <Q21>.

J20 – Connects to J19 to carry 125 V dc power for contact outputs #47 and #48. Connected in <Q11> and <Q51>, not connected in <Q21>.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

DTBD Hardware Configuration

P1/M1 through P16/M16 – Solenoid enable for contact outputs #31 through #46 respectively. Must be both in or both out.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200PTBA – Protection Termination Module

The Protection Termination Module (PTBA), located in the <P1> core terminates the signals for the <P1> core. Input signals for the high and low pressure shaft speeds, flame detection, generator and bus voltages and generator currents are landed on the PTBA terminal board and connected to the TCEB board in <P1>. The speed signals are also connected to the <R1> core. The external trip input signals, generator and bus signals and generator breaker close signals are read by the PTBA terminal board and then written directly to the Turbine Trip (TCTG) board in the <P1> core. Trip output signals and generator breaker close signals from the TCTG board are written to the unit via the PTBA terminal board. The audible alarm (horn) located on the TCEB board is powered using a hardware jumper on the PTBA board.

PTBA Connectors

JJR – Writes the speed signals for the high and low pressure shafts to the TCQE board in the <R1> core.

JM – Reads and writes the generator breaker signals (52GL) and writes the emergency trip outputs to/from the TCTG board in the <P1> core.

JN – Reads and writes the generator breaker signals (G125P), writes the enable signal to the horn, and reads the external trip signals to/from the TCTG board in the <P1> core.

JU – Writes the emergency overspeed signals, the flame detect signals, and the audible alarm (horn) enable signals to the TCEB board in the <P1> core.

JV – Writes the generator and bus voltage signals and the current signals (PT and CT) to the TCEB board in the <P1> core.

JVA – Carries the 335 V dc out to the flame detection devices from the TCEB board in the <P1> core.

JJS/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

PTBA Hardware Configuration

J1 – Audible alarm (horn) enable. Remove to silence.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200QTBA – Termination Module

The Termination Module (QTBA) is located in location six of the <R1>, <R2> and <R3> cores. The QTBA terminal board lands the signals used by the TCQC board in the respective cores. The COREBUS connections are also on the QTBA terminal boards. The inputs for pulse rates and megawatt transducers are connected on the QTBA terminal board and written to the TCQC board. The LVDT/R excitation and servo valve outputs are also connected to the QTBA terminal board from the TCQC board. The Terminal Interface Monitor (TIMN) connections are also located on the QTBA terminal board. A bypass relay that allows the COREBUS to continue to communicate if power is lost on the QTBA terminal board is located on the QTBA terminal board.

Notes As there is no voting being performed for the I/O inputs and outputs, redundant signals would not be used. Signals for the same inputs and outputs would only be used in one of the three locations, <R1>, <R2>, or <R3>.

QTBA Connections

JAI – COREBUS connection. If not used a termination resistor should be installed.

JAJ – COREBUS connection. If not used a termination resistor should be installed.

JEE – Communicates the I/O signals with the respective STCA board for use by the COREBUS.

JGG – Writes the mA input signals, pulse rate input signals and megawatt transducer signals and reads the servo valve output signals to/from the TCQC board in the respective core.

JFF – Writes the LVDT/R excitation signals and servo output signals to the TCQC board in the respective core.

JRS – Reads the RS232 monitor signals.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

QTBA Hardware Configuration

J1 – Selects the mA input signal currant range, either 0–1 mA or 4–20 mA.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200TBCA – Termination Module RTD Inputs

The RTD Termination Module (TBCA) is in location nine of the <R5> core. The RTD connections to <R5> are landed on the TBCA terminal board, which is connected to the TCCA board in <R5>.

TBCA Connections

JCC – Writes the RTD signals #1 through #15 to the TCCA board in the <R5> core.

JDD – Writes the RTD signals #16 through #30 to the TCCA board in the <R5> core.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBCA Hardware Configuration

There are no hardware jumpers on the TBCA terminal board.

DS200TBCB – Termination Module RTD and 4 – 20 mA Input

The Termination Module RTD and 4–20 mA Input (TBCB) is in location seven of the <R5> core. RTD and mA input signals are landed on the TBCB terminal board. Eight of the 4 -20 mA input signals have the option to be configured using hardware jumpers to be 0 -1 mA input signals. The signals connected to the TBCB terminal board are written to the TCCB board in the <R5> core.

TBCB Connections

JHH – Writes the mA input signals to the TCCB board in the <R5> core.

JII – Writes the RTD signals to the TCCB board in the <R5> core.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBCB Hardware Configuration

BJ1 through BJ22 – Connects the mA input signals #1 through #22 to DCOM.

BJ23 through BJ30 – Configures mA input signals #15 through #22 to either a 0 -1 mA or to a 4 -20 mA current range.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200TBQA – Thermocouple Termination Module

The Thermocouple Termination Module (TBQA) is located in the <R1> and <R5> cores. The TBQA terminal board can receive 45 thermocouple input signals. The TBQA in <R1>, distributes its input signals as follows: 15 signals (thermocouples #1 through #15) to TCQA in <R1>, 15 signals (thermocouples #16 through #30) to TCQA in <R2> core, and 15 signals (thermocouples #31 through #45) to TCQA in <R3>. The TBQA board in <R5> can receive 42 thermocouple input signals, which are all connected to the TCCA board in <R5>. The TBQA board also provides the cold junction compensation circuits.

TBQA Connections

JAR – From the <R1> core, writes thermocouple signals #1 through #15 and cold junction signal to the TCQA board in the <R1> core. From the <R5> core, writes the thermocouple signals #1 through #15 and the cold junction signal to the TCCA board in the <R5> core.

JAS – From the <R1> core, writes thermocouple signals #16 through #30 and cold junction signal to the TCQA board in the <R2> core. From the <R5> core, writes the thermocouple signals #16 through #30 and cold junction signal to the TCCA board in the <R5> core.

JAT – From the <R1> core, writes thermocouple signals #31 through #45 and cold junction signal to the TCQA board in the <R3> core. From the <R5> core, writes the thermocouple signals #31 through #42 and cold junction signal to the TCCA board in the <R5> core.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBQA Hardware Configuration

There are no hardware jumpers on the TBQA terminal board.

DS200TBQB – Input Termination Module

The Input Termination Module (TBQB) is in location seven of the <R2> and <R3> cores. The TBQB terminal board in the <R2> core is connected to the TCQA and TCQC boards in the <R1> core. The TBQB terminal board in the <R3> core is connected to the TCQA and TCQC boards in the <R3> core. The voltage, vibration and pulse rate input signals are landed on the TBQB terminal board.

TBQB Connections

JGR – Writes the vibration, and analog current and voltage signals to the TCQA board in the respective cores.

JHR – Writes the pulse rate input and compressor stall detection inputs to the TCQC board in the respective cores.

JGS/T – Typically not used.

JHS/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBQB Hardware Configuration

BJ1 through BJ4 – Used to fan out the pressure transducer #1 (compressor stall detection) input signal in old applications.

BJ5 through BJ7 – Used in connection with BJ1 through BJ4. Installs a burden resistor to the pressure transducer #1 input signal causing the signal to be a mA rather than voltage signal.

BJ8 through BJ15 – Configures analog inputs to be either current or voltage.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200TBQC – Analog Input, Milliamp Input/Output Termination Module

The Analog Input Termination Module (TBQC) is in location nine on the <R1>, <R2> and <R3> cores. TBQC connects the 4–20 mA inputs and the LVDT/R position inputs to the TCQA board in its respective core. The 20 - 200 mA outputs are read from the TCQA boards in the respective cores. The outputs can be configured to be either a 20 mA maximum current or a 200 mA maximum current using hardware jumpers on the TBQC terminal board.

TBQC Connections

JBR – Writes the 4 – 20 mA input signals and reads the mA output signals to/from the TCQA board in the respective cores.

JFR – Writes the LVDT/R position input signals to the TCQA board in the respective cores.

JBS/T – Typically not used.

JFS/T – Typically not used.

TEST. – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBQC Hardware Configuration

BJ1 through BJ15 – Connects the mA input signals #1 through #15 to DCOM.

BJ16 and BJ17 – Selects the maximum current output range for the mA outputs, either 20 mA or 200 mA maximum current for the two mA output signals.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200TBQE – LM6000 Analog Termination Module

The LM6000 Analog Termination Module (TBQE) is in location seven of the <R1> core. TBQE is used for all LM engine applications and contains all of the inputs and outputs used by the TCQE board in the <R1> core. The inputs read by the TBQE terminal board include the proximity transducer, accelerometer, LVDT/R position feedback inputs, RTD inputs, and the pulse rate signals for LP Shaft speed monitoring and shear protection applications. These signals are written to the TCQE board for processing. The 4 -20 mA outputs from the TCQE are written to the TBQE terminal board.

TBQE Connections

JLLR – Writes the LVDT/R position inputs, RTD inputs and pulse rate inputs to the TCQE board in the <R1> core. Reads the mA output signals from the TCQE board in the <R1> core.

JQQR – Writes the proximitor and vibration signals to the TCQE board in the <R1> core.

JLLS/T – Typically not used.

JQQS/T – Typically not used.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBQE Hardware Configuration

BJ1 and BJ2 – Selects the maximum current output range for the mA outputs, either 20 mA or 200 mA maximum current for the two mA output signals.

Refer to Appendix A for information on the hardware jumper settings for this board.

DS200TBSA – Serial Communication Termination Module

The TBSA terminal board is in location eight of <R2>. The pressure transducer signal wires from the externally-mounted XDSA board for DLE applications and the FMVED serial link wires are connected to this terminal board. The pressure transducer signals are connected to the TCSA board in <R>. The FMVED signals are connected to the PCM daughterboard on the IO Engine in <R2>.

TBSA Connections

P3 – Receives 12 V dc power from TCSA in <R> and connects it to DLE serial pressure transducers. This connection also links the pressure signals from the transducers back to the TCSA board in the <R> core.

P4 – Receives 12 V dc power from TCSA in <R> and connects it to FMVED motor controllers.

P5 – Connects FMVED communication channels 1 and 2 to P3 on the PCM daughterboard on the UCPB in <R2>.

P6 – Connects FMVED communication channels 3 and 4 to P6 on the PCM daughterboard on the UCPB in <R2>.

The hardware document in Appendix B and the signal flow diagrams in Appendix D have more specific information about connectors on this terminal board.

TBSA Hardware Configuration

JP1 through JP16 – These hardware jumpers enable the transmit and receive communication circuits for the FMVED motor controller serial links.

Refer to Appendix A for information on the hardware jumper settings for this board.

TB1

The TB1 terminal board located in the <PD> core lands the incoming 115/230 V ac and 125 V dc power to the Mark V LM controller. ac power is connected to the TCPD board in the <PD> core and routed through the JZ2 and JZ3 connectors for ac to dc conversion in the DACA module(s). dc power is usually from a 125 V dc uninterruptable power source (UPS/battery) and is connected directly to TCPD through the TB1 terminal board. The JZ5 connector provides power for the ignition. The JZ4 connector is used for the same purpose, but with the auxiliary ac signals.

TB2

The TB2 terminal board allows the excitation voltage for contact inputs (DTBA and DTBB terminal boards in the digital cores) to be 125 V dc from <PD> core or 24 V dc from <P> core. Implementation of the desired contact input excitation option is done at factory.

1TB

The 1TB terminal board located in the <R> core and receives Genius Global Data signals. It is connected to the GEN1 and GEN2 connections on the UCIB board in the <R> core.

Notes

Chapter 5 Control Engine

Controller Operation

This chapter is designed as a guide to the functions running in the Mark V LM Aeroderivative Turbine control systems. The Mark V LM is a specialized extension of the Mark V which meets the computation and frame rate specifications for Dry Low Emissions (DLE) aeroderivative gas turbines made by GE Marine and Industrial Engines in Cincinnati, OH. The Mark V LM allows GE Industrial Systems to compete in a market that is not supported by any other SPEEDTRONIC product.

Measurement and control devices are connected to the Mark V LM through terminal boards on the analog and digital IO cores and the protective core. In addition, serial data links are used for DLE gas fuel pressures and FMVED motor controllers. The Control Engine converts fixed point IO signals obtained from the COREBUS to floating point values for use in the application software. The Control Engine also converts the values back to fixed point for transfer back across the COREBUS to the IO cores. More information on the communication networks can be found in Chapter 1 of this manual.

This chapter is presented as follows:

Application Software Structure

The Mark V LM Control Engine stores application specific software, operating system and control constants and loads them into RAM when <R> is initialized. The processor runs the Control Sequence Program (CSP), which calls the Big Blocks and Control Constants from RAM as they are needed. The processor also controls access to the Control Signal Database (CSDB) and Linearization Database (LDB), which reside in special memory areas in <R>. These databases store values used by the CSP for engine control and monitoring and HMI for operator review and data logging. The CSP is assembled by the Control Sequence Editor, which can be used to create a new CSP or to edit an existing one. The Control Sequence Editor provides online help to the user and is explained in detail in the HMI documentation.

The CSP is built using Relay Ladder Logic and functional blocks (also called Big Blocks or BBLs) for specific control, monitoring, and protection of the unit. The CSP uses software signal names, for easy user identification of a parameter, which correspond to CSDB memory locations in <R>. These parameters are used for calculation, IO validation, control constants, and alarm monitoring. A *Fatal Sequencing Error* diagnostic alarm message indicates that the CSP revision documented in the MSTR_SEQ.CFG file does not agree with the product software revision in the Control Engine. MSTR_SEQ.CFG determines which segments to execute and their frequency.

This relay ladder logic based software structure defines data flow and function execution. The software structure is made up of a series of rungs with combinations of comments, contacts, coils, and Big Blocks. Big Blocks are software modules that perform standard control functions. There are three different types of Big Blocks: Primitive, Generic, and Application Specific.

- Primitive Blocks perform simple arithmetic, relational or switching operations. They are used with software relay contacts and coils, which control how they operate each time they are executed.
- Generic Blocks are usually more complex than primitive blocks and will operate the same way every time they are executed. These blocks are used extensively for IO validation and analog output control functions.
- Application Specific Blocks are usually more complex than generic blocks and will operate the same way every time they are executed. These blocks may also do IO validation and analog output control functions; however, they control highly complex operations for engine control and monitoring. Many of these blocks execute complex algorithms specified by the GEAE Control Specifications.

Similarities to the Mark V Controller

Mark V LM Unit Configuration software files are similar to those of the Mark V controller. These files are placed on a virtual drive named F:. Turbine Control Interface (TCI) software, which replaces the IDP software, is placed on a virtual drive named G:. These drives carry out functions equivalent to F: and G: on the Mark V <I>. The virtual F: contains the Unit Configuration software and its path is usually in the C:\SITE directory.

Mark V and Mark V LM Controller Differences

This is not intended to be an all-inclusive list of differences between Mark V and Mark V LM controllers. Some of the more significant differences between these two controllers are:

- Floating point processor eliminates the need for shifts in arithmetic functions
- Minor frame rate of 100 Hz
- Maximum of 32 sequencing segments
- Compilers create .AP1 files in place of .DAT files
- Separate linearization database (LDB) for analog linear interpolation data
- Data conversion for I/O engines (fixed point) to control engine (floating point)
- Rolling average function
- Peak detection function
- Format change to MODBUS.DAT to convert from floating point to fixed point
- New board library for automatic update of IO PROMset support files
- Table compiler functions BOI, EPA, MAOUT, and CHNG are not used

Control Engine Software Directory Structure

The Mark V LM Control Engine runs the QNX® real-time operating system and has its own directory structure. The QNX operating system is POSIX® compliant and requires UNIX®-style commands for navigation and file manipulation. The HMI is able to send and receive files from the Control Engine via the User Defined File (UDF) server. The portion of the Control Engine directory structure with the turbine control software is:

/unit	/config	Site-specific AP1 data files
	/product	Engine-specific executable code (LM25, LM16, LM6)
	/q	Control Engine operating code for all Mark V LM controllers
	/log	Control Engine start-up log files and Turbine trip log file

The unit/config directory is the target for AP1 files generated by the sequencing and table compilers, Controller Configuration tools and special-purpose files created by the TXT2AP1 command. Unless otherwise specified, all downloads described in this chapter will be to the Control Engine unit/config directory.

The unit/product directory contains BBL executable code and other software compiled with the baseline (engine-specific) database. The VXFR.AP1 and SOED.AP1 files reside in this directory, since they are only factory configurable.

The unit/q directory contains the Mark V LM code that supports communications and other functions that are neither database-dependent nor site-specific.

The unit/log directory contains the Mark V LM Control Engine start-up logs generated each time the control is rebooted. In addition, a TRIP.AP1 log file is written to this directory after a turbine trip. This file is not affected by Control Engine reboots, it is only overwritten when a turbine trip is detected.

Control Engine Cyclic Redundancy Check (CRC)

Mark V LM diagnostics exist to inform the user whether the product software downloaded to the control engine is correct and intact. After downloading a TMCx software product to the Mark V LM Control Engine, a reboot must be performed to begin execution of the new program. If a *Control Engine CRC Error* diagnostic alarm and *CE Files Corrupted* message appears in the Control Engine CRC data window in DIAGC, the product software download should be repeated. A CRC error is indicative of a missing or truncated file in the Control Engine product software download. The IO State of the Control Engine will not be able to go any higher than A4 until the problem listed in DIAGC for the Control Engine CRC data window is resolved.

Control Engine Functions

Cable Remote Function

The Cable Remote function allows contact inputs to write to a point defined as a Control Pushbutton (CPB) in the CSDB. This function precludes the need for added sequencing in the Control Sequence Program (CSP). The Cable Remote function is enabled only when the Control Mode Boolean L43CA is set TRUE. The Control Engine requires a reboot to enable Cable Remote changes, since changing this function constitutes a sequencing change.

Momentary and Maintained types of pushbuttons are supported. Momentary contact inputs, on a logic level transition from 0 to 1, will cause the associated CPB signal name to be set TRUE for 680 milliseconds. Maintained contact inputs, on a logic level transition from 0 to 1 will cause the associated CPB signal name to be TRUE until the same contact input transitions from 1 to 0.

The source file for this function is CBLR_Q.SRC, which is compiled by the TABLE_C program to create the CBLR.A1 file. CBLR_Q.SRC supports up to 16 inputs, with the following three download parameters required:

Contact Input	CPB Name	Type Code for Contact Input
(software signal name of input assigned in IO.ASG)	(LQPB software signal name assigned in a *.ASG file or UNITDATA.TPL)	(0= momentary contact, logic level set for fixed duration) (1=maintained contact, logic level set as long as pu*shbutton is held down*)

Diagnostic Alarm Masking Function

The Diagnostic Alarm Scanner looks for diagnostic alarms generated by the IO boards, IO Engines (IOE) and Control Engine (CE) without filtering. This function is designed to filter out diagnostic alarms that are inappropriate for a specific application or engine type. The file DIAG_MSK.TXT, which can be found in the F:\UNIT1 directory, contains a list of alarm drop numbers to be compiled into the DIAG_MSK.AP1 with the TXT2AP1 executable. After downloading DIAG_MSK.AP1 to the Control Engine via the UDF server, the Control Engine will implement the changed diagnostic alarm masks within two minutes. No Control Engine reboot is required to activate the new masks.

Event Logging Function

The Event Logging function allows Boolean values other than alarms to be recorded on the alarm printer, and on the CIMPLICITY alarm display when enabled. The events to be monitored are entered into the EVENT_Q.SRC file on the operator interface in a vertical list of up to 64 signal names. EVENT_Q.SRC is compiled by TABLE_C to create EVENT.AP1 for download the to the Control Engine. The Control Engine will implement the changed Event Logging within two minutes. No Control Engine reboot is required to activate the new events.

When a logic signal in EVENT_Q.SRC changes state to TRUE, the following will be printed on the Alarm and Event Logger:

- Date/time stamp
- String *EVENT*
- Software signal name
- String *TRUE* to indicate that the logic is set
- Written description of signal name from LONGNAME.DAT

When the same contact opens, *FALSE* will appear in place of the *TRUE* to indicate that the logic signal has been reset.

Dry Low Emissions (DLE) Gas Fuel Metering Valve Security

DLE technology enables a site to operate within certain clean air standards, without having to inject de-mineralized water or steam into the combustor. There are big cost savings for a customer who does not have to support de-mineralizers and boilers over the life of a power plant. DLE combustion is accomplished by precisely controlling the fuel to air ratio in the combustor. The simplest way to do this is through high-precision mapping of the effective area of each Fuel Metering Valve (FMV) associated with a DLE engine. An FMV map is contained in three separate data tables, with the tables tracked by the serial number assigned to the FMV.

The challenge in matching FMV to data tables is presented by the fact that requisition software and FMV(s) may not be joined until they get to a customer site. A specialized program in the TCI software called FMVID accomplishes this. This Feature is used to help verify that the FMVs have the matching Area (TFMVAR.LDB) and Pressure Correction (TFMVCRH.LDB and TFMVCRL.LDB) maps are loaded into the Mark V LM Control Engine.

➢ To properly install the DLE FMV Security function:

1. Determine the Whittaker FMV Part number and Serial number for the Valve(s) to be installed at the site from the Fuel Valve nameplate. A DLE engine will have either 1 mapped Fuel Valve for a Class A Fuel Metering System or 3 mapped Fuel Valves for the Class B Fuel Metering System.
2. Obtain Fuel Metering Valve maps for the valve(s). The data for each valve will be in a PKWARE 1.1 file with the name SN###LDB.ZIP and will contain the following three files:

TFMVAR.LDB	Nominal Pressure Area map
TFMVCRH.LDB	High Pressure Area Correction map
TFMVCRL.LDB	Low Pressure Area Correction map

3. If the Fuel Metering System is **Class A**, copy these files, as named, to the F:\UNIT1directory.

4. If the Fuel Metering System is **Class B**, Outer, Pilot, and Inner Fuel Metering Valve (FMV) maps need to be established.

   Do the following for the Outer FMV Serial Number data:

   a. Copy TFMVAR.LDB to TFMVOAR.LDB in the unit directory.

   b. Copy TFMVCRH.LDB to TFMVOCRH.LDB in the unit directory.

   c. Copy TFMVCRL.LDB to TFMVOCRL.LDB in the unit directory.

   For the Pilot FMV Serial Number data:

   a. Copy TFMVAR.LDB to TFMVPAR.LDB in the unit directory.

   b. Copy TFMVCRH.LDB to TFMVPCRH.LDB in the unit directory.

   c. Copy TFMVCRL.LDB to TFMVPCRL.LDB in the unit directory.

   For the Inner FMV Serial Number data:

   a. Copy TFMVAR.LDB to TFMVIAR.LDB in the unit directory.

   b. Copy TFMVCRH.LDB to TFMVICRH.LDB in the unit directory.

   c. Copy TFMVCRL.LDB to TFMVICRL.LDB in the unit directory.

5. Install these maps into the Mark V LM Control Engine software by recompiling and downloading the LDB.AP1 file. Then, enter the Valve Part and Serial Number Data into NVRAM using the FMVID program described below.

The FMVID program reads the valve serial number in the *ID* field at the top of the LDB files associated with a specific FMV and compares it to a value typed into the command line as prompted by the program FMVID. The FMVID program online help is provided when the user enters the command FMVID:

FMVID - FMV IDENTIFICATION UTILITY

This program will show the user which FMVs are listed in the unit's NVRAM as being installed on the unit. The FMV identification can be changed by using the /SET option.

COMMAND LINE: FMVID <UnitName> [/SET=<num>:<part>:<serial>]

The unit name must be supplied. If no /SET commands are supplied then no changes will be made, and the current settings will be shown. If one or more /SET commands are supplied, the values will be changed in the unit's NVRAM, and the resulting configuration will be shown.

/SET=<num>:<part_num>:<serial_num>

This option will set the given FMV number to expect the given part and serial number. The FMV number is an integer (1..n), the part number and serial number are treated as strings. More than one /SET can be given on the command line.

Example: FMVID T1 /SET=1:C329465-B2:11

This registers unit T1's FMV number one (1) as expecting part number C32465-B2, serial number 11. After the change is made, the new configuration is shown.

Specialized big blocks called xFMVSEC, where x = I, O, P or M, ensure that the fuel metering system security is properly implemented. I, O and P are Inner, Outer and Pilot, respectively; while M is Main. The appropriate block(s) are compiled into the CSP to carry out these three basic functions:

1. Compare the string in the map files' ID field to Non-Volatile RAM (NVRAM)
2. Determine if each valves' LDB map file and manually entered strings match
3. Set the big block start permissive and inhibit signals as required

The first string in NVRAM is the Main or Outer FMV, second string is the Pilot FMV and the third string is the Inner FMV. The engines listed below require the following fuel metering valve security algorithms:

- LM1600 DLE engines require IFMVSEC and OFMVSEC.
- LM6000 DLE engines require IFMVSEC, OFMVSEC and PFMVSEC.
- LM2500(+) DLE engines require IFMVSEC, OFMVSEC and PFMVSEC when equipped with the three FMV Class B fuel metering system) or just MFMVSEC when equipped with the one FMV Class A fuel metering system.

Trip History Function

The Trip History logging automatically collects and stores a predefined set of analog and boolean data in Control Engine memory while a turbine is running. These data are saved in a logarithmic progression to help diagnose the source of turbine trips. In addition, the 30 most recent alarms with their date/time stamp are also saved. This information is maintained in Control Engine RAM as the turbine is running and written out to a TRIP.AP1 file in the *unit/log* directory of Control Engine flash after a trip. A trip is defined as the L4 logical transitioning from TRUE to FALSE (1 to 0).

The software signal names to be monitored are entered into the HIST_Q.SRC file in a vertical list of up to 63 parameters. HIST_Q.SRC is compiled by TABLE_C to create HIST.AP1 for download the to the Control Engine. The Control Engine will implement the changed Trip History Logging parameter list within two minutes of HIST.AP1 being downloaded to the Control Engine without requiring a Control Engine reboot.

Data in the Control Engine may be collected and viewed online with the TRIPDLOG command (Trip History icon) to open the Trip History dialog box. Information collected as *New Data* may later be viewed as *Saved History Data* . These data remain in Control Engine RAM until overwritten by another New Data collection or until the Control Engine is rebooted. *Trip History Data* is written to Control Engine flash when the turbine trips and is saved until the next time the turbine trips. The TRIP.AP1 file collected after a trip is available even after the control is rebooted.

These data may be uploaded to the HMI by running the TRIPHIST.EXE command line program provided with the TCI product software or by saving the TRIPDLOG output to a file. The TRIPHIST command provides the capability to save turbine operating parameters and alarms from New, Saved or TripHistory Data into separate TXT or CSV files on the HMI.

Linearization Database (LDB) Function

LDB is a data structure in the Mark V LM Control Engine and provides a separate database from the UniData® database for univariant and bivariant analog linear interpolation data. More simply, it is called *table database*. It is used to supply linear interpolation blocks the data they need to perform linearization functions. Previous SPEEDTRONIC control systems, stored this data in the CSDB as control constants. This option is still available in Mark V LM for smaller tables and job-specific use.

The amount and size of these tables required the creation of a separate database to hold all of this data and to save constant space in the CSDB. To accomplish this, the table name given by GEAE is placed into the UniData database as a control constant. The control constant is used to provide a cross-reference to an ASCII text file, containing the table look-up data, in the F:\UNIT1 directory. These tables are contained in *.LDB files in F:\UNIT1 and cross-referenced to their *address* constant in LDB_Q.SRC. The LDB_Q.SRC and *.LDB files are compiled by the TABLE_C program into the LDB.AP1 file for download to the Control Engine.

There are two primary sources of the *.LDB files:

- Tables from the GEAE Control Specifications are provided by GEAE as controlled releases.
- DLE tables required for the FMV files are controlled and released by GE Industrial Systems.

Some of the files in this database are set up to be adjustable online as required by GEAE. The outputs, or Z dimension values, are the only online adjustable values. Adjustments are accomplished by using a text editor and downloaded to the Control Engine through the LDB2RAM command line program that is part of TCI software. The table to be adjusted may be referenced by its either filename or address constant. Limits on the minimum and maximum Z value are also embedded in the table. A sample annotated .LDB file header follows for instructional purposes only:

```
[HEADER]
;     "------------------------"  Max size of ID and REV fields
ID     = "GEAE name or FMV Serial"
REV    = "date/time stamp"
;     "-------"                   Max size of ENG_? fields
ENG_X  = "units"  Optional text string
ENG_Y  = "units"  Optional text string
– line may be omitted for univariant (2D) tables
ENG_Z  = "units"  Optional text string
DIM_X  =      2   Total number of X values in array
DIM_Y  =      0   Total number of Y values in array
MIN_Z =     0.0 Min allowable output value
MAX_Z =     1.7 Max allowable output value
ADJUST = 0  0 = not online adjustable, 1  = online adjustable
[DATA X]   All data following this line is the X array,
until next [DATA] is reached
           15.000
          300.000
[DATA Y]     All data following this line is the Y array,
until next [DATA] is reached – Omitted for 2D tables
[DATA Z]          All data following this line is the Z array,
table lookup output
           .25000
           .25000
```

IO Transfer and Scaling

The Mark V LM Control Engine IO Transfer and Scaling functions place data in the proper Control Engine memory locations and convert analog data into the proper format, respectively. All CSDB data exchanged between the IO Engines and Control Engine are placed in a fixed memory location. Analog input data from the IO Engines is converted from two-byte integer format to four-byte real format. Analog output data to the IO Engines is converted from four-byte real format to two-byte integer format.

IO Transfer

The IO data transfer into and out of the assigned Control Engine memory locations is controlled by a Vote Transfer file called VXFR.AP1. This file contains the IO Transfer tables associated with the current Mark V LM controller configuration. This file is located in the *unit/product* directory of the Control Engine and should be uploaded to the HMI F:\UNIT1 directory whenever a product software upgrade is done at a customer site.

IO Scaling

Analog IO scaling is required in the Mark V LM since IO data on must be in two-byte integer format, while the Control Engine floating point processor requires four-byte real format. The VXSC.AP1 file contains the IO Conversion Factors for the analog inputs and outputs for a specific requisition. The source files VXFR.AP1, UNITDATA.DAT and IOSCALE.DAT are used by TABLE_C to create VXSC.AP1. Indirectly, IO.ASG is the source for the analog IO scaling data, since the scale codes assigned in IO.ASG are compiled into UNITDATA.DAT by the database compiler when MK5MAKE.BAT is run.

The scale type column of IO.ASG contains a string representing the IOSCALE.DAT scale type for converting a two-byte integer value to a four-byte real for use in the CSP. The CSDB full-scale value in the IO Configuration (when required as an input) must be the same as the Scale Type gain value for that input in IO.ASG. Otherwise the value in the CDB will no be an accurate representation of the actual value read by the IO board. The vibration, servo, LVDT, RTD and thermocouple inputs all have fixed CSDB values in the IO Configuration. The IO.ASG file is arranged as follows:

Hardware Name	Software Signal Name	Scale Type
(assigned in VARDEF, does not change)	(name used in CSP to describe the input device and scaling)	(2 to 6 character alpha-numeric code to convert-between 2-byte integer and 4-byte real values)

Rolling Average Function

The Rolling Average function in the Mark V LM is for fuel property input signal processing in DLE fuel system control. Lower heating value (LHV), specific gravity (SG), ratio of specific heats (Cp/Cv), and gas compressibility (Z) are typical parameters in gas fuel systems. A rolling average is required for every non-redundant fuel property input, when the Control Engine does not compute it. To ensure smooth operation of the control in response to changes to these parameters, input signal processing and fault detection is performed on each input using a specialized BBL named GAS_ISP.

If a fault is detected, GAS_ISP substitutes a one-hour rolling average in place of the present input value. The rolling average calculations are made by a dedicated function in the Control Engine, which receives the value to be averaged from the CSDB and also passes back to the CSDB. The CSDB signals that control the rolling average function are entered ROLL_Q.SRC, which is complied using TABLE_C to generate ROLL.AP1.

The Rolling Average function interfaces to GAS_ISP parameters described below through the three columns in the sample ROLL_Q.SRC file as follows:

- Manual/Clear Logic (LAST_LMAN) – Latched output driven by momentary pushbutton
- Input Signal to Avg (GAS_SEL) – Selected output after fault handling and rate limiting
- Avg Signal to CSDB (GAS_AVG) – One-hour rolling average value passed to CSDB

```
; Manual/Clear Logic   Input Signal to Avg   Avg Signal to CSDB
; ------------------    ------------------   ------------------
  LLHVMAN               LHVSEL                LHVAVG
  LSGMAN                SGSEL                 SGAVG
  LCPCVMAN              CP_CV_SEL             CPCVAVG
  LZMAN                 ZSEL                  ZAVG
```

The Rolling Average function, in conjunction with GAS_ISP, impacts the value used by the CSP (GAS_SEL) as described in the table below. The GAS_FAIL logic and LAST_LMAN (Manual/Clear Logic) have the following impact on the CSP:

GAS_FAIL	LAST_LMAN	Resulting Action
True	True	Step change Input and Average value to manual input value within 1 min
True	False	Input value transitions to average at rate set by GAS_LIM parameter
False	True	Step change Input and Average value to manual input value within 1 min
False	False	Input value transitions to GAS_INPUT at rate set by GAS_LIM parameter

Totalizers, Timers, Counters, and Peak Detectors

The Mark V LM has 100 four-byte accumulators in fixed locations in Non-Volatile RAM (NVRAM) for tracking engine operating history. The NVRAM chip is located on the UCIB board in <R> and is equipped with a battery to preserve the stored data in the event of a Mark V LM power loss. In addition, all of the accumulator data in NVRAM is written to the Control Engine flash drive in a file called TOTD.AP1 once each hour. Therefore, a failure of NVRAM will not lose more than one hour of accumulator data.

The parameters to be accumulated are entered into the TOTT_Q.SRC file on the operator interface as described below. TOTT_Q.SRC is compiled by TABLE_C to create TOTT.AP1 for download the to the Control Engine. The Control Engine will zero out what was previously in the accumulators and implement the revised Accumulator parameter list within two minutes. No Control Engine reboot is required to activate the new parameter list.

The accumulator default signal names have been placed into ALLOCSSP.ASG for assignment of custom signal names. The display variable, ACCUM_DSPnn, must be used to view the value of an accumulator. The following lines are a sample entry in ALLOCSSP.ASG:

```
ACCUM_DSP01  TOTAL_STRTS  NONEG

ACCUM_DSP02  FIRED_HRS    HOURS

ACCUM_DSP03  PK_CYCS_0    TC

ACCUM_DSP04  FUEL_FLOW    K_LBS
```

The associated lines in TOTT_Q.SRC define the accumulator type and the signal being accumulated, which is written to in the CSP. The order, from top to bottom in TOTT_Q.SRC, dictates which accumulator will hold the data. To be more specific, the first signal listed in TOTT_Q.SRC will write to ACCUM_DSP01 listed in ALLOCSSP.ASG, and so on. That name given to the accumulator in ALLOCSSP is shown as a comment (semicolon indicates comment) in TOTT_Q for cross-referencing purposes. It is important to ensure that the scale type assigned in ALLOCSSP.ASG is correct for the type of data being accumulated. The following lines are a sample entry in TOTT_Q.SRC, which correspond to the lines in ALLOCSSP listed above:

```
1  L30CTS     ;TOTAL_STRTS

2  L30FT_T       ;FIRED_HOURS

5  TFLCYCS_0     ;PK_CYCS_0

6  FQG_TOT .001  ;FUEL_FLOW
```

Valid accumulator types in TOTT_Q.SRC are:

- Type 1 – Counter. The NVRAM value of this accumulator increments by one each time the associated software logic signal in TOTT_Q.SRC transitions from zero to one. The scale type of the display signal defined in ALLOCSSP.ASG must be assigned as NONEG for a Type 1.
- Type 2 – Timer. The NVRAM value of this accumulator continuously increments while the associated software logic signal in TOTT_Q.SRC has a value of one. The scale type of the display signal defined in ALLOCSSP.ASG must be assigned as HOURS for a Type 2.

- Types 3 and Type 4 – Not valid for Mark V LM, reserved for HMI interface to Mark V.
- Type 5 – Peak Detection. This accumulator is used to record the maximum value of any analog signal in NVRAM. The scale type of the display signal defined in ALLOCSSP.ASG may be assigned as any analog scale type.
- Type 6 – Analog Accumulator. This accumulator presumes an input of pounds per second for fuel flow accumulation. A scaling factor is defined with the accumulator type in TOTT_Q.SRC. The value saved in NVRAM under the analog signal name in ALLOCSSP.ASG is normally scaled in K_LBS, which means *thousands of pounds*.
- Type 7 – Meter Accumulator. This accumulator is used to total the number of zero-to-one transitions of a software logic signal. This value is stored in NVRAM in units of a selected display scale. The signal name in TOTT_Q.SRC will be multiplied by the scaling factor on the same line, each time the number of transitions (also listed on the same line) are counted up and saved in NVRAM under an analog signal name in ALLOCSSP.ASG. An example of this is kilowatt-hours based on a contact input or logic pulse in the CSP.

Setting Accumulators to Zero

Each accumulator location listed previously can be set to zero for restarting or changed to another type without requiring a Control Engine reboot. The Control Engine tests for a change to the TOTT.AP1 file every two minutes.

To set an accumulator value to zero, the original accumulator type in TOTT_Q.SRC should be changed to 0. Then recompile TOTT_Q.SRC with the command TABLE_C TOTT and download the resulting TOTT.AP1. Within two minutes the value will be reset to zero and will remain at zero until the accumulator type in TOTT_Q.SRC is changed. It can be changed from Type 0 to its original Type or any other type if the sequencing supports it, and recompiled and downloaded. Within two minutes of the second download of TOTT.AP1, the accumulators will resume their normal function.

Setting Accumulators to Specific Values

Accumulators can be set to predetermined values and start accumulating from that value. A file named TOTDINZ.TXT needs to be filled out with the value for each accumulator defined.

Therefore, if accumulator 23 of 33 is the only one requiring reset, all others with the values shown in their assigned software signal names must also be recorded from the HMI and entered into the file using the format shown on the next page. The TOTDINZ.TXT should be filled out as follows:

```
ID “TDIZ” ;File ID.
;
; type 0 dummy example:
LONG 0                                    ; type 0 lsh, always 0
LONG 0                                    ; type 0 msh always 0
;
; type 1 counter example:
LONG 0  -> 100000000                      ; type 1 lsh
LONG 0                                    ; type 1 msh always 0
;
;type 2 timer example:
DOUBLE 0.0 -> 10000000000.0               ;type 2
;
;type 5 peak example:
FLOAT 0 -> max 4byte float                ;type 5 lsh
FLOAT 0                                   ;type 5 msh always 0
;
;type 6 analog example:
DOUBLE 0.0 -> 10000000000.0    ;type 6
;
;type 7 meter example:
DOUBLE 0.0 -> 10000000000.0    ;type 7
;
```

A TOTDINZ.AP1 is compiled with the command TXT2AP1 TOTDINZ.TXT. After downloading TOTDINZ.AP1, reboot the Control Engine. During reboot, NVRAM will be populated with the contents of TOTDINZ.AP1, if it is present, instead of TOTD.AP1, as it normally would. After that, TOTDINZ.AP1 file is copied into TOTD.AP1 and TOTDINZ.AP1 is automatically deleted from the Control Engine. The user should also ensure that TOTDINZ.AP1 is removed from the HMI to prevent downloading it again.

<R5> Milliamp Output Scaling

There are 16 low-resolution milliamp outputs set by the TCCA board in the R5 core and have a fixed output scaling of 0 to 100%. The subject outputs are terminated on the CTBA board, at Location 6 of the R5 core. Therefore, a gain factor with units of %/unit will need to be applied in the CSP. If the full scale to be displayed is 0-50 psi = 0-100 %, the gain factor would be calculated as 100%/50psi = 2%/psi.

The best way to apply a gain and offset in the CSP is done with the SIG_SCALE1 or OUT_SCALE1 generic big blocks, since each can accommodate multiple outputs. The input, gain, offset and output software signal names must be added to the appropriate ASG file. The input may already be assigned in *.ASG or UNITDATA.TPL. The gain and offset are usually constants assigned in either FACTORY.ASG or SITE.ASG, with the value of each in CONST_Q.SRC. The output software signal name must be assigned to R5_MAO_REFnn in IO.ASG.

If the SIG_SCALE1 algorithm is used, the offset is subtracted from the input before the gain is applied. For example, a range 10 to 50 psi is converted to 0 to 100 % as follows:

output(%) = (input(psi) - 10psi)*(100%/40psi);

therefore, OFFSET=10 psi GAIN=2.5%/psi.

If the OUT_SCALE1 algorithm is used, the offset is added after the gain is applied to the input. Using the same example as above, 10 to 50 psi is converted to 0 to 100 %:

output(%) = input(psi)*(100%/40psi)*(-10psi*(100%/40psi));

therefore, OFFSET= (-10psi*(100%/40psi)) = -25 % GAIN=2.5%/psi.

If an appropriate gain scaling (e.g., %/psi, %/rpm, etc) is not available in the database, it may be added manually or the scale type N_D (non-dimensional) may be used. Since all values in the Control Engine are dimensionless, the scale type only provides a units string for documentation and display.

Sequence of Events Logger

The Sequence of Events (SOE) Logger is also referred to as Contact Input Change Detection or Digital Input Function. It records the time that a contact input changes state with 1 millisecond accuracy. This level of accuracy is achieved by placing the time stamp program in the TCDA Promset. The Control Engine assigns a contact input change to the correct CSDB address and passes it to the HMI for logging. An SOED.AP1 file is present in the /unit/product directory of the Control Engine to map the SOE data from the TCDA boards to their proper area in Control Engine memory.

SOE is enabled by setting the TCDA change-detect in IO_CFG to *1*. IOCFG.AP1 is then downloaded to the Control Engine and the IO Engine with the affected TCDA is rebooted. The IO Engine reconfigures the TCDA during boot up. The inversion mask and change detect status for are used only by the TCDA PROMset and IO Engine. The IO Engine uses inversion masks to set the contact inputs to their failsafe position for transmission to the Control Engine if communication with the TCDA is lost.

When a contact closes, with Mask = 0 and Change Detect = 1 in IOCFG, the following will be printed on the Alarm and Event Logger:

- Date/time stamp,
- String *SOE*,
- Software signal name,
- String *TRUE* to indicate that the logic is set,
- Written description of signal name from LONGNAME.DAT.

When the same contact opens, *FALSE* will appear in place of the *TRUE* to indicate that the logic signal has been reset. If the Contact Input Mask is Inverted (CIM_I), with Mask = 1 and Change Detect = 1 in IOCFG, the appearance of the *FALSE* and *TRUE* strings are reversed. Note that the CIM and CIM_I notations in the IO.ASG file are for information only and do not affect IOCFG.AP1 or the SOE Logger.

Card Library and Controller Configuration

The Card Library contains files for every version of Software and Firmware that could potentially be installed in a Mark V LM Controller. It is used to update the controller configuration during installation or software upgrade. Each data file has the IOCFG, DIAGC, Diagnostic Alarm Text and Diagnostic Alarm Help sections for a given revision of Software or Firmware. A compressed file with the Prom Subdirectory information for each version of engine-specific product code is also in the Card Library. The following Card Library files are placed in C:\MarkV_LM\CardLib on the HMI during installation:

- STCA1Axx DAT IO Engine motherboard
- TCCA1Bxx DAT Analog IO board
- TCCB1Bxx DAT Extended analog input board *(also contains IOCFG rev support for 320 Promset TCCBP2B)*
- TCDA1Bxx DAT Digital IO board
- TCEA1Bxx DAT Protective IO board
- TCQA1Bxx DAT Control IO board
- TCQE1Axx DAT LM Control IO board *(also contains IOCFG rev support for 320 PROMset TCQEP2A)*
- TMCy06xx Z Compressed PROM Subdirectory files
- TMCy06xx DAT Control Engine daughterboard *(also contains QNX rev support for TMQB)*
- TMIA06xx DAT IO Engine daughterboard
- UCIA1Axx DAT Control Engine motherboard

xx are the alpha characters indicating the revision level (BB is equivalent to 2.2)
y is engine-specific product code (D=LM25s, E=LM16s, F=LM6s)

The Controller Configuration is documented in a unit-specific file called CONTROLLER.CFG, which resides in the F:\UNIT1 directory of the HMI. CONTROLLER.CFG is a list of the hardware, software, and firmware to support operation of the Mark V LM controller. The CONTROLLER.CFG file must be manually updated by using the CARDID program output. The cross-reference to the Card Library files is the *xx* string in their filename. This will agree with last two characters in the SFTW_ID line in CONTROLLER.CFG. The format for each item in the PNEL.CFG file follows:

```
;
; [ITEM <String>]              - Type of item in the controller
;  NAME = <String>             - Printable name
;  CORE_BMS = <String          - BMS core to contact this item
;  SOCKET_DIAG = <Decimal_int> - BMS socket to contact this
item
;  SLOT_PHY = <Decimal_int>    - Actual physical position
within core
;  LOC_PHY = <String>          - Name of core R, R1, R2 etc
;  HDWE_ID = <String>          - Hardware catalog number
;  SFTW_ID = <String>          - Software catalog number
;  SFTW2_ID = <String>         - Software catalog number for
additional flash or 320 if applicable
;  DAUGHTER = <String>         - Identify daughterboard and po-
sition
```

CONTROLLER.CFG determines which Card Library files will be opened by MK5LMREV, which is a batch file that calls upon the four executables summarized below. The MK5LMREV command is used to manually initiate the creation of the following files in the site directory of the HMI:

PROM Subdirectory	DIAGC.DAT	DALARM.AP1T
AGENT.DAT	ALARMD.DAT	
IO_CFG.DAT	HELP_QD.DAT	

DIBUILD1.EXE extracts the IO Configuration (IOCFG) Screens from the Card Library files listed in CONTROLLER.CFG and will concatenate them into one file called IO_CFG.DAT. In addition, it creates the AGENT.DAT file, which lists the cores required by CONTROLLER.CFG to start the IO Configuration Editor. The IO Configuration Editor is the user interface to set up the IO processors scaling information, diagnostic alarms, and so on.

DCBUILD1.EXE extracts the Diagnostic Counters (DIAGC) Screens from the Card Library files listed in CONTROLLER.CFG and will concatenate them into one file called DIAGC.DAT. DIAGC is the user interface into the contents of the IO Card, IO Engine, and Control Engine processors in the Mark V LM. Its screens provide feedback regarding the IO Configuration, logic states and the raw signal levels (such as volts, amps, hardware counts).

DABUILD1.EXE extracts the Diagnostic Alarm Text and Diagnostic Alarm Help from the Card Library files listed in CONTROLLER.CFG as follows:

1. Diagnostic alarm text messages are concatenated in numerical order to form the ALARMD.DAT file.
2. Diagnostic alarm help screens are concatenated in numerical order to form the HELP_QD.DAT file to enable online diagnostic alarm explanations and recommended actions from the alarm display.

3. Core and socket information from CONTROLLER.CFG is compiled into DALARM.AP1T to instruct Control Engine on how to identify diagnostic alarms. This file needs to be downloaded to the /unit/config directory on the Control Engine.
4. Diagnostic alarm drop number directory to identify which core a board is in by its alarm drop number. The *diagnostic alarm drop number directory* is sent to MK5MAKE.LOG and can be copied to another file for reference purposes.

DPBUILD1.EXE creates the Prom subdirectory under F:\UNIT1 and extracts the *.PIC, *.TPL and *.DEF files from the appropriate TMCy06xx.DAT file listed in CONTROLLER.CFG. The extracted files are then placed into the Prom Subdirectory to configure and compile the database, sequencing and table files.

Alternative Gas Fuel Compressibility Calculation

An alternative algorithm for gas fuel compressibility available in the Mark V LM Control Engine is an American Gas Association (AGA) standard. It is called AGA Transmission Measurement Committee Report No. 8, 2nd edition, Nov. 1992, 2nd printing, July 1994. Gross Method 2 is used, hence the name AGA8M2PR given to it in the picture. This method of computing the gas fuel compressibility value is not the standard method. This algorithm only runs when enabled by special sequencing and is not compiled into the CSP downloaded to the Control Engine. It appears in the CSP as for documentation purposes only.

It requires two inputs that are not required by our standard software. The mole fraction of Nitrogen (N_2) and Carbon Dioxide (CO_2) present in the gas fuel. The ranges of Natural Gas characteristics for which Gross Method 2 will still provide a valid computation for compressibility are:

- Relative Density (SGSEL) 0.554 to 0.87 at 60 °F, 14.73 psia
- Gross Heating Value 477 to 1150 btu/scf at 60°F, 14.73 psia
- Gross Heating Value 18.7 to 45.1 MJ/m^3 at 0 °C, 0.101325Mpa
- Mole Percent Methane 45.0 to 100.0 (0.450 to 1.000 fraction)
- Mole Percent Nitrogen 0.0 to 50.0 (0.0 to 0.5 fraction)
- Mole Percent Carbon Dioxide 0.0 to 30.00 (0.0 to 0.30 fraction)
- Mole Percent Ethane 0.0 to 10.00 (0.0 to 0.10 fraction)
- Mole Percent Propane 0.0 to 4.0 (0.0 to 0.04 fraction)
- Mole Percent Total Butanes 0.00 to 1.0 (0.0 to 0.01 fraction)
- Mole Percent Total Pentanes 0.0 to 0.3 (0.0 to 0.003 fraction)
- Mole Percent Hexane Plus 0.0 to 0.2 (0.0 to 0.002 fraction)
- Mole Percent Helium 0.0 to 0.2 (0.0 to 0.002 fraction)
- Mole Percent Hydrogen 0.0 to 10.0 (0.0 to 0.1 fraction)
- Mole Percent Carbon Monoxide 0.0 to 3.0 (0.0 to 0.03 fraction)
- Mole Percent Argon 0.0 (0.0 fraction)
- Mole Percent Oxygen 0.0 (0.0 fraction)
- Mole Percent Water 0.0 to 0.05 (0.0 to 0.0005 fraction)
- Mole Percent Hydrogen Sulfide 0.0 to 0.02 (0.0 to 0.0002 fraction)

The measured characteristics of N_2 and CO_2 are checked against the limits listed above (0.0 to 0.5 MF of N_2 and 0.0 to 0.3 MF of CO_2). An alarm will be generated stating the as Characteristics are outside the permissible range. If the values of the non-measured characteristics are outside their specified ranges, then this method should NOT be used.

The reference temperature and pressure for the Relative Density (Specific Gravity) are also checked and an alarm is generated if they are outside the following limits, which are common values used throughout Europe and the US:

- Relative Density Temperature Ref (KTGR) 20 to 80 °F (-7 – 27 °C)
- Relative Density Pressure Ref (KPGR) 10 to 20 psia

This method should only be used for measured gas fuel temperatures in the range of 32 °F to 130 °F and pressures up to 1200 psia. This pressure range is not a factor in gas turbine applications, but the temperature range may be too restrictive for some applications, since typical gas fuel supply temperatures may range from 100 – 150 °F (38 – 66 °C). If the gas fuel supply temperature is outside this range, an alarm will be generated but the computation will still provide a compressibility based upon the measured gas fuel supply temperature.

Chapter 6 General I/O Capacities and Specifications

Introduction

This chapter provides tables of input/output (I/O) for the Mark V LM controller. The information is presented as follows:

Contact Inputs

The Mark V LM controller provides either 125 V dc or 24 V dc from power distribution core to provide a fuse isolated and current limited interrogation voltage for the contact inputs. The DTBA and DTBB terminal boards have jumpers that can be used to isolate field grounds by disconnecting the interrogation voltage. They are connected in groups of eight contact inputs. These jumpers should only be changed while the turbine is not running. Each contact input is optically isolated on the TCDA board, which is in Location 1 of the digital I/O core.

Each contact input receives a time stamp within 1 millisecond of a status change by the processor located on the TCDA board. The operator interface printer can log each contact input status change with the time stamp if that input is selected for logging. Diagnostic tests run continuously and initiate an alarm if the contact input circuit fails.

Table 6-1. Contact Inputs

Core	Number of Inputs	Ratings	Comments
Q11, Q51	96	4 mA at 125 V dc per input: 12 mA for paralleled inputs	Consult factory for voltages other than 125 V dc
Q21	96	Same as Q11	Optional core.
P1	7	Series contacts for *4's* circuit	Manual and external trip inputs to Master Trip Circuit. Open to trip
P1	1 to 3	12 mA at 125 V dc	52G auxiliary contact
P1	1	Breaker close current	Close Permissive
P1	1	Breaker close current	Manual Sync Input. Close breaker through sync check only

Table Notes:

1. Electro-mechanical relay contacts only.
2. *1 to 3* means 1 contacts parallel wired to 3 boards – <X>, <Y>, <Z> in <P1>.

Contact and Solenoid Outputs

The Mark V LM exclusively uses plug-in type magnetic relays for contact outputs (that is, no solid-state outputs). With the exception of the <P1> core, all of the relays are mounted on the TCRA boards in the <Q11> and <Q51> digital I/O cores. There are two TCRA boards in each of the digital I/O cores.

The capacities listed below are the **total contact outputs available**. By selecting jumpers on the terminal boards, certain outputs can be internally powered by 125 V dc or 120 V ac. These internally powered outputs are also called solenoid outputs. A 15 A fuse in the <PD> core protects each terminal board. The *Solenoid Outputs* column of these tables provides the number of contact outputs that can be internally powered by 125 V dc or 120 V ac, depending on the application.

Each TCRA board has a maximum of 30 contact outputs. The TCRA in core <Q11>, location 4 has 4 contact outputs for special use. Eighteen contact outputs on the TCRA in core <Q51>, location 4 of <Q51> and 16 of the contact outputs on the TCRA boards in location 5 of both cores can be self-powered with 125 V dc using hardware jumpers. Two contact outputs on the TCRA in location 5 of both cores can be powered with 120 or 240 V ac (15 A) if the power connectors are installed.

Table 6-2. Contact Outputs

Core	Total Contacts	Number of Contacts That Can Be Solenoid Outputs*	Comments
Q11	34	4 on the TCRA board in Loc 4; controlled by TCQE in <R1> and 16 on the TCRA board in Loc 5; 18 with 2 described per comment.	2 additional contact outputs may be self powered by ac on the TCRA board in location five, normally used for ignition transformers. The 4 other outputs are only for gas manifold blowoff valves.
Q21	60	Optional core. No solenoid outputs.	
Q51	60	34 total, 18 on one board, 16 on the other.	
P1	4 from 3	All 4 are self powered and designed as solenoid outputs.	Fuel Shut Off Valve power.
P1	1 from 3		Series logic for automatic sync signal and complete sequence.
P1	1 from 3		Breaker Close coil connection, series connection of 25, 25P, 25A relays.

Table Notes:

1. Electro-mechanical relay contacts are factory rated at the values shown in Table 6-3.
2. All contacts are form C; 3- wire; one normally open and one normally closed with a common center conductor.
3. *4 from 3* means 4 outputs that are voted at the relay contacts from X, Y, and Z.

Table 6-3. Electromechanical Relay Contacts

Volts	Inductive	Resistive	Other	Comments
120 ac	2 A	3 A	10 A in-rush	Breaker Control circuits and similar circuits requiring additional interrupting capacity should use other devices to interrupt current flow, for example, auxiliary contacts.
220-240 ac	2 A	3 A	10 A in-rush	See above.
125 dc	0.2 A (no suppression)	0.5 A	0.5 A (with suppression)	See above.
28 dc	2 A	3 A		See above.

Thermocouple Inputs

Thermocouple inputs to the Mark V LM are organized in two groups: thermocouples which feed the TCQA boards in <R1>, <R2> and <R3> and thermocouples which feed the TCCA board in <R5>. A total of 45 thermocouple inputs can be monitored by the <R1>, <R2> and <R3> cores. These inputs are landed on the TBQA terminal board and are divided into three groups of 15, one group for each core, with separate solid-state cold junction compensation. The thermocouple inputs are typically used for control and trips.

The <R5> controller can monitor forty-two thermocouples which are landed on a TBQA terminal board in the <R5> core. These inputs are divided into three groups of fourteen inputs with separate solid-state cold junction compensation. The <R5> inputs are typically used for monitoring only - no control or trip.

Table 6-4. Thermocouple Inputs

Core	Inputs	Comments
R1	15	For monitoring and protection.
R2	15	For monitoring and protection.
R3	15	For monitoring and protection.
R5	42	Typically used for monitoring only; not for protection

Table Notes:

1. The thermocouples inTable 6-5 may be used in any configuration. Each input is set separately in software, thus it is not necessary to group types together.
2. Thermocouples may be grounded or ungrounded.
3. Thermocouples may have up to 1000 feet (305 meters) of 16 or 18 AWG wire.
4. A separate solid-state cold junction compensation device is mounted on the board where the field wires terminate for each input.
5. Thermocouple diagnostics vary with the application, but any input will alarm if the circuit opens.
6. Linearization for different thermocouple types is provided in software.

Table 6-5. Thermocouple Ranges

Type	Range in ºF	Range in ºC
E	-60 to +1150	-51 to +621
J	-60 to +1500	-51 to +816
K	-60 to +2000	-51 to +1093
T	-60 to +750	-51 for +399

Resistance Temperature Device (RTD) Inputs

Table 6-6. RTD Inputs

Core	Inputs	Comments
R1	4	TCQE board; may use 200 Ohm RTDs.
R5	44	TCCA and TCCB board, may use 200 Ohm RTDs

Table Notes:

1. The RTDs in Table 6-7 may be used in any configuration. Each input is set separately in software, thus it is not necessary to group types together.
2. RTDs may have up to 1000 feet (305 meters) of 12 to 18 AWG wire.
3. Linearization for different types of RTD's is done in software.
4. RTDs may be grounded or ungrounded.

Table 6-7. RTD Statistics

Ohms	Composition	Manufacturer/ Standard	Range in °F	Range in °C
10	Copper	SAMA or GE	-60 to +500	-51 to +260
100	Platinum	SAMA	-60 to +1100	-51 to +593
100	Platinum	DIN 43760	-60 to +1292	-51 to +700
100	Platinum	MINCO (PA)	-60 to +1292	-51 to +700
100	Platinum	MINCO (PB)	-60 to +1292	-51 to +700
100	Platinum	Rosemont 104	-60 to +1292	-51 to +700
120	Nickel	MINCO (NA)	-60 to +480	-51 to +249
200 #	Platinum	----------	-60 to 400	-51.1 to 204.4
OHMS	Chip Detector	Engine Lube Oil	NA	NA

Seismic (Velocity) Vibration Measurement Device Inputs

For application information see Chapter 7.

Table 6-8. Seismic Vibration Measurement Device Inputs

Core	Inputs	Comments
R1	12	TBQB/TCQA boards. Uses TBQB in <R2>.
R3	12	TBQB/TCQA boards

Proximity Transducer Inputs

For application information see Chapter 7.

Table 6-9. Proximity Transducer Inputs

Core	Inputs	Comments
R1	8	Proximiter inputs
R1	2	Position inputs
R1	1	Key phasor input
R1	3	Accelerometer inputs

Flame Detector Inputs

For application information see Chapter 7.

Table 6-10. Flame Detector Inputs

Core	Inputs	Comments
P1	8 to 3	335 V dc (+1-15V) excitation provided by internal power supplies

Table Notes: *8 to 3* means 8 inputs parallel wired to <X>, <Y>, and <Z>.

Pulse Rate Inputs

For application information see Chapter 7.

Table 6-11. Pulse Rate Inputs

Core	Inputs	Comments
R1	7[1]	Magnetic speed sensors, minimum sensitivity 0.03 volts.
R1	6	TTL inputs.
R2	6	Magnetic speed sensors, minimum sensitivity 0.03 volts.
R2	2	TTL inputs.
R3	7	Magnetic speed sensors, minimum sensitivity 0.03 volts.
R3	4	TTL inputs.
P1	2 to each <X>, <Y> and <Z> for a total of 6[2]	Magnetic speed sensors, minimum sensitivity 0.03 volts

Table Notes:

1. In the <R1> core, two of the seven speed sensors are typically not used since the HP and LP shaft speeds are usually paralleled from the PTBA terminal board in the <P1> core. In this case, only 5 magnetic speed sensors would be available.
2. In the <P1> core, the <Z> board typically does not receive a speed signal, making 4 magnetic speed sensors used. See Chapter 7 for more information.

LVDT/LVDR Position Feedback Inputs

For application information see Chapter 7.

Table 6-12. LVDT/LVDR Position Feedback Inputs

Core	Inputs	Comments
R1	16	TBQC terminal board in location 9 of <R1>.
R1	4	TBQE terminal board in location 7 of <R1>. <R1> has 20 total.
R2	16	TBQC terminal board in location 9 of <R2>.
R3	16	TBQC terminal board in location 9 of <R3>.

Table Notes:

1. All inputs may not be available in all applications. See Chapter 7.
2. Excitation power source provided in Mark V LM.

Servo Valve Outputs

For application information see Chapter 7.

Table 6-13. Servo Valve Outputs

Core	Outputs	Comments
R1, R2, R3	4	Bi-polar 10, 20, 40, 80, 120, 240 mA.

Analog Voltage and Current I/O

Most of the analog inputs to the Mark V LM controller come directly from transducers on the turbine such as vibration or speed sensors; however, 4–20 mA and 0–1 mA inputs are provided for other types of transducers.

Each analog input can receive isolated 21 V dc excitation power for the transducer from the Mark V LM. The inputs are connected to the TBQC, CTBA and TBCB terminal boards. Jumpers are provided for such selections as:

- Current or voltage input
- Burden resistor size
- And grounding options

Some inputs can be used as either voltage or current inputs by the selection of a jumper. In current input mode a burden resistor produces a voltage from the transducer current. This voltage is then internally parallel wired with ribbon cables to the TCQA boards in <R1> and <R3>. Diagnostics monitor the inputs to insure that they are within their proper range.

An additional input to the I/O cores is provided for the megawatt transducer input on generator drive units. This input is similar to a general purpose 4–20 mA input except that it terminates on the QTBA board where a jumper selects whether the input is 0–1 mA (requires a 5k ohm burden resistor) or the input is 4–20 mA (requires a 250 ohm burden resistor). The megawatt input is then wired to the TCQC board in <R1>, <R2>, or <R3>.

If a transducer is powered by the Mark V LM or by an isolated power supply, a grounding jumper should be installed on the terminal board. If the transducer is separately powered by a grounded supply, the jumper should be removed. Refer to Appendix D for jumper numbers and connection diagrams.

Both 4 – 20 mA (500 ohm max burden) and 0 – 200 mA (40 ohm max burden) analog current outputs are available. The TCCA board in the <R5> controller has 4–20 mA (500 ohm max burden) outputs available via the CTBA terminal board. These outputs can be independently configured from the Mark V LM operator interface, and are typically used for driving remote instrumentation for monitoring.

Table 6-14. Analog Voltage and Current Inputs and Outputs

Core	# of Inputs/Outputs	Comments
P1	2, 3-phase delta connected	Nominal 120 V ac inputs from Generator Potential Transformers. 1 for Bus volts, 1 for Generator volts. PTBA 29-34
P1	3, isolated, 2 wire	Nominal 5 amp Current Transformer connections. PTBA 73-78
R	2	Stage Link connections. BNC connectors. <R> AAHA
R1	2	4–20 or 0 - 200 mA current outputs. TBQE 15-18.
R1	2	4–20 or 0-200 mA current outputs. TBQC 81-84.
R1	15	4–20 mA current inputs. 21 volt power. TBQC 35-79.
R1	2	4–20 mA current OR ± 10 V dc voltage inputs. TBQB 23-46 in the <R2> core.
R1	2	4–20 mA current OR ± 10 V dc voltage inputs with excitation. TBQB 23-46 in the <R2> core.
R1	1	4–20 or 0–1 mA current OR ± 10 V dc voltage input. Usually used for MW transducer input. 21 volt power. QTBA 65-66.
R1	1	4–20 mA current OR 0-5 V dc voltage. Usually used for pressure transducer inputs. 21 volt power. TBQB 1-12 in the <R2> core.
R2	2	4–20 or 0-200 mA current outputs. TBQC 81-84.
R2	15	4–20 mA current inputs. 21 volt power. TBQC 35-79.
R2	1	4–20 or 0–1 mA current OR ± 10 V dc voltage input. Usually used for MW transducer input. 21 volt power. QTBA 65-66.
R3	2	4–20 or 0-200 mA current outputs. TBQC 81-84.
R3	15	4–20 mA current inputs. 21 volt power. TBQC 35-79.
R3	2	4–20 mA current OR ± 10 V dc voltage inputs. TBQB 23-46.
R3	2	4–20 mA current OR ± 10 V dc voltage inputs with excitation. TBQB 23-46.
R3	1	4–20 or 0–1 mA current OR ± 10 V dc voltage input. Usually used for MW transducer input. 21 volt power. QTBA 65-66.
R3	1	4–20 mA current OR 0-5 V dc voltage. Usually used for pressure transducer inputs. 21 volt power. TBQB 1-12.
R5	1	Shaft voltage input. CTBA 79-80.
R5	1	Shaft current input. CTBA 81-82.
R5	16	4 – 20 mA current outputs. CTBA 1-32.
R5	14	4 – 20 mA current inputs. 21 volt power. CTBA 37-78.
R5	22	Current inputs. 21 volt power. TBCB 1-66. 14 of 22 are 4 – 20 mA, 8 can be 4 – 20 OR 0 – 1 mA.

Table Notes:

1. For application notes see Chapter 7.
2. 21 volt power means 21 volt dc excitation power for the transducer is available. See Appendix D for connection information.
3. *TBQC 35-80* means TBQC terminal board, termination points 35 to 80. See Appendix D for connection information.

Notes

Chapter 7 Application-Specific Functions

This chapter is presented as follows:

Pulse Rate Inputs

Pulse rate inputs monitored by the Mark V LM controller fall into three categories: magnetic speed sensors which feed the TCQC boards in <R1>,<R2>, and <R3>; TTL type inputs which feed the TCQC board(s); and magnetic speed sensors which feed the TCEA boards in the Protection core, <P1>. The most common application for the pulse rate inputs is monitoring the turbine shaft speed with magnetic speed sensors. Speed is sensed by magnetic field speed sensors mounted near a multi-toothed wheel attached to the turbine shaft. These can be programmed for any number of teeth. Voltage pulses are generated by the speed sensors as the teeth of the wheel pass through the magnetic fields surrounding the speed sensors. Redundant signals are not used in the Mark V LM, signals should be landed and used in one core.

The Mark V LM can interface with the standard passive or the optional active speed sensors with an effective frequency range of 2 to 10,000 Hz. Sensitivity at 2 Hz is 0.033 V peak-to-peak which allows detecting zero speed without the need for any external devices. The maximum input voltage is 200 V peak-to-peak. Magnetic speed sensors can be monitored by the <R1>, <R2> and <R3> controllers. Speed sensors in the <P1> core are typically used for monitoring turbine speed for both the high and low pressure shafts. Consult the vendor turbine documentation or control sequence program (CSP) for details. Refer to Chapter 6 for the specific number of speed sensors available per core.

Caution

Flexible couplings must not be used for connecting Mark V LM speed feedback tachometers to the turbine shaft.

A totally separate and independent set of electronics for emergency trip protection is provided by the three TCEA boards in the <P1> core each having independent power supplies and processors. Each TCEA board can interface with two speed sensors, and the overspeed trip settings are adjustable. (See section 7-3.)

Master Trip Circuit and Protection Core

Turbine protection in the Mark V LM Control System is performed by multiple cores within the controller. The following text and illustrations show the manner in which various protective functions are implemented.

There are two parts to the Master Trip Circuit: the inputs to the Mark V LM and the outputs from the Mark V LM.

The *hardwired* or remote trip inputs to the Mark V LM (contact open to trip) connect to the *4's* relay coils (known as the *4's* for the ANSI standard device number referring to the Master Protective). These relays are energized during normal operation by 125 V dc from the power distribution core. This circuit has redundant relay coils connected to the positive dc bus in series with the external trip contact inputs and another set of redundant relay coils connected to the negative dc bus. (See Figure D-45.) A failure of any one of the four *4's* relay coils will not accidentally trip the turbine. Only de-energizing both relays connected to the same (positive or negative) dc bus will trip the turbine.

If an external trip signal is received, the *4's* trip circuit will de-energize and the voting contacts circuit will de-energize the internal 24 V dc protective bus. The supply to this 24 V dc protective bus comes from a circuit which selects the maximum voltage from three power supplies; one on each TCEA board in the <P1> core.

The 24 V dc protective bus supplies all the primary trip relays (PTRs), emergency trip relays (ETRs), and other relays which interface with the turbine trip solenoids. These PTR's and ETR's comprise the output portion of the Master Trip Circuit. The microprocessors on the TCEA boards monitor the status of the *hardwired* or remote trip inputs, however, the actual tripping is independent of any microprocessor.

The PTR's, ETR's, and *4's* are located on the TCTG board.

The Control Sequence Program (CSP) located in the <R> processor, provides protection for conditions such as loss of flame, starting means failure, excessive exhaust temperature spreads, excessive vibration, over temperatures, primary overspeed trip, and loss of hydraulic oil via the PTRs of the Master Trip Circuit. The PTR trips are JOB SPECIFIC and are defined in the CSP.

The <P1> core consists of three independent, identical TCEA printed circuit boards known as <X>, <Y>, and <Z>. These boards have their own power supplies and provide emergency overspeed protection, flame detection, and the automatic synchronization signal. If two out of three boards *vote* for a trip, a shutdown is initiated by sending signals to the ETR's on the trip board. The automatic synchronization signal energizes an output relay on the trip board and, if two out of three TCEA boards agree, will close the generator's power circuit breaker. Each board has an 80196 microprocessor that runs a continuous loop program which is stored on firmware (EPROMs). The <P1> core is standard with firmware that does not change with each application and cannot be modified without changing EPROMs.

The <P1> core master protective functions (ETRs) will be covered in this section. Job specific master protective functions (PTR's) will be covered in the CSP and other turbine vendor documentation.

Figure 7-1 is a simplified block diagram of the protective functions provided by each board <X>, <Y>, and <Z> in the <P1> core. The blocks used are representations of the firmware, which can only be changed by replacing the EPROMs. The types of blocks used are as follows:

Block	Description
AND	Logical AND function. All inputs must be *true* for the output to be *true*.
COMPARE	Compares two signals, with the output being defined by the text. For example, the software parameters are compared with the hardware jumpers. If they are not identical, a diagnostic alarm is generated. If the software and hardware are identical, the configuration information is sent on to the next block.
ISO	Isolates and conditions signals from field devices to the levels used in the processors.
LATCH	Latches the trip signal until reset manually.
LIMIT	Limits the input to the range of the MAX and MIN values.
RANGE CHECK	Limits the range of the output to within the limits defined by the MIN and MAX values. If the input is within range, the output equals the input. If the input is not within range, a diagnostic alarm will be generated.
OR	Logical OR function. Any *true* input will result in a *true* output.
RD	Relay Driver, converts logic level signals to drive the 24 V dc ETR relays.
SCALE	Scales the speed signal pulses using the configuration data to be a percent of rated speed.

The small boxes near the signal lines contain the typical Mark V LM software signal names for these signals. The values of these control signal data base point names can be monitored via the operator interface. The text in quotations is the diagnostic alarm message that will be enunciated if that alarm condition is active.

A logic high or *1* from any trip signal will de-energize the ETR relays and cause the turbine to shut down. The status of the <P1> core trip signals while in normal running condition is a logic low or *0*.

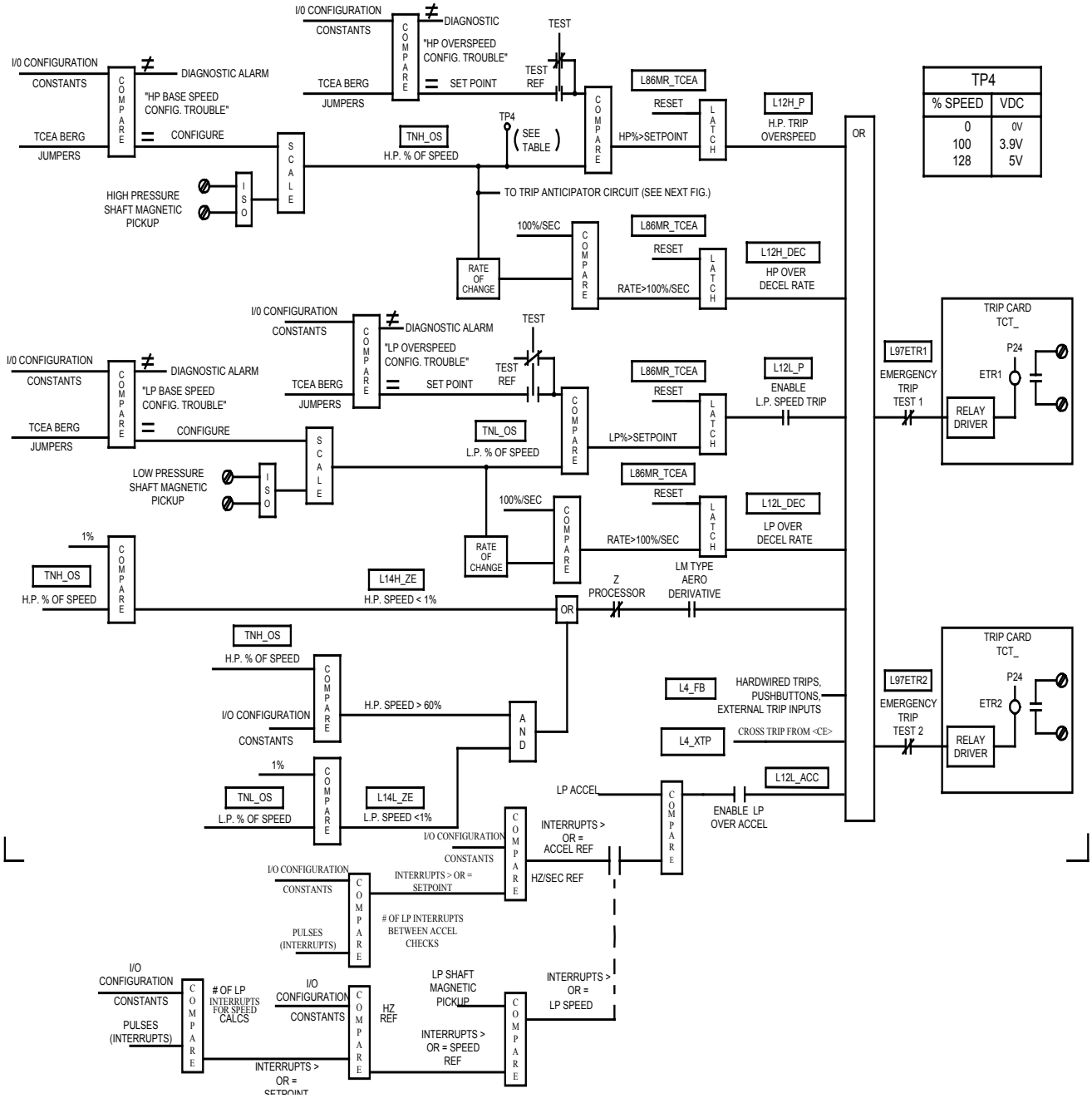


Figure 7-1. Simplified Block Diagram - TCEA Boards

The emergency overspeed trips that originate in the <P1> core are as follows:

- High Pressure Shaft (HP) Overspeed Trip – If the HP shaft scaled speed feedback exceeds the setpoint, an HP shaft overspeed trip will be initiated. This trip signal will be latched until a master reset command is given. For testing a different setpoint can be substituted for the design value.
- High Pressure Shaft Over Deceleration Rate Trip – If the HP shaft scaled speed feedback decreases faster than 100% per second, an HP shaft over-rate trip will be initiated. This fast rate of change usually indicates a defective speed sensor or wiring. This trip signal will be latched until a master reset command is given.
- Low Pressure Shaft (LP) Overspeed Trip and LP Shaft Over Deceleration Rate Trip – If enabled in a dual shaft system, these trips function in the same fashion as respective HP shaft trips.
- Locked Rotor Trip – Two additional protective functions are provided in the <X> and <Y> boards only (the boards are identical; jumpers are used to select the option). If the HP shaft speed is greater than 60% and the LP shaft speed is less than 1%, a trip will be initiated. Also, any time the HP shaft speed is less than 1% of rated speed a trip will be initiated.
- Hardwired Trips – Any pushbuttons or other hardwired trips initiated outside the Mark V LM control system will be connected to the PTBA terminal board in the <P1> core (see Appendix D, D-45). These hardwired trips will de-energize the 24 V dc supply from all the ETR and PTR relays. The <P1> core will also initiate a trip.
- Cross Trip from <R> – If the CSP in <R> initiates a trip to the PTR relays, a backup signal will be sent to the <P1> core to also trip the ETR relays.
- LP Over Acceleration Trip – If the LP shaft scaled speed feedback rate of change exceeds the setpoint, and the LP shaft speed exceeds the enable threshold, an LP over-acceleration trip is initiated. This trip signal is latched until a master reset command is given. This trip must be enabled in the I/O Configurator.

Each of these trip functions is derived independently by <X>, <Y>, and <Z>. In some LM applications, two speed signals are brought in to the <X> and <Y> boards only. The <Z> board is set with hardware jumpers to always initiate a trip for overspeed conditions. All of the hardware jumpers on the <X>, <Y>, and <Z> boards need to be set identical to each other. This creates a dual redundant system. The <X> and <Y> boards send their respective trip signals to their separate relays on the trip (TCTG) board. The two out of three voting takes place with the relay contacts. Throughout the documentation and drawings, the abbreviation *2/3* has been adopted to mean *two out of three*.

Trip Board TCTG

The trip board has four separate sets of three primary trip relays (PTR1, 2, 3 &4), and two separate sets of three emergency trip relays (ETR1 & 2). The PTRs are controlled from the TCQA board in the <R1> core, and the ETRs are controlled from the TCEA boards in <P1>. If two out of three PTRs or two out of three ETRs de-energize, the turbine will trip. The TCTG board also has three relays for synchronizing in addition to other auxiliary relays. Table 7-1 details which solenoid output will de-energize for a given relay output. The " √ " indicates this solenoid will de-energize if the relay is de-energized. See Appendix D for the signal flow diagrams.

Table 7-1. Solenoid Output

Relays	Solenoid 1	Solenoid 2	Solenoid 3	Solenoid 4
2/3 ETR 1	√		√	
2/3 ETR 2		√		√
2/3 PTR 1	√			
2/3 PTR 2		√		
2/3 PTR 3			√	
2/3 PTR 4				√

Primary and Emergency Overspeed Trip Setpoints

The Mark V LM control system provides two independent levels of electronic overspeed protection—primary and emergency—for up to two turbine shafts.

Primary overspeed detection and trip initiation is accomplished by the overspeed protection Big Block Language (BBL) blocks of the CSP in the <R> control processor. These blocks use the turbine shaft speed sensors typically landed on the PTBA terminal board in the <P1> core. The Control Constants define the trip setpoints for the blocks. The magnetic speed sensor pulses are filtered and scaled (converted to percent of rated shaft speed) by the I/O boards. When the scaled turbine shaft speed signal exceeds a Control Constant setpoint, the CSP overspeed block initiates a turbine trip.

The emergency overspeed protection is accomplished by the protective processors <X>, <Y>, and <Z> in the protective core, <P1>. Emergency overspeed protection is completely independent of primary overspeed protection. The turbine shaft speed sensors landed on the PTBA terminal board are used.

Note The Mark V LM will not permit turbine operation without HP shaft speed sensor inputs connected to the protective processors. LP shaft emergency speed sensors must be connected, as well, if the unit has an LP shaft.

Emergency overspeed protection is performed by algorithms based on I/O Configuration software on the TCEA boards in the <P1> core. The emergency overspeed setpoint must be the same in the I/O Configuration Constants file as in the hardware jumper settings. If these two are not set the same, a diagnostic alarm will be enunciated.

The frequency of the pulses from the shaft speed sensors depends on the number of teeth on the feedback wheel as well as shaft RPM. For example, most heavy duty gas turbines use magnetic speed pickups with 60-toothed speed sensing wheels for primary and emergency shaft speed feedback signals. In this case there are 60 pulses per revolution, so the frequency of the speed signal is equal to the RPM of the shaft (1 Hz equals 1 RPM). The <R1> core scales the primary speed feedback signals to be a percent of rated shaft speed. Rated shaft speed is the speed at which the turbine is designed to be operated, not the highest possible maximum shaft speed.

Emergency speed feedback signals are normally scaled to percent of rated design speed, not necessarily normal operating speed. For example, a turbine whose rated design speed is different from its normal operating speed is a Frame 6 heavy duty single shaft gas turbine being used as the prime mover for a generator through a gear box. To operate at synchronous speed, the input to the gear box must be at 5196 RPM. The rated design speed for a Frame 6 heavy duty single-shaft gas turbine is 5100 RPM. In this case, the normal operating speed would be 5196 RPM. Therefore it is possible that the scaled primary speed feedback signal and the scaled emergency speed feedback signal may not have the same value for percent of HP shaft speed.

The following two sections describe the operation and adjustment of the primary and emergency overspeed protection functions.

Primary Overspeed Protection

The turbine speed sensor is typically connected to a pulse rate input on the PTBA terminal board in location 6 of the <P1> core. The frequency from the shaft speed sensor is converted to a percent of normal operating speed by the I/O Configuration software on the TCQA board in the <R1> core. The definition of *normal operating speed* is made on the TCQA board *Pulse Rate Definition* screen of the I/O Configurator (see the operator interface manual).

The frequency defined for the input's `Max Pulse Rate` (100% rating) is the input frequency which will be equal too normal operating turbine speed. This value must be expressed in frequency, not in RPM; the input frequency will depend on the type of input device and the number of teeth on the speed sensing wheel. The digitally scaled speed feedback signal is communicated to the communication processor <R>.

The value is used in the overspeed detection BBL block in the <R> core's CSP. If the value exceeds the primary overspeed trip value from the Control Constant table file (also expressed as a percent of normal operating speed), that processor will call for a trip via the primary trip relays. (See Section 7-2.) As with all Control Constants, the value of the turbine primary overspeed Control Constant is determined by the turbine vendor, and should not be modified without the concurrence of the factory.

Emergency Overspeed Protection

Emergency overspeed protection is provided by the Mark V LM controller. The HP (High Pressure) shaft emergency overspeed protection function must have speed feedback and it will be active. If LP (Low Pressure) shaft emergency speed protection is not necessary, it can be disabled by setting the I/O Configuration Constant overspeed setting values and hardware jumpers to zero. Two speed sensor signals, for both the HP and LP shafts, are landed on the PTBA terminal board in the <P1> core and are written to the <X> and <Y> boards. In some applications, the overspeed signals are written to the <Z> board also.

The I/O Configuration Constant overspeed setting and hardware jumper settings must agree for the control processor associated with each TCEA board to reach *ready to run*. The HP shaft emergency overspeed setting (and hence the TCEA HP shaft emergency overspeed hardware jumper settings) are defined by the turbine vendor and should not be modified without concurrence; it can be calculated using the formula shown on the I/O Configurator screen located on the operator interface.

The speed feedback frequency from the sensing device is scaled to a digital value proportional to rated design speed. The CDB point name for scaled HP shaft emergency speed feedback is expressed as a percent of rated design speed (not necessarily the same as normal operating speed: see Section 7-3).

The microprocessors on the <X> and <Y> boards compare the emergency speed feedback frequency to the overspeed setpoint (software setting in agreement with hardware settings, see above) and when it exceeds the setpoint a turbine trip is initiated by de-energizing the ETRs on the TCTG board (see Section 7-2). The <Z> board typically initiates a trip. In some applications, all three TCEA boards will vote on the trip.

LP shaft emergency overspeed detection and trip is accomplished in an identical manner. If a unit does not have an LP shaft, then the LP shaft emergency overspeed setpoints (both software and hardware) must all be set to zero.

Servo Valve Drive System

The servo valve drive system interfaces the Mark V LM control system to the hydraulic actuators that position mechanical devices. The basic system compares the actual position of the hydraulic actuators to a setpoint and outputs a position control signal that maintains the system balance. The system consists of the following components:

- Mark V LM Closed Loop Regulator Sequencing and Interface circuit.
- Servo Valve for control of oil to the hydraulic actuator or cylinder.
- Feedback devices such as LVDTs, LVDRs, pressure transducers or a combination.
- Hydraulic actuator and a source of hydraulic power to position mechanical devices.

Servo Valve

The servo valve is used to control the direction and rate of movement of a control device actuator. In effect, it acts as the interface between the electrical and mechanical systems by converting an electrical signal to a hydraulic output. In response to this electrical signal (typically less than one watt), the servo modulates high pressure hydraulic fluid to the actuator.

The servo outputs of a Mark V LM controller will generally be connected to a one-coil servo valve.

Regulator Feedback Devices

This section describes the operation of the following feedback devices:

LVDT or LVDR Position Feedback

Pressure Feedback from pressure transducers

LVDT or LVDR Position Feedback

The physical position of an actuator is detected by an LVDT (Linear Variable Differential Transformer) or an LVDR (Linear Variable Differential Reactor). The Mark V LM control provides 7 V rms and 3 kHz excitation to the device, then detects the voltage feedback. The variable ac voltage signal from an LVDT or LVDR is converted from an analog value to a digital value, then scaled to a value proportional to position. When the actual position is equal to the requested position setpoint, the servo is set to the lapped, closed, or null position. If the system is not in balance (the hydraulic actuator is not at the position setpoint), the controller will set a positive or negative current output to move the servo in the proper direction, restoring the system balance by repositioning the hydraulic actuator.

Pressure Feedback

Pressure feedback to the Mark V LM is generally provided by 4–20 mA transducers. After being converted from an analog value to a digital value, the signal is scaled to a value proportional to pressure.

Flame Detection

The flame detection system detects a flame in the combustors and trips the turbine when improper combustion is detected in the turbine firing chambers. Two principle requirements of the flame detection system are:

1. *To protect the turbine during startup.* During startup, the turbine fuel is ignited by spark plugs. These plugs are usually fired for one minute. By the end of the firing time, the flame detector must sense the presence of flame in the combustors or the startup attempt will be aborted, the fuel stop valve will close, the ignition circuits will de-energize, and the turbine will shutdown.

2. *To protect the turbine against a flameout while running.* If flame is lost while the turbine is running, fuel will be shut off and the turbine will be shut down.

Ultraviolet flame detectors monitor flame in the combustion chamber by detecting the ultraviolet radiation emitted by the flame. Each detector consists of a window body filled with hydrogen gas and a cathode element made of pure copper. When flame is present in the combustion chamber, the energy present in the ultraviolet radiation of the flame ionizes the gas and releases electrons from the pure copper cathode, causing a *cascade effect,* and a pulse of current flows.

When ultraviolet radiation is present in the tube, the resulting gas ionization causes current to pass through it, discharging (firing) the tube's capacitance. When the voltage across the tube is reduced sufficiently, the tube stops conducting. This process is repeated as the voltage across the tube again starts to rise toward its *firing voltage.* The voltage level at which the tube fires is dependent upon the intensity of the ultraviolet light present. This process continues by giving out current pulses from the tube as long as the ultraviolet (UV) light is present. In effect, pulses of current at a rate of approximately 120 per second are being generated when the system is excited by the energy present in the ultraviolet (UV) spectrum.

The Mark V LM <P1> core contains three independent, identical TCEA boards <X>, <Y>, and <Z> that have their own processors and power supplies. The power supplies provide the 335 V dc excitation current for the detectors as well as the control power for the board. Eight UV flame detectors can be connected to the <P1> core terminal boards. Each detector is then internally parallel wired to each of the three boards. This design avoids the need for interposing transducers and separate 335 V excitation supplies.

The flame detection takes place in the <P1> core and sends the information via the IONET to the <R1> control processor. The I/O Engine in <R1> sends the information across the COREBUS to the <R> core for use by the CSP. The CSP determines if and when to trip and, if necessary, will trip the PTRs. See the CSP and turbine vendor documentation for details. Appendix D Figure D-49, shows a simplified diagram of the flame detector circuit and a table with terminal numbers, cable and pin numbers, and threshold values. The threshold is the number of pulses generated by the flame detectors in 1/16th of a second. The threshold values are stored in the I/O configuration file, and should not be modified without direction from the manufacturer. The flame intensity frequency and logic names for the detector output can be displayed on the operator interface.

Vibration Measurement and Protection

Three different types of vibration sensors can be directly connected to the Mark V LM controller. These sensors or transducers are mounted on several critical components of turbine and driven load to protect against long term excessive vibration damaging the turbine or load.

Seismic (Velocity) Sensors

Normally, there are three to five transducers on the turbine which generate a small ac current by passing a magnet through a fixed coil. The Mark V LM control processors interface directly with up to twelve vibration sensors or *pickups*.

These sensors output a millivolt signal which is converted to a digital value proportional to vibration by I/O Configuration software on the TCQA board. The CSP in the <R> core uses this information in controlling and protecting the turbine. The seismic vibration pickups are terminated in the Mark V LM on the TBQB I/O Terminal board in location 7 on the <R2> and/or <R3> cores.

The types of sensor diagnostic alarms provided include:

- Open sensor detection and alarm. A small dc current is continuously passed through the vibration sensor at all times to detect a broken wire or other open input.
- Shorted sensor detection and alarm. If the dc current is still flowing and there is no signal, a sensor short is alarmed.
- Disabled sensor alarm. Failed sensors can be manually disabled via the operator interface and will result in a permanent alarm condition.

The vibration protection system will either trip or initiate a controlled shutdown of the turbine or generator under any one of the following conditions:

- A shutdown will occur if several sensors fail or are manually disabled. (The number of sensors varies with each application, thus the number of sensors out of service before a shutdown occurs will vary.)
- A trip will occur if a high level vibration is detected on any one sensor,
  - and an adjacent pair of sensors is disabled or alarmed,
  - or any other sensor is above the alarm limit.
  - or two or more sensor inputs are disabled.

Vibration inputs are monitored by the TCQA board which has a range of 0 to 0.75 V-peak and an input impedance of 100 to 2,000 ohms. Typical sensitivity ranges are 0.1 to 0.4 V peak-to-peak per inch per second.

Configuring Seismic Vibration Pickups in the Mark V LM

The I/O Configurator on the operator interface configures the seismic vibration pickups. The TCQA seismic vibration screen is used to enable the input, disable diagnostic alarms associated with unused inputs, and to provide the I/O Configuration Constants for scaling. Additional I/O Configuration information for seismic vibration pickup diagnostic alarms are entered on a separate screen. The following fields are typically edited on the I/O Configurator screens:

- `Transducer-Used` field – If a seismic vibration pickup is connected to an input point, the value YES must be entered into the Transducer-Used field on the screen and the sensitivity of the pickup must be entered in the corresponding Vibration Sensitivity field. If no pickup is connected to an input point, the value NO must be entered in the Transducer used field to prevent diagnostic alarms associated with the unused input point from being enunciated. If NO is entered under Transducer used, the value in the corresponding Vibration Sensitivity field is of no consequence.
- `Vibration Sensitivity` field – The value entered in the Vibration Sensitivity field is the sensitivity rating of the velocity-type seismic vibration pickup, and must be in English engineering units (V/inch-per-second).
- `Seismic Vibration Transducer Open Circuit` field – The entry in the Seismic Vibr. Xdcr. Open Ckt. field is the voltage above which a diagnostic alarm indicating a seismic vibration pickup open circuit condition exists (for all seismic vibration pickups). In order to accurately calculate this value, the pickup's characteristics must be known, particularly the maximum expected resistance of the pickup circuit at maximum running ambient temperatures. The formulae for calculating the value will be displayed on the appropriate TCQA I/O Configurator screen

Accelerometer Inputs

Accelerometers are used to monitor vibration on aero-derivative gas turbines. The charge amplifiers, which are located on the turbine base, feed a velocity signal to the TBQE termination board. Three accelerometers can be monitored. Internal tracking filters are used to select the appropriate frequencies which result in alarm and trip protection of the turbine.

The Mark V LM is capable of both exciting accelerometer vibration sensors and scaling accelerometer feedback signals. Configuring the Mark V LM to scale accelerometer input signals involves entering information on one I/O Configurator screen.

`HP and LP rpm max scaling value` fields – The entry in each of the three rpm maximum scaling value fields must be a power of 2 greater than the highest expected shaft speed for the high (HP) and low (LP) pressure shafts of the turbine when accelerometers are being connected to the Mark V LM. These entries are not related to the highest expected frequency from the shaft speed pickups, but the highest expected scaled shaft speed feedback signals.

Proximity Transducer Inputs

Proximity transducers use radio frequency waves to measure distance between an object and the probe. The transducer's output is a voltage signal inversely proportional to this distance. The ac component of the transducer's output is interpreted as vibration, while the dc component is interpreted as a change in position.

The Mark V LM provides a direct three-wire interface to the proximity transducer for monitoring, alarm and trip. The number of probes that each Mark V LM has have the capability to interface with changes with the application, but typically values are:

- 8 vibration inputs
- 2 position inputs
- 1 key phasor inputs

Each proximity transducer receives -24 V dc power from the Mark V LM. The vibration inputs produce a dc voltage with an ac component which must be within 3 ac V peak-to-peak and -2 to -18 V dc. Each input terminates on a single termination point and is then internally wired with ribbon cables to the TCQE board in <R1>.

The input signals from proximity transducer (and associated key phasor) inputs will be wired to the TCQE board in <R1>. The first proximity transducer input points are designated for vibration sensor inputs (PRX01 – PRX08); the next two proximity transducer input points are designated for axial position/differential expansion sensor inputs; and the last proximity transducer input point is designated for a key phasor input. Several TCQE I/O Configurator screens are used to configure proximity transducer inputs, depending on the type of input signal (that is, vibration, axial position/differential expansion, or key phasor). The following fields are typically edited on the I/O Configurator screens:

- `Proximitor Shaft Location Assignments` fields – The TCQE I/O Configurator screen is used to set the shaft assignments for the proximity transducers. Valid entries for the field for each input are HP, LP and "--" (not used). For example: the vibration proximity transducer input #1 is connected to a sensor mounted on a high-pressure turbine shaft bearing, therefore HP is entered in the field for the #1 input, meaning that the input signal will be filtered using the HP shaft speed.
- `Proximitors :- Peak to Peak Vibration Transducer Sensitivity`field – The vibration proximity transducers' nameplate sensitivity must be entered in the transducer sensitivity fields in order for the I/O Configuration software to scale the input voltage appropriately.
- `Proximitor low (or high) limit diag:` field – There are two fields in which voltage values corresponding to low and high limits for diagnostic alarms (indicating out-of-rage conditions) are entered. Common proximity transducers normally have an output range of -20.0 V dc to -2.0 V dc, with a typical voltage output of -10.0 V dc when properly installed and the shaft is at rest. Values in these fields will determine when the out of limits diagnostic alarm for the first eight proximity transducer inputs will be enunciated (these two values are for all of the first eight proximity transducer inputs).
- `Proximitors :- Position Inputs Transducer Sensitivity` fields – Axial Position/Differential Expansion proximity transducer inputs are designated for use as either axial position or differential expansion inputs. The transducer's sensitivity, from the manufacturer's nameplate, must be entered in this field for each input point to which a transducer is connected in order for I/O Configuration software to scale the input voltage appropriately.

- `Proximitors :- Position Inputs Position Offset` fields – The entries in the position offset fields will be dictated by the application. The offset setting is the zero position, at rest position, or starting position.
- `Proximitor low (or high) limit diag:` fields – There are two fields in which voltage values corresponding to low and high limits for diagnostic alarms (indicating out-of-rage conditions) are entered. Common proximity transducers normally have an output range of -20.0 V dc to -2.0 V dc, with a typical voltage output of -10.0 V dc when properly installed and the shaft is at rest. Values in these fields will determine when the *out of limits* diagnostic alarm for proximity transducer inputs will be enunciated.
- `Proximitor Keyphasor Inputs Transducer Sensitivity` field – Proximity transducer inputs are designated for use as keyphasor (shaft speed sensor) inputs. The transducer's sensitivity, from the manufacturer's nameplate, must be entered in this field for each input point to which a transducer is connected in order for I/O Configuration software to scale the input voltage appropriately and recognize the shaft's rotation indicator.
- `Proximitor Keyphasor Inputs Position Offset` field – The entry in the position offset field for keyphasor inputs will be determined by field/Customer personnel as it must be the unit's desired offset in its zero speed condition.
- `Proximitor Keyphasor Inputs Low and High Diag:` field – There are two fields in which voltage values corresponding to low and high limits for diagnostic alarms (indicating out-of-range conditions) are entered. Common proximity transducers normally have an output range of -20.0 V dc to -2.0 V dc, with a typical voltage output of -10.0 V dc when properly installed. When entering a value in these fields, the negative voltage sign is implied and must not be entered with the value. Values in these fields will determine when the out of limits diagnostic alarm for proximity transducer inputs will be enunciated. Note that the value in the high limit field is in excess of the usual -20.0 V dc; this is to disable the diagnostic alarm when key phasors are connected because of their tendency to saturate when the shaft rotation indicator passes

Shaft Voltage and Current Monitor Inputs

The Mark V LM is capable of accepting voltage inputs from shaft voltage and current monitors that monitor ac and dc voltages and ac and dc currents which might be present or develop on the turbine. An I/O Configuration screen used to define the I/O Configuration Constants which are used by the I/O Configuration software to scale the voltage input signal(s) proportional to shaft voltage and/or current. The values in these screens are provided for units having the optional shaft voltage and current monitor functions. The values scale the input signals (typically they are voltages) prior to being written into the control signal database where they are used by the shaft voltage/current monitor BBL. Consult GE Industrial Systems or the turbine vendor before changing these values. The following fields are typically edited on the IO Configurator screens:

`Full Scale CDB Value` field – The value in this field is the maximum CDB value for the scale type chosen for the input (the scale type assigned in the scale column of the unit-specific IO.ASG file). Since shaft voltage and current monitor inputs are usually between 0.0 and 16.0 V dc, the usual CDB scale type selected for these inputs is V32 which has a maximum CDB value of 32.00 V dc.

`Min (0 V) CDB Value` field – This is the minimum, or zero voltage, value for the input in V dc (typically 0.0 V dc) used to scale the input signal prior its value being written into the control signal database.

`Max (16 V) CDB Value` field – This is the maximum, or full-range, value for the input in V dc (typically 16.0 V dc) used to scale the input signal prior its value being written into the control signal database.

Chapter 8 Troubleshooting

Introduction

This chapter provides information to help detect and correct problems with the Mark V LM controller but will not cover troubleshooting the turbine, the operator interface, or the site specific process. It is organized as follows:

As shown, this chapter is organized into four primary sections:

General Troubleshooting. This section covers general troubleshooting areas that can be applied to several different problem types. General problems may include fuse failures, repetitive board failures, and Stage Link communication failures.

I/O Core Troubleshooting. This section covers basic troubleshooting areas that can be applied to an unhealthy I/O core. I/O core troubleshooting is generally required when one particular core or board will not communicate with the system. In the case of the <R1> core, this includes the TCEA boards in the <P1> core and the TCDA board in the <Q11> core. The <R5> core includes the TCDA board in the <Q51> core. If a <Q21> core is installed, the <R2> core would include its TCDA board.

Control Engine Troubleshooting. This section covers basic troubleshooting for the Control Engine in the <R> core. Control Engine troubleshooting is generally required when communication is lost between the HMI and Mark V LM controller over the Stage Link.

Diagnostic Alarm Troubleshooting. This section covers basic troubleshooting using the diagnostic alarms on the operator interface. These alarms are core and/or board specific, but may indicate a failure outside the Mark V LM controller. These failures may include external device and wiring failures.

This equipment contains a potential hazard of electrical shock or burn. Only adequately trained personnel who are thoroughly familiar with the equipment and the instructions should maintain this equipment.

Troubleshooting the Mark V LM controller requires the standard tools used when working with electrical equipment. References such as the site-specific hardware document, operator interface document, the Mark V LM controller document, I/O report, and other site-specific documents may be helpful when troubleshooting the controller.

Note All tools and instruments used to touch electrical components should be insulated and grounded to meet National Electrical Code (NEC) standards.

To prevent electrical shock, ensure that all power supplies to this equipment are turned off. Then ground and discharge the equipment before performing any adjustment, servicing, or other act requiring physical contact with the electrical components or wiring.

General Troubleshooting

Table 8-1 outlines some of the general problems and possible solutions that may occur with the Mark V LM controller.

Table 8-1. General Troubleshooting Chart.

Problem	Correction Procedures
1. Fuse Blowing.	1. Compare the fuse size with the Renewal Parts List. Check that the fuse is the correct size. 2. Check for grounds, especially on external devices such as proximity devices.
2. Repetitive Board Failures.	1. Check all connections on terminal boards. 2. Check that all ribbon cables and plugs are connected properly (for example, not offset by one row or pin, or not inverted). 3. Check that all voltages (incoming ac and dc and internal dc) are correct. 4. Check for moisture. 5. Check for damage caused by airborne chemical contamination.
3. Line Voltage Problems.	1. Check that the power sources are within specifications, per Table 3-1. 2. Check for ac line notches or spikes. 3. Check that the ac line frequency is within tolerance, per Table 3-1. 4. Check that the proper connector plugs are in place in the <PD> core. 5. Check that the ac and dc wires are landed on the appropriate terminations.
4. Unable to obtain a Ready to Start.	1. Is the Mark V LM in the proper operate mode (for example Auto). 2. Check the Control Sequence Program (CSP) for what is inhibiting the ready to start. 3. Check all hardware jumpers per the site specific hardware jumper screen on the operator interface. 4. Check all I/O Configuration screen information. 5. Check communication link between the operator interface and the controller. 6. Re-compile and re-download software and re-boot the operator interface and the controller.
5. Turbine speed is incorrect.	1. Check the I/O Configuration for the turbine speed setting. 2. Check any related Control Constants. 3. Check the Big Block in the CSP for what may be inhibiting the proper speed. 4. Re-compile and re-download software and re-boot the operator interface and the controller.

Problem	Correction Procedures
6. Stage Link is not functioning.	1. Check connections between the operator interface and the controller. 2. Check the ARCNET address settings on the operator interface and the controller. 3. Check that the cable meets specifications. 4. Check the cable for failure. 5. Check that a 93 ohm termination resistor is installed at the end of the Stage Link. 6. Check the operator interface for the appropriate ARCNET board used and internal configuration. 7. Try the other BNC connector on the AAHA board. 8. Verify that the Stage Link topologies are correct. See Chapter 10.
7. Erratic Operation.	1. Check connections on all ribbon cables. 2. Tighten all connections on terminal boards and all power connections. 3. Confirm correct hardware jumper settings. 4. Confirm correct I/O Configuration settings. 5. Check related Control Constant parameters. 6. Check for a noisy ground connection. 7. Check CSP. 8. Check external devices for proper operation. 9. Re-compile and re-download software and reboot the operator interface and the controller.
8. Suspected Wiring Problems.	1. Check if the wire sizes meet specifications. 2. Check that the control/signal wires do not run in the same conduit or run parallel closer than 4 inches to the power wires, causing noise pickup. 3. Check that all signal wires are twisted-pair, shielded and that shields are grounded at the controller end only. 4. Check that signal wires are not grounded at more than one end or other than the controller end only. 5. Check that there is only one system ground.
9. Suspected Power Supply Problems.	1. Check the power supply boards (TCPS) using the appropriate test points. (See Table 3-2.) 2. Check the power supply voltages on the TCEA boards using the appropriate test points. (See Table 3-2.) 3. Check the ac and dc voltages in the <PD> core using the appropriate test points. (See Table 3-2.)

I/O Core Troubleshooting

An I/O core that is unable to communicate with the HMI, <R> core, or external devices, is considered to be an unhealthy I/O core. After being rebooted or powered up, the I/O boards will progress through various I/O states, starting from an A0 and ending at A7 if the initialization is successful. All I/O boards contained in or associated with a core must each reach I/O status A6 after being powered up before the I/O Engine for that core will go to I/O status A7. When problems arise, usually only I/O states less than A7 will be indicated; however, three additional I/O states are also possible – A8, A9, and AA. These states are summarized in Table 8-3. The I/O states can be viewed using the TIMN function. Refer to the *TIMN (Terminal Interface Monitor)* section of this chapter for more information.

When troubleshooting a core which has failed to reach I/O status A7 after being powered up, the I/O board(s) which are preventing the core from reaching A7 must first be determined. This section describes the procedure to troubleshoot an I/O core, which has failed to reach I/O status A7 either after an I/O board has been replaced, I/O Configuration software EPROMs have been changed, or during initial controller start-up activities.

Whenever software is downloaded to the controller, the controller must be rebooted in order for the changes to be copied into the associated RAM where it will become effective. All of the associated core I/O boards will be rebooted when the core is rebooted, with the exception of the TCEA boards. See below.

When downloading TCEA I/O Configuration Constants or after changing TCEA hardware jumper settings, it is necessary to re-boot/initialize the TCEA boards individually for the changes to become effective. This is necessary because the TCEA boards are not re-booted/initialized when their associated core is re-booted because they have their own power.

Note If new TCEA I/O Configuration Data is downloaded or hardware jumper settings on the TCEA boards are changed each TCEA must be re-booted/initialized. Toggling the TCEA boards' 125 V dc power supply switch on the TCPD board in the <PD> core is the preferred method of re-booting/initializing the TCEA boards. Re-booting the <R1> core does NOT re-boot/initialize the TCEA boards.

TIMN (Terminal Interface Monitor)

The terminal interface monitor (TIMN) is a software program in the Mark V LM controller. Although typically used by factory personnel, certain program functions can assist customers in troubleshooting hardware and software problems. Using a laptop or other suitable computer terminal (one that is equipped with a telecommunications software package), it is possible to access TIMN through the RS-232C Serial 9-pin connectors located on the I/O terminal boards of the I/O cores (QTBA or CTBA terminal boards). TIMN does not work for the <R> core; however a system called MON_SYS will. It uses the same type of serial communication link as TIMN and is described in the next section of this chapter.

Connecting the RS-232C serial port and the serial port of the computer can be done with a *straight through* serial cable that requires a null modem for proper communication, or a specially made cable with two DB-9 connectors (if the computer has a DB-9 serial port). This type of cable would eliminate the need for a null modem. Three connections are required on the special cable: pin 2 to pin 3, pin 3 to pin 2, and pin 5 to pin 5.

Note Only one CPU can be connected to an individual controller board at a time; multiple connections are not possible.

Figure 8-1. Pinout connections for DB-9 TIMN Interface Cable

A communication software package or computer terminal using the above communications configuration can access the TIMN program. The link configuration requirements are:

- Baud rate in bits/second 9600
- Data bits 8
- Parity NONE
- Stop bits 1
- Flow Control (if required) Xon/Xoff
- Connect (if using HMI) COM2
- Emulation (if required) VT100
- Back Scroll (if required) 500 (suggested)

To activate the TIMN editor, press CTRL-Z from the communication software. The screen displays the program version, the core in which the connection was made, and the time/date of the Promset release. The current time and date is also displayed. User options available in TIMN are summarized below.

TIMN Help Function

Type H at the # prompt to get help on the commands available in TIMN as shown below:

```
#H
User help; * indicates that remaining characters in that word
are optional:
Type 'D*ebug ' to enter the DEBUG monitor.  (Factory use only)
Type 'S*tatus to display agent status.
Type 'U*pdate for continuous Status display.
Type 'H*ELP' for HELP menu.
Type CTRL_Z, EX, or Q to EXIT.
Type 'FMS' to enter Fuel Metering System
```

TIMN Update Function

Type U at the # prompt to get help on the commands available for on line monitoring in TIMN as shown below:

```
#U <letter from list below>
```

Enter selection:

A: = ARCNET counters

B: = BMS qst entries

C: = Counters

D: = Dpm

E: = System errors

F: = File Dates

I: = I/O status

L: = Frame logging

M: = Memory tables

Q: = Quit/Exit

R := BMS qst summary

S: = BMS sockets

U: = Update command

V: = Voter Status

X: = Quit/Exit

Y: = Sync Info

Z: = Zero counters

TIMN Fuel Metering System Monitor Function

Type FMS at the # prompt to get to the FMS> prompt. The notation <d> is the FMVED motor controller channel number, which is 1, 2, 3 or 4. Help on the commands available for the FMVED system monitoring in TIMN is shown below:

```
#fms
Fuel Metering System terminal interface.
Type 'H' for help.
Drive 1 is unused, configured, off-line, not downloaded, and
not under test.
Drive 2 is unused, configured, off-line, not downloaded, and
not under test.
Drive 3 is unused, configured, off-line, not downloaded, and
not under test.
Drive 4 is unused, configured, off-line, not downloaded, and
not under test.
FMS>h
H       HELP            This display.
E  <d>  ERRORS          Display real-time errors for drive <d>.
CE <d>  CLEAR ERRORS    Clear real-time errors for drive <d>.
L  <d>  LOGS            Display latest logs for drive <d>.
```

```
CL <d>  CLEAR LOGS      Clear logs for drive <d>.
W  <d>  WATCH           Continuously watch log entries for
drive <d>.
M  <d>  MONITOR         Monitor real-time data for drive <d>.
MT <d>  MONITOR/TRIGGER Same as above but triggers on unusual
events.
S       STATUS          Show general status of FMS hardware.
T  <s>  TERM            Enter ASCII terminal mode through
serial port <s>.
Q       QUIT            Exit FMS terminal interface.
Note: L, CL, and W with parameter 0 operate on the general log.
```

TIMN Status Function

Type S at the # prompt to get to the Status> prompt. Help on the commands available for I/O Engine status is available by pressing **Enter** at the Status> prompt in TIMN as shown below:

```
#S
  ----- Agent Status -----
Status>
  --- bad option ---
  Enter selection:
      A := Arcnet counters
      B := BMS qst entries
      C := Counters
      D := Dpm
      E := System errors
      F := File Dates
      I := I/O status
      L := Frame logging
      M := Memory tables
      Q := Quit/Exit
      R := BMS qst summary
      S := BMS sockets
      U := Update command
      V := Voter Status
      X := Quit/Exit
      Y := Sync Info
      Z := Zero counters
```

Practical Use of TIMN Update Function

To obtain I/O status information, press **U**, **space**, **I,** then **Enter**. The screen will display several columns of information. The columns of most interest in the I/O status display of TIMN are the board name, major revision (maj rev), minor revision (min rev), I/O states (I/O Stat), and configuration status (cfg stat). Asterisks in the board name column indicate that the board is being enabled by the I/O Configuration download but is unable to communicate/be communicated with the associated I/O core. If asterisks are being displayed for a board that should be enabled, check all the ribbon cables and wire harnesses associated with the board. If the board should not be enabled, check the I/O Configuration Editor Configuration Menu for the board's core and ensure the board is disabled (purple background). If the board was enabled but should not have been, disable it in the I/O Configuration Editor, save the changes, and re-download to the Mark V LM, performing a hard re-boot of the core or board after the download.

Values in the major and minor revision should agree with the I/O Configuration Editor. If not, refer to the *TIMN Help Function* section of this chapter.

The last column to check is the cfg stat column. The hexadecimal code *D0* should be displayed in the cfg stat column for all boards which have the I/O status A7. Configuration status codes other than *D0* should only be shown for boards with an I/O status other than A7. Table 8-2 shows configuration status information for each code which might appear in the cfg stat column.

Table 8-2. TIMN I/O Status Cfg Stat Column Codes

Configuration Status Code	Code Meaning	Status
00	Unable to communicate with board.	Valid
C0	I/O Configuration in progress.	Valid
C1	No BMS socket for configuration message.	Valid
C2	EEPROM image has not been downloaded.	Not Valid
C3	EEPROM image has an invalid voter ID.	Not Valid
C4	LCC board does not conform to network.	Not Valid
C5	EEPROM missing Stage Link ID	Not Valid
C6	BMS type mismatch on a configuration message.	Valid
C7	BMS sequence number mismatch on a configuration message.	Valid
C8	Configuration message returned a bad status.	Valid
C9	Configuration message not received in 10 seconds.	Valid
CA	Download and actual PROM revision levels do not agree.	Valid
D0	Configuration completed successfully.	Valid

I/O configuration status 00 indicates that the board is not communicating or cannot be communicated with the associated I/O core. Check both ends of the ribbon cables and wire harnesses attached to the board. Also check for bent/broken pins on socketed microchips on the board and for proper orientation of the socketed microchips.

I/O configuration status CA indicates that the actual PROM revision levels, the downloaded PROM revision (as entered into the I/O Configuration Editor and downloaded to the Mark V LM) and/or the board's configuration file major revision levels do not agree. The actual PROM revision levels for the board are shown in the *maj rev* and *min rev* columns on the TIMN I/O Status display on the computer/terminal. Compare these levels against the levels entered in the I/O Configuration Editor and refer to the *TIMN Help Function* section of this chapter.

Contact GE Industrial Systems - Product Service (see *How to Get Help* in Chapter 1) for support and information if a configuration status other than those detailed in this procedure is displayed when using the TIMN function.

Checking I/O Status and PROM Revision Level

The board with the lowest I/O status should be the first board to troubleshoot. Table 8-3 is a list of the possible I/O states with a brief description of the status codes.

Table 8-3. Mark V LM Board I/O State and Status Meanings

I/O States	Status Code Description
A0	i80186 started cold start init. Processor initializes its half of the dual ported memory.
A1	i80196 started cold start init. Initializes its half of dual ported memory, if successful go to status A4.
A2	i80196 not responding - warm start requested. 80196 losses synchronization with the 80186. The 80196 should re-initialize and return to state A4.
A3	i80186 not responding - warm start requested. 80186 losses synchronization with the 80196. The 80186 should re-initialize and return to state A4.
A4	BMS/dual ported memory is being initialized, communication channels tested and checks of ARCNET addresses for the Stage Link and COREBUS.
A5	i80186 is being configured via BMS messages. Checks all I/O configuration, current revisions, and dual ported memory.
A6	Board is performing only input functions. All boards need to reach A6 before any can reach state A7. If a board looses state A7, the other boards stay at A7 while the suspect board re-initializes and attempts to return to state A7.
A7	Board is performing normal I/O operations/functions.
A8	Cold start init error detected. I/O board does not match type specified in configuration file.
A9	Board not included in I/O Configuration (but required). Failure when no I/O board is present.
AA	Board in quality control test mode.

During the normal sequence of powering up, the I/O boards pass through the first I/O States and all reach a state of A7. A failure during the power-up sequence or during operation causes the core to return to states A2 (80196 failed) or A3 (80186 failed). I/O states less than A7 but more than A4 are usually indicative of improper I/O Configuration software PROM revision levels entered into the I/O Configuration Editor for that board or an improper I/O board configuration file present in the unit-specific PROM subdirectory on the operator interface. To begin the process of comparing the actual I/O Configuration software PROM revision levels against the downloaded PROM revision levels, use the Card Identification program on the operator interface (see the appropriate documents), the TIMN function, or check the PROM chip labels on the EPROMs themselves to find out the actual revision levels of the I/O boards EPROMs. To do this, each alpha character corresponds to its associated numeric character. For example AE = 1.5. To determine the downloaded I/O Configuration software PROM revision levels, enter the I/O Configuration Editor on the operator interface and select the appropriate core and I/O board.

Confirm that the actual PROM revision levels match the I/O Configuration Editor. If the minor revisions do not agree, change the revision levels on the I/O board's I/O configuration screen to match the actual revision level. Save the changes, exit and download to the controller, performing a hard re-boot of the core/board.

If the major revision levels of the EPROMs are different (the major revision is the 5 of revision 5.2), check the I/O boards configuration file in the unit-specific PROM subdirectory of the operator interface. The I/O_CFG.DAT file will list which configurtion file each board uses. For example, the TCCA board may use the TCCA_CFG.DAT. If the highest major revision level specified in the I/O board's configuration file header does not matches the major revision level of the EPROM installed on the board this means that the latest board configuration file is NOT present in the PROM subdirectory.

For example, if the latest entry in the header of a board's PROM subdirectory configuration file indicated revision 4.1 and the PROM labels indicated revision 5.1, a new board configuration file must be obtained and copied to the PROM subdirectory. New PROM subdirectrory board configuration files should have been sent to the site and copied to the operator interface if new PROMs were sent to the site. Check to see that the new I/O board configuration file for the new PROM was copied from the distribution disk to the unit-specific PROM subdirectroy on the operator interface; if not, copy the new file to the operator interface hard disk and continue with the procedure. The time/date file specifications of the file on the operator interface and the file on the distribution disk can be compared to determine if the distribution disk's file exists on the operator interface. A decompression program may be required to extract and decompress the file from the distribution disk; contact GE Industrial Systems - Product Service for assistance, if necessary.

After the new board configuration file is copied to the PROM subdirectory, the user must run the I/O Configuration Editor and produce new I/O Configuration Printout and Parameter files by clicking on the *List Screens* and *List Parms* targets for each core. Exit the I/O Configuration Editor and print out the I/O Configuration list files. Return to the I/O Configuration Editor and select the I/O core and the I/O board and select the *Default Card* target, answering the prompt by pressing *Y*. Clicking on the *Default Card* target will cause the I/O Configuration Editor to use the new I/O board configuration files as well as its default I/O Configuration Constants overwriting the unit-specific I/O Configuration Constants. For this reason, the unit-specific I/O Configuration Constants from the I/O Configuration list files must be manually re-entered into each and every field of each screen of the defaulted I/O board. Remember to click on the *Verify Screen* target after re-entering the information on each screen. When finished re-entering unit-specific I/O Configuration constants, select list parms and list screens and save the information, exit and download to the controller, performing a re-boot/initialization of the core/board. Print out the new I/O Configuration lists.

Checking I/O Network

The next item to check is the position of the IONET termination resistor hardware jumpers and IONET address hardware jumpers if the problem board is either a TCEA or a TCDA.

Caution

If it is necessary to change IONET termination resistor and/or IONET address jumpers on the TCDA board, power down its associated core before doing so. To change IONET termination resistor and/or IONET address hardware jumpers on the TCEA boards, remove the power to the board before changing the jumpers.

The core drawings on the site specific hardware document can help to determine the actual IONET of the application. The <R1> core's IONET daisychains from the TCQC board with the TCEA boards in the <P1> core and then to the TCDA board in the <Q11> core. The <R5> core's IONET daisychains from the CTBA terminal board with the TCDA board in the <Q51> core. The IONET terminates at the last I/O board of each IONET by placing the IONET termination resistor hardware jumper on the board in the *IN* position. The IONET termination resistor hardware jumpers of any intermediate I/O board must be in the *OUT* position for proper operation. If the IONET termination resistor hardware jumpers are correct for each IONET, check the IONET addresses. If the IONET termination resistor hardware jumpers are not correct, power down the core/board, change the hardware jumpers and power the core/board back up. See Appendix A or the on-line hardware jumper screen on the operator interface for more information on the correct hardware jumper settings.

Check the IONET address hardware jumpers of the TCEA boards and TCDA boards. The TCEA boards must each have unique IONET addresses that are set by their own IONET address hardware jumpers. The IONET address for <X> must be 4, <Y> must be 5 and <Z> must be 6. The hardware jumpers each have a value equal to a power of 2 when the hardware jumper is placed in the *1* position. The IONET address hardware jumpers for each TCEA board should be set so that the sum of their values equals the IONET address required for that particular board. The TCDA board in the <Q11> and <Q51> cores will also have IONET addresses which are set by hardware jumpers. See Appendix A or the site specific hardware jumper screens on the operator interface for the correct IONET address hardware jumper settings.

Check the IONET cable for proper connections and defects. Contact GE Induatrial Sstems - Product Service for support and information if all the above efforts have failed to resolve the problem and the core will not obtain a status of A7.

Control Engine System Monitor (MON_SYS)

The Control Engine Monitor function is similar to the TIMN interface to the I/O Engines. A serial cable is connected to the COM1 port of <R> in location six. The communication settings are the same as those for TIMN, described in the *TIMN (Terminal Interface Monitor)* section of this chapter. This function is also called MON_SYS.

Striking any key, other than those described below, while in MON_SYS will generate a Control Engine Idle Time display and an informational message to the user that the *?* command will provide a directory of all valid MON_SYS commands.

MON_SYS reports approximate times associated with processes in the Control Engine. Actual interrupts are not used so control timing is undisturbed. Select any one option below. Lower case options display once only. Upper case options repeat every 3 seconds. Press any key to stop a repeating display.

```
-OPTION-      ----------ACTION----------
 i or I       Display IOXFR input status
 l or L       Display Corebus Link status
 n or N       Display NVRAM
 o or O       Display SysROM data
 p            Spawn shell prompt if not in A6 or A7  (inhibits CPU state
transitions)
 s or S       Display running segments
 t or T       Display SysRAM data (schedule time, time sync, CE status)
 u or U       Display all possible segments
 x            Display SysRAM Process Table
 z or Z       Display I/O Packet Received Table
 ?            Display this menu
```

MON_SYS I/O Transfer Input Status

A *1* in the Used column indicates that the packet is actually being transmitted. <R0> is the same as <R> in MON_SYS. The output below is normal for a properly functioning Mark V LM controller, since:

There are no slow packets in <R>. The fast packets are from UCIB to LBC586P.

There are no packets in <R4>, since there is no <R4> core in the controller.

There are no fast packets in <R5>.

Critical I/O Flag: 0x1

```
---- I/O status of Possible Cores ---
<R0> FAST Used:1 Crit:1 Actv:1 ACnt:0082 ICnt:0000 Miss:0 MCnt:0
<R0> SLOW Used:0 Crit:0 Actv:0 ACnt:0000 ICnt:0000 Miss:0 MCnt:31999
<R1> FAST Used:1 Crit:1 Actv:1 ACnt:0046 ICnt:0000 Miss:0 MCnt:0
<R1> SLOW Used:1 Crit:1 Actv:1 ACnt:0045 ICnt:0000 Miss:0 MCnt:0
<R2> FAST Used:1 Crit:1 Actv:1 ACnt:0045 ICnt:0000 Miss:0 MCnt:0
<R2> SLOW Used:1 Crit:1 Actv:1 ACnt:0064 ICnt:0000 Miss:0 MCnt:0
<R3> FAST Used:1 Crit:1 Actv:1 ACnt:0045 ICnt:0000 Miss:0 MCnt:0
<R3> SLOW Used:1 Crit:1 Actv:1 ACnt:0047 ICnt:0000 Miss:0 MCnt:0
<R4> FAST Used:0 Crit:0 Actv:0 ACnt:0000 ICnt:0000 Miss:0 MCnt:31999
<R4> SLOW Used:0 Crit:0 Actv:0 ACnt:0000 ICnt:0000 Miss:0 MCnt:31999
<R5> FAST Used:0 Crit:0 Actv:0 ACnt:0000 ICnt:0000 Miss:0 MCnt:31999
<R5> SLOW Used:1 Crit:1 Actv:1 ACnt:0015 ICnt:0000 Miss:0 MCnt:0
```

MON_SYS COREBUS Link Status

A *0x1* indicates that the core is communicating on COREBUS. The output below is normal for a properly functioning Mark V LM controller, since there are no <S> and <T> cores in the controller.

```
** Corebus Link Status **
VOTING --  R : 0x1  S : 0x0  T : 0x0
LINK ----  R1: 0x1  S1: 0x0  T1: 0x0
           R2: 0x1  S2: 0x0  T2: 0x0
           R3: 0x1  S3: 0x0  T3: 0x0
           R4: 0x1  S4: 0x0  T4: 0x0
           R5: 0x1  S5: 0x0  T5: 0x0
```

MON_SYS Non-Volatile RAM Status

The output below is normal for a properly functioning Mark V LM controller four accumulators configured and has been powered up 62 times since the NVRAM was installed. The memory offsets may vary with different software releases.

```
Number of entries  = 4
Power-Up Counter   = 62
TOTD offset     = 0x10
TOTT offset     = 0x33c
FMV offset      = 0x85c
```

MON_SYS Read-Only Memory Status

The output below is normal for a properly functioning Mark V LM controller, since:

L indicates a Mark V LM controller

S indicates a Simplex controller

Frame Rate for a Mark V LM controller must be once every 10 milliseconds

```
** SysROM data **
product    L
type       S
frame rate 100 Hz
```

MON_SYS Command Prompt Enable

The command prompt may only be enabled before the Control Engine reaches the A6 or A7 I/O State. It will provide the user with a # prompt that will allow the user will be able to enter QNX commands. To determine the usage of a command, type:

```
# use <command>
```

MON_SYS Running Segment Status

A segment corresponds to a sequencing source file that has been compiled into the SEQ.AP1 file and downloaded to the Control Engine. The output below is normal for a properly functioning Mark V LM controller with 8 segments running with offset=0:

```
** Running Segment data **
* Segment  0 Running *  rate    0.000 hz  Total bids 27133153
* Segment  5 Running *  rate    0.000 hz  Total bids 6783289
* Segment  6 Running *  rate    0.000 hz  Total bids 13566577
* Segment  7 Running *  rate    0.000 hz  Total bids 27133153
* Segment  8 Running *  rate    0.000 hz  Total bids 27133153
* Segment 13 Running *  rate    0.000 hz  Total bids 27133153
* Segment 14 Running *  rate    0.000 hz  Total bids 13566577
* Segment 15 Running *  rate    0.000 hz  Total bids 27133153
Seg  0 :  Ptr 0xc7001  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg  5 :  Ptr 0xc89ca  Mask 0x0003  Offset 0x0000  Time 0.04000  Interval  40
Seg  6 :  Ptr 0xc8b11  Mask 0x0001  Offset 0x0000  Time 0.02000  Interval  20
Seg  7 :  Ptr 0xc8b8d  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg  8 :  Ptr 0xc9275  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg 13 :  Ptr 0xc9514  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg 14 :  Ptr 0xc9561  Mask 0x0001  Offset 0x0000  Time 0.02000  Interval  20
Seg 15 :  Ptr 0xc9598  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
```

MON_SYS Random Access Memory Status

The output below is normal for a properly functioning Mark V LM controller.

```
** Schedule Time data **
Schedule Time:  34963 (5ms)  4 (1ms)
Real Time:   910016127 (sec)  317062 (usec)
Time Delta:  3373 (sec)  -343606 (usec)
Tic Duration:  999937 (nsec)
I/O Packet info: 0x1  CE System Status: 0xa7
Time Server Network: 0x1
Time Server ID:      0x28
Time Server Status:  0
usec Error (behind): -1243
8254 timer interval: 1193.180054
Sync integral:       0.000000
Sync proportional:   0.000000
Sequence Frame Reference:   10
IOXFR Output Reference:     10
IOXFR Work Frame Reference: 10
```

MON_SYS Total Segment Status

A segment corresponds to a sequencing source file that has been compiled into the SEQ.AP1 file and downloaded to the Control Engine. The output below is normal for a properly functioning Mark V LM controller with 19 segments running with the offsets indicated. A value of 0 for Total Bids indicates that a segment is not used.

```
** Unconditional Segment data **
* Segment  0 Running *  rate    0.000 hz  Total bids 27107565
* Segment  1 Running *  rate    0.000 hz  Total bids 6776891
* Segment  2 Running *  rate    0.000 hz  Total bids 423556
* Segment  3 Running *  rate    0.000 hz  Total bids 1694223
* Segment  4 Running *  rate    0.000 hz  Total bids 3388445
* Segment  5 Running *  rate    0.000 hz  Total bids 6776892
* Segment  6 Running *  rate    0.000 hz  Total bids 13553783
* Segment  7 Running *  rate    0.000 hz  Total bids 27107566
* Segment  8 Running *  rate    0.000 hz  Total bids 27107566
* Segment  9 Running *  rate    0.000 hz  Total bids 13553783
* Segment 10 Running *  rate    0.000 hz  Total bids 6776892
* Segment 11 Running *  rate    0.000 hz  Total bids 13553783
* Segment 12 Running *  rate    0.000 hz  Total bids 6776891
* Segment 13 Running *  rate    0.000 hz  Total bids 27107566
* Segment 14 Running *  rate    0.000 hz  Total bids 13553783
* Segment 15 Running *  rate    0.000 hz  Total bids 27107566
* Segment 16 Running *  rate    0.000 hz  Total bids 1694223
* Segment 17 Running *  rate    0.000 hz  Total bids 1694223
* Segment 18 Running *  rate    0.000 hz  Total bids 1694223
* Segment 19 Running *  rate    0.000 hz  Total bids 0
……
* Segment 31 Running *  rate    0.000 hz  Total bids 0
Seg  0 :  Ptr 0xc7001  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg  1 :  Ptr 0xc70b8  Mask 0x0003  Offset 0x0001  Time 0.04000  Interval  40
Seg  2 :  Ptr 0xc7666  Mask 0x003f  Offset 0x000d  Time 0.64000  Interval 640
Seg  3 :  Ptr 0xc7ac3  Mask 0x000f  Offset 0x000b  Time 0.16000  Interval 160
Seg  4 :  Ptr 0xc848d  Mask 0x0007  Offset 0x0007  Time 0.08000  Interval  80
Seg  5 :  Ptr 0xc89ca  Mask 0x0003  Offset 0x0000  Time 0.04000  Interval  40
Seg  6 :  Ptr 0xc8b11  Mask 0x0001  Offset 0x0000  Time 0.02000  Interval  20
Seg  7 :  Ptr 0xc8b8d  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg  8 :  Ptr 0xc9275  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg  9 :  Ptr 0xc938b  Mask 0x0001  Offset 0x0001  Time 0.02000  Interval  20
Seg 10 :  Ptr 0xc944b  Mask 0x0003  Offset 0x0001  Time 0.04000  Interval  40
Seg 11 :  Ptr 0xc94d2  Mask 0x0001  Offset 0x0001  Time 0.02000  Interval  20
Seg 12 :  Ptr 0xc94f3  Mask 0x0003  Offset 0x0003  Time 0.04000  Interval  40
Seg 13 :  Ptr 0xc9514  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg 14 :  Ptr 0xc9561  Mask 0x0001  Offset 0x0000  Time 0.02000  Interval  20
Seg 15 :  Ptr 0xc9598  Mask 0x0000  Offset 0x0000  Time 0.01000  Interval  10
Seg 16 :  Ptr 0xca13e  Mask 0x000f  Offset 0x0005  Time 0.16000  Interval 160
Seg 17 :  Ptr 0xcbeaf  Mask 0x000f  Offset 0x0005  Time 0.16000  Interval 160
Seg 18 :  Ptr 0xcd562  Mask 0x000f  Offset 0x0005  Time 0.16000  Interval 160
Seg 19 :  Ptr 0x0000  Mask 0x0000  Offset 0x0000  Time 0.00000  Interval   0
……
Seg 31 :  Ptr 0x0000  Mask 0x0000  Offset 0x0000  Time 0.00000  Interval   0
```

MON_SYS Process Status

The output below is normal for the Mark V LM Control Engine Program Functions:

```
** Process Table data **
(00) T:C P:27 C:0037 W:0000 I:9292 O:9292 F:0000 Ovr:9292 anetdrvr
(01) T:R P:10 C:0035 W:0000 I:9191 O:9191 F:0000 Ovr:9191 load_con
(02) T:S P:25 C:0054 W:0063 I:0000 O:0000 F:0000 Ovr:0000 ioxfr
(03) T:C P:20 C:0039 W:0000 I:9292 O:9292 F:0008 Ovr:9292 bmsdrv
(04) T:S P:21 C:0064 W:0066 I:0000 O:0000 F:0007 Ovr:0000 timesync
(05) T:S P:18 C:0067 W:0069 I:0000 O:0000 F:0007 Ovr:0000 udmsvr
(06) T:C P:18 C:0041 W:0000 I:9292 O:9292 F:0000 Ovr:9292 msp_exec
(07) T:C P:13 C:0044 W:0000 I:9292 O:9292 F:0000 Ovr:9292 udfsvr
(08) T:S P:22 C:0070 W:0071 I:0000 O:0000 F:0000 Ovr:0000 watchdog
(09) T:C P:11 C:0047 W:0000 I:9292 O:9292 F:0000 Ovr:9292 uciasvr
(10) T:C P:26 C:0048 W:0050 I:9292 O:9292 F:0000 Ovr:9292 seqsched
(11) T:C P:11 C:0049 W:0000 I:9292 O:9292 F:0000 Ovr:9292 diagcsvr
(12) T:C P:14 C:0052 W:0000 I:9292 O:9292 F:0000 Ovr:9292 aecestab
(13) T:S P:14 C:0072 W:0079 I:0000 O:0000 F:0008 Ovr:0000 alm_mgr
(14) T:S P:14 C:0081 W:0088 I:0015 O:0000 F:0008 Ovr:0000 dal_mgr
(15) T:C P:14 C:0053 W:0000 I:9292 O:9292 F:0000 Ovr:9292 digin
(16) T:S P:14 C:0091 W:0092 I:0003 O:0000 F:0008 Ovr:0000 evt_scan
(17) T:S P:19 C:0096 W:0098 I:0003 O:0000 F:0007 Ovr:0000 cmdsvr
(18) T:S P:10 C:0099 W:0100 I:0015 O:0000 F:0008 Ovr:0000 totalizr
(19) T:S P:10 C:0101 W:0102 I:0015 O:0000 F:0008 Ovr:0000 cmdap1wr
(20) T:T P:11 C:0106 W:0107 I:0000 O:0000 F:0008 Ovr:0000 trip_his
(21) T:T P:11 C:0108 W:0109 I:0063 O:0000 F:0008 Ovr:0000 rollavg
(22) T:T P:10 C:0110 W:0111 I:0000 O:0000 F:0008 Ovr:0000 aga8m2pr
(23) T:S P:14 C:0103 W:0104 I:0003 O:0000 F:0008 Ovr:0000 cblrempb
(24) T:T P:03 C:0112 W:0113 I:0001 O:0000 F:0008 Ovr:0000 dbackgnd
(25) T:S P:12 C:0105 W:0000 I:0003 O:0000 F:0007 Ovr:0000 tgenisvr
```

MON_SYS I/O Packet Received Status

A *1* in the FAST or SLOW row indicates that the packet is actually being received. <R0> is the same as <R> in MON_SYS. The output below is normal for a properly functioning Mark V LM controller, since:

There are no slow packets in <R>. The fast packets are from UCIB to LBC586P.

There are no packets in <R4>, since there is no <R4> core in the controller.

There are no fast packets in <R5>.

The phase indicates history over the last 32 samples of data received. A 0 in a row that should normally be populated with 1, indicates that a communication packet was missed by the Control Engine. This would be a cause for concern if there are consecutive zeroes in a row where communications should be taking place.

```
** I/O Packet data **
Kill I/O Status:      0x0000
CSBD Contol Mode:  0x0000
Critical I/O Flag: 0x1
---- I/O packets received ---
   phase                      1 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 2 3 3
          0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R0> FAST 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
<R0> SLOW 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R1> FAST 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
<R1> SLOW 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R2> FAST 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
<R2> SLOW 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R3> FAST 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
<R3> SLOW 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R4> FAST 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
<R4> SLOW 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
<R5> FAST 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
<R5> SLOW 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
          -.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-.-.-.-.=.-.-.-.-.+.-
```

Diagnostic Alarms

Diagnostic alarms inform the user that a particular core or board has an unusual condition. Diagnostic self-tests are run continuously on the cards and software in the I/O Engines and Control Engine. Whenever an abnormal condition is detected, a diagnostic alarm will be displayed. Each diagnostic alarm will display the following information on a single line of the alarm display window:

- Date/time of the alarm occurrence
- Unit (Mark V LM controller) the alarm occurred in.
- A *drop* number
- Short description of condition (not to exceed 40 characters)
- Status of the alarm (logic 1 meaning set or active, logic 0 meaning reset or cleared).
- Whether the alarm has been acknowledged or not is determined by color of lettering on the line

Note Diagnostic alarms should be reported to the proper personnel for investigation and resolution. They serve as an indication of the internal operation of the Mark V LM Controller and as such, should be dealt with promptly to ensure continued availability and reliability of the control system and turbine.

A diagnostic alarm *Help* function is also available to provide an alarm help screen explaining the alarm, possible causes/effects for the alarm and possible solutions. If additional causes or solutions are found, this file, HELP_QD.DAT, may be edited to include them.

Note Before alarms can be reset, they must be acknowledged and the alarm conditions must no longer exist.

The *Diagnostic Alarm* (Process Alarm Drop 0) appears when one or more diagnostic alarms are present. Once all of the diagnostic alarms are resolved, Process Alarm Drop 0 should reset automatically.

Note The diagnostic alarm annunciation on the Process Alarm Display can only be reset, or cleared, from the display when all diagnostic alarms have been acknowledged, resolved, and reset from the Diagnostic Alarm Display.

Note Diagnostic alarms may be a problem external to the Mark V LM controller. Be sure to check all terminations and external devices prior to assuming that a board has failed.

The troubleshooting/maintenance tools on the operator interface may assist in pinpointing the cause of the alarm. TIMN may also be used to diagnose any communication or board failures in the I/O Engines.

Notes

Chapter 9 Parts Replacement

Introduction

This chapter provides instructions for replacing printed wiring boards and EPROMs, information needed when ordering spare and renewal (replacement) parts, and warranty information.

GE tests all equipment before shipping, and does not expect equipment failure under normal conditions. Most components never require repair or replacement.

Warning

Disconnect all power supplies before performing any maintenance, adjustments, servicing, parts replacements, or any act requiring physical contact with electrical working components or wiring of this equipment.

Circuit breakers, if supplied as part of the total system, may not disconnect all power to the equipment. Whether the ac voltage is grounded or not, high voltage to ground may be present at many points.

This chapter is organized as follows:

Replacing Boards

Caution

To prevent component damage caused by static electricity, treat all boards and devices with static-sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation. Store EPROMs in anti-static sleeves or boxes.

Printed wiring boards may contain static sensitive components which must be considered when handling and replacing a board. GE ships replacement boards in anti-static bags or boxes. It is important that they be stored and transported in these bags/boxes when not installed in the system.

Caution

While power is applied to the board/core, do not remove printed wiring boards or connections, or re-insert them. This can damage the equipment.

To replace a board:

1. **Make sure that power to the core is off.**
2. Carefully disconnect cables.
3. Release all hold down tabs, then carefully pull out board.
4. Set all jumpers and switches on the replacement board in exactly the same position as those on the failed board.
5. If the EPROMs from the failed board are **good**, remove the EPROMs using an EPROM removal tool, and install into sockets on the new board, making sure that they are properly aligned.
6. If the EPROMs from the failed board are **damaged**, replacement EPROMs must be ordered if spares are not available.
7. Install new board, making sure that all tabs snap tightly into position.
8. Reconnect all cables, making sure that they are properly seated in the connectors.

Replacing EPROMs

Caution

To prevent component damage caused by static electricity, treat all boards and devices with static-sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation. Store EPROMs in anti-static sleeves or boxes.

Caution

While power is applied to the board/core, do not remove EPROMs or re-insert them. This can damage the equipment.

To replace an EPROM:

1. **Make sure that power to the core is off.**
2. Remove board if needed. Refer to the *Replacing Boards* section in this chapter
3. Verify the revision on the old PROM. The last two alpha characters of the part number on the EPROM represent the major and minor revision levels of the EPROM. Each alpha character represents a number, (A=1, B=2). For example, the last two alpha characters on the EPROM part number DS200DENCG1ABE would translate to major revision 2 (B=2) and minor revision level 5 (E=5), or revision level 2.5.
4. Verify the revision on the new EPROM, as stated above.
5. If the major revision levels are the same and the minor revisions of the new EPROM are the same or higher, remove the old EPROM using an EPROM removal tool. Replace it with the new EPROM, making sure the EPROM is properly aligned. Replace the board if removed.
6. If the major revision levels are different, the I/O Configurator must be updated on the operator interface before changing out the EPROM. GE recommends that a qualified field service representative assist in any EPROM upgrade. This procedure may take approximately 4 to 6 hours and should be performed during a scheduled shutdown. A detailed procedure is typically included in any EPROM upgrade packages. If the procedure is not available, please call GE Industrial Systems Product Service for more information (see *How to Get Help* in Chapter 1). The following is a summary of the procedure:
7. Before powering down the Mark V LM controller,
   a. Back up the unit-specific directories and files on the operator interface.
   b. Copy the new unit-specific files accompanying the EPROMs onto the operator interface.
   c. Manually update the appropriate information in the I/O Configuration files.
   d. Check the unit-specific files to ensure that Control Constants and I/O Configuration Constants have not changed.
   e. Download the new configuration information to the Mark V LM controller.
   f. Shut the Mark V LM controller down.
   g. Change the EPROMs, using an EPROM removal tool.

h. Power the Mark V LM controller back up.

i. Verify that the processors are all communicating.

8. If the minor revisions are different, update the I/O Configurator screen for that board with the new EPROM revision levels, save, redownload I/O Configuration to the controller, and re-boot.

For detailed description of the EPROM upgrade process, please contact GE Industrial Systems Product Service (se *How to Get Help* in Chapter 1).

Preventive Maintenance

Because the Mark V LM controller has few moving parts, minimum preventive maintenance is required. Periodic maintenance is recommended.

Warning

The equipment contains a potential hazard of electrical shock or burn. Only adequately trained personnel who are thoroughly familiar with the equipment and the instructions should maintain the equipment.

Preventive maintenance helps prevent, detect, and correct conditions that could cause equipment malfunction. It includes inspections for damage and wear, and cleaning of equipment at regular intervals.

The schedule for preventive maintenance depends largely upon the environmental conditions around the equipment. As a guide, it is suggested that preventive maintenance be performed at least once every two months in bad environments, and on scheduled shutdowns in good environments.

The following functions should be performed at regular intervals:

- Turn off power to the equipment to be inspected and maintained. Test equipment using multimeter to ensure power is off.
- Using a vacuum cleaner with a non-metallic nozzle or low-pressure dry compressed air, remove dust and dirt from cabinets and electrical components.

Caution

Do not use high-pressure compressed air to remove dust and dirt, as this may damage components.

- Inspect all cabinet air filters, if equipped. Shake filters clean or replace, as required.
- Check tightness of all electrical and mechanical connections. Tighten or replace any crimp-style lugs that have loosened during operation. Tighten or replace all loose or missing hardware.
- Inspect wiring for wear (fraying, chipping, or nicks). Repair minor defects with a good grade of electrical tape, or replace if necessary.
- Inspect printed wiring board plugs, wiring, and connectors to ensure correct seating.
- Inspect fans for correct operation. Ensure that air passages are clear.

Renewal Parts

GE recommends that the customer keep a set of spare parts on hand to minimize down time if repair is needed. GE provides a Renewal Parts List that applies specifically to the equipment furnished on a customer's particular application at the time of shipment.

If the renewal parts list is missing or to obtain warranty replacement parts or service assistance, contact the nearest GE Sales Office, GE Sales Representative or GE Business Associate Sales Representative. Please have the following information ready to exactly identify the part and application:

- GE requisition number
- Controller serial number and model number
- Part number and description

Parts still under warranty may be obtained directly from the factory. The *GE Industrial Systems Terms and Conditions* brochure details product warranty, which includes the warranty period and parts and service coverage. The brochure is included with customer documentation. It may also be obtained separately from the nearest GE Sales Office or authorized GE Sales Representative. When ordering warranty parts, be sure to include the above information.

Part Numbers

A GE part number is structured so that different portions of that number identify the type of equipment and location of manufacture. For ordering, a customer does not need to understand this makeup – the equipment nameplate, and tags on the individual parts provide the complete number. All numbers should be reported to GE when ordering any parts. See Chapter 5 for a description of the printed wiring board's part numbering system. EPROM part numbers also follow the same part numbering system as the printed wiring boards.

Note The factory may substitute later versions of boards based on availability and design enhancements.

Notes

Chapter 10 Stagelink Configurations

Introduction

Communication between the operator interface(s) and the Mark V LM controller(s) is carried out by means of the control system's Stagelink. In its simplest configuration, the Stagelink connects one Mark V LM turbine controller to a single operator interface (or node) across a single segment (see segment definition below). This communication topology may however be expanded to accommodate multiple operator interfaces and/or multiple controllers. For example, a single operator interface can be configured to issue commands to and receive turbine data from up to eight Mark V LM turbine controls. In addition, multiple operator interfaces may be attached to the Stagelink – each operator interface communicating with multiple controllers. In this way, the Stagelink provides enhanced flexibility for establishing effective communications that can be tailored to individual site needs.

The Stagelink was designed specifically to address turbine control needs such as downloading or uploading software between the Mark V LM and the operator interface, issuing commands, alarm management, and monitoring. Distributed control systems (DCS) interface to the Mark V LM via separate communication link(s) routed to the operator interface, typically using a Modbus protocol.

This chapter is organized as follows:

Terms of Reference

This Chapter provides guidance and rules for successfully mapping Stagelinks. Examples are used to help explain how certain topologies maximize communication link availability and/or enhance network distances.

- **NODE** – Any device connected to the Stagelink system that has a valid address; an <R> core (Control Engine) or an operator interface.
- **REPEATER** – Electronic device that receives, amplifies and re-transmits Stagelink signals. The <R> core and a hub are considered repeaters, operator interface's are not.
- **HUB** – For the Stagelink, the hub is a 4-port **repeater** (two coax ports and two fiber-optic ports) for converting electrical signals to or from light pulses for fiber-optic transmission or reception. It can also be used as a repeater to amplify coax signals. It is not considered a node because it does not have an address.
- **SEGMENT** – Any Stagelink section that joins two repeaters **or** connects one repeater to one or more high impedance devices and ends with a terminating resistor. A segment may have multiple taps for high impedance connections to operator interface's.

Stagelink Characteristics

The Stagelink consists of a 2.5 MHz/2.5 Megabit-per-second ARCNET system that uses either fiber-optic or standard RG-62 A/U copper cabling. Either type can be purchased with a variety of insulation systems such as flame retardant teflon or high density polyethylene.

In applications that must meet IEC codes, GE Industrial Systems recommends using armored co-axial cable. These cable types have a metal sheath outer layer that functions as both a mechanical shield and as an electrical conductor that can alleviate lightning induced disturbances on short outdoor runs. This outer layer must be grounded at each building's entrances and exits. Fiber-optic cabling prevents electromagnetic interference and is often a better alternative for long outdoor segments (refer to the *Fiber-Optic Cabling* section in this chapter).

General Specifications

Local area network (LAN) type:	ARCNET
Communication type:	Baseband
Frequency/speed:	2.5 MHz/ 2.5 Mbps
Propagation delay (maximum):	31 µsµ
Maximum network length, based on propagation delay:	6,000 m (19,680 ft)
Repeater nodes:	<R>
Other repeaters:	Fiber-optic hubs
High impedance nodes:	Operator interface

Mark V LM Controller

Within the Mark V LM controller, the ARCNET cable should be connected to the AAHA board, which is located in the <R> core (Control Engine). The AAHA board communicates directly with the <R> core. This data exchange is carried out through the one internal port of a three port repeater; the remaining two ports are for external customer use. Signals entering any one of these three legs are amplified and sent out through the other two. Therefore, a signal entering the first external port will be sent to <R> and re-transmitted on the second external port. Signals entering the internal port will be sent out on both external ports. Should the AAHA board loose control power, a relay de-energizes and connects the two external ports. In this manner, all the other nodes on the Stagelink can continue to function as long as the topology is designed in accordance with the distance rules provided later in this Chapter.

Operator Interface

The operator interface utilizes a single high impedance port that distributes signals in both directions on the Stagelink via a *T* type connector. The ARCNET board within the operator interface receives data by tapping off a portion of signal transmitted on the Stagelink.

Cable Recommendations

Copper Cable

Indoor cable	RG-62 A/U co-axial cable
Outdoor cable	Armored co-axial or tri-axial cable
Connector type	BNC plug (both ends)

Fiber-optic Cable

Cable	Multi-mode with 62.5 micron core/120 micron cladding
Connector type	ST bayonet
Hub power	120 V ac/60 Hz or 240 V ac/50 Hz (customer-supplied)
Hub configuration	Two co-axial ports and 2 fiber-optic ports (four ST type connectors)

If the turbine control application requires a segment too long for a co-axial cable, a fiber-optic cable should be used. For more on fiber-optic installation, refer to the *Fiber-Optic Cabling* section in this chapter.

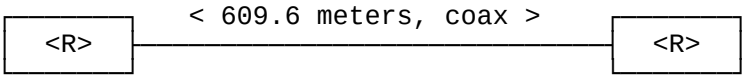
Stagelink Rules

Summary of Topology Rules

No loops	
Maximum number of nodes allowed:	100
Maximum number of operator interfaces in one network:	16
Maximum time delay between any two nodes:	31 microseconds
Both ends of the stagelink must have a 93 ohm terminating impedance	
Every node must have a unique network address	
Maximum segment lengths:	
co-ax repeater to repeater	609.6 m (2000 ft)
co-ax repeater to single operator interface	609.6 m (2000 ft)
co-ax repeater to more than one operator interface	304.8 m (1000 ft)
operator interface between two repeaters	304.8 m (1000 ft)
Maximum operator interfaces per segment:	8
Fiber-optic cable hub to hub (62.5/120 micron fiber):	1825 m (5,987.5 ft)
Minimum cable length between operator interfaces:	1.5 m (4.9 ft)

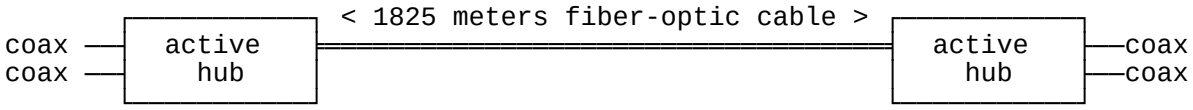
Segment Rules

1. The cable and nodes between two repeaters is called a segment. The segment distance cannot exceed 609.6 meters for a coax connection. Fiber-optic segments can go farther as described below.



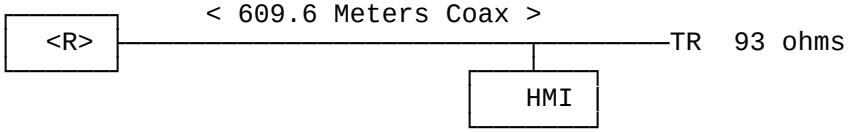
   If an <R> core looses power total length becomes the sum of the two adjacent segments (see rule 8 below).

2. The segment between fiber-optic repeaters can be as much as 1825 meters.

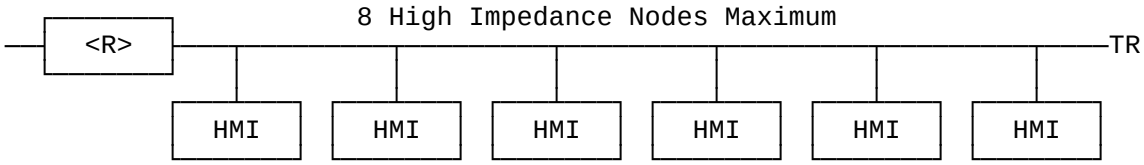


   The typical fiber-optic hub is a 4 port repeater that contains two coax and two fiber-optic ports.

3. A two node segment with one repeater and one high impedance node forming the end of the link may be 609.6 meters long. **The operator interface (shown as *OI*) must have a cable terminating resistor (shown as TR).**

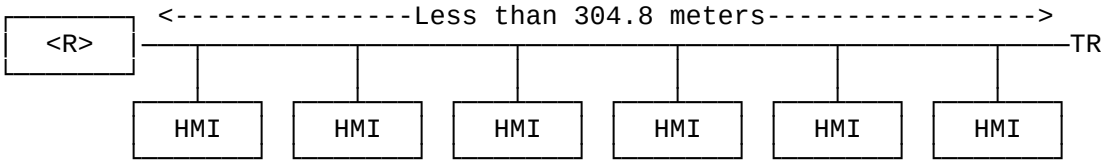


4. No more than 8 operator interface's can be used in one segment. Each node must use a proper *T* connector in the cable to minimize reflection. The *T* is located on the board, and does not have a length of cable between the *T* and the board.

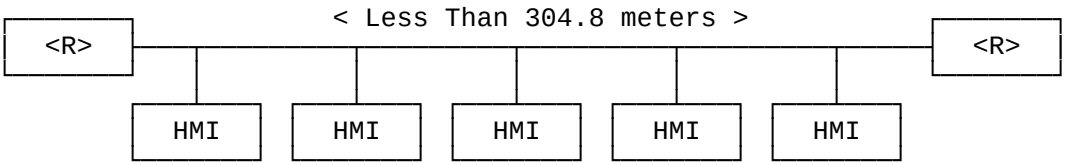


5. High impedance nodes must be separated by a minimum of 1.5 meters of cable between the Ts.

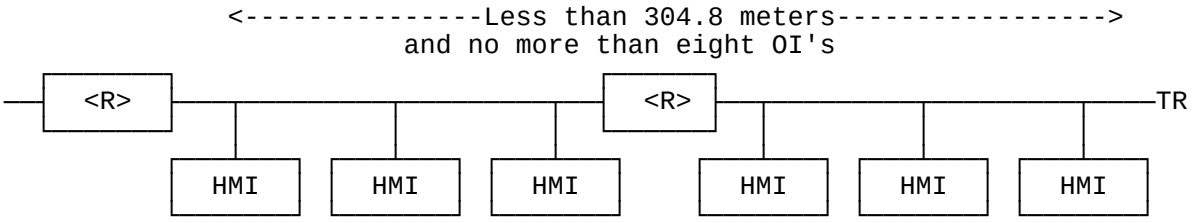
6. On a segment that has one <R> and two or more high impedance nodes, the maximum segment cable distance must be limited to 304.8 meters or less.



7. The length of a segment with two <R>'s, and one to eight operator interface's, must be limited to 304.8 meters or less.



8. Each <R> repeater has a relay that drops out when the power is off, connecting the two ports in order to maintain communication among the remaining nodes. This complicates the distances allowed between nodes because the segment formed by any single failure still must not exceed 609.6 meters. For segments containing operator interface's this distance drops to 304.8 meters.



Total Effective Distance Rules

Always calculate the total *effective cable distance* between the two network nodes that have the longest **effective** distance. This is not always the nodes that are farthest apart physically. Each repeater has a delay equal to the delay in 25 meters of cable. Effective distance is calculated as follows:

Copper (coax) cable length + (Fiber-optic cable length * 1.25) + (number of repeaters * 25 meters)

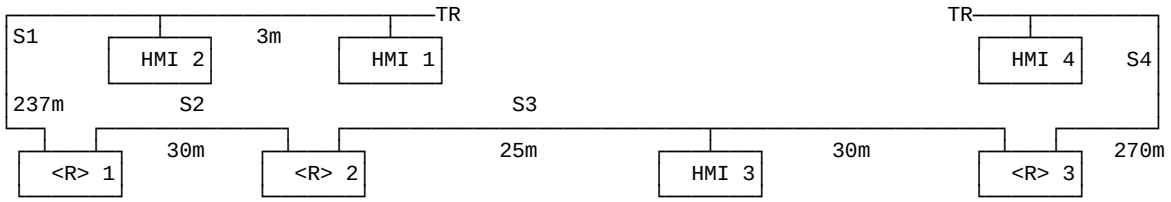
with all lengths in meters

Total *effective cable distance* may not exceed 6000 meters.

The maximum 31 micro second propagation delay is approximately equal to the delay in 6000 meters of cable. As it is easier to calculate *effective cable distance* than it is to measure propagation delay, this approximation is used. The deciding factor is **propagation delay, not total length.** If questions arise about a particular application, it may be necessary to measure the propagation delay.

Examples

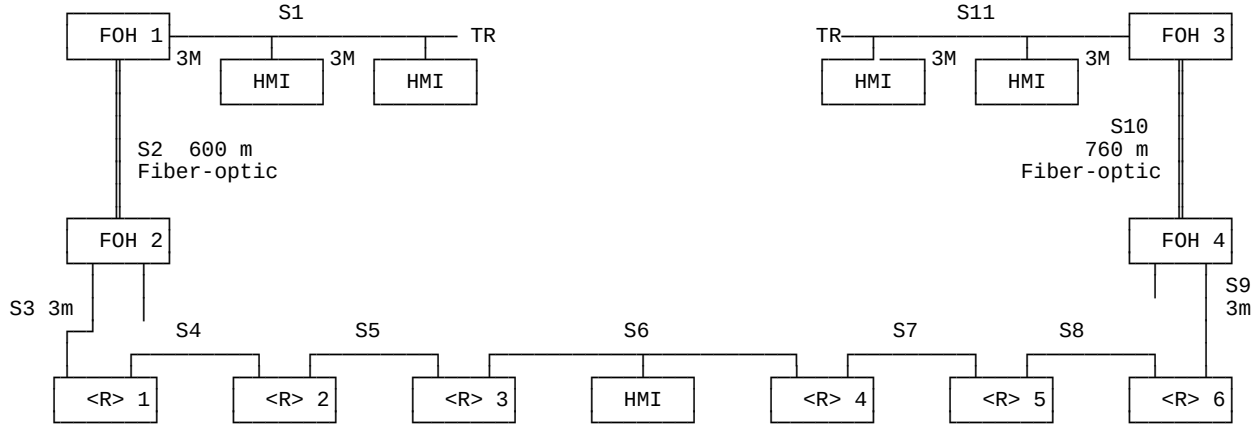
Example 1: A Simple Plant Application



<R> – Communications Processor
HMI – Operator Interface

	Segments				Totals and Comments
	S1	S2	S3	S4	
Cable length, meters:	240	30	55	270	595
Effective cable length:	3 <R>s at 25 = 75, plus 595				670, well below 6000 meter limit
Maximum segment with 1 node failure: Calculations	Failure of node:				*All combined segments have HMIs. Therefore, the maximum is 304.8 meters. <R> 2 to HMI 4 communications will probably fail if <R> 3 fails. One way to avoid this potential problem is to move HMI 3 to the <R> 1 to <R> 2 segment.
	<R> 1	<R> 2	<R> 3		
	Results in combined segment of:				
	HMI1 to <R> 2	<R> 1 to <R> 3	<R> 2 to HMI 4		
	270	85	325*		
Total number of nodes:					7, well below 100 maximum

Example 2: Complex Plant Application



<R> – Communications processor
FOH – Fiber-optic hub
HMI – Operator interface

	Segments											**Total**	
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11		
Fiber-optic cable length:		600								760		1360	
Co-ax cable length:	6		3	30	30	180	30	150	3		6	438	
Max. effective cable length:	(6 <R>s at 25) + (4 FOH at 25) + {1.25 * (600 + 760)} + 438											2388, well within 6000 meter maximum	
Maximum segment with 1 node failure: calculations	Failure of node:												All are less than 609 or 304 maximums.
	<R> 1		<R> 2		<R> 3		<R> 4		<R> 5		<R> 6		
	Results in combined segment of:												
	FOH 2 to <R> 2		<R>1 to <R> 3		<R> 2 to <R> 4		<R> 3 to <R> 5		<R> 4 to <R> 6		<R> 5 to FOH 4		
	33		60		210		210		180		153		
Total number of nodes:							15, much less than 100 maximum						

Fiber-Optic Cabling

Fiber-optic cabling can be an effective substitute for copper coax cabling, especially in cases where longer distances are required, or electrical disturbances are a serious problem.

Advantages

- Larger diameter fiber extends this to 9000 feet (2,740 m) because the light transmitter gets more light into the fiber.
- If the plant is in a high lightning area, fiber-optic segments can reduce the control outages caused by lightning.
- Grounding problems are avoided with optical cable. The ground potential can rise when there is a ground fault on transmission lines, caused by currents coming back to the generator neutral grounding point.
- Optical cable can be routed through switch yards and other electrically noisy areas with no interference. This can shorten the required runs and simplify the installation.
- With proper cable jacket materials it can be run direct buried, in trays, or in conduit, being careful not to drop below the bend radius.
- High quality optical fiber-optic cable is light, tough, and easily pulled.
- The total cost of installation and maintenance of a fiber-optic segment may be less than a coax segment.

Disadvantages

- Fiber-optic links require powered hubs, with a reliable source of ac power. Failure of power to either hub causes a link failure.
- The effective distance of a fiber-optic cable segment is 1.25 times the actual cable routing distance. The rule for Stagelink is that the total effective distance between the farthest apart devices must not exceed 20,000 feet.
- The extra equipment required for fiber links can increase maintenance.
- Cost, particularly for short runs, may be more for a fiber-optic Stagelink segment.
- Inexpensive fiber-optic cable is easily broken during installation and more prone to mechanical and performance degradation over time. The highest quality cable is recommended.

Review of Components

This section will review all of the basic components of a fiber-optic system, including cable, hubs, and connectors.

Basics

The recommended fiber-optic hub accepts two copper coax connections and two fiber-optic links. A message coming in on any one of the four ports is repeated out the other three ports. Each fiber port consists of an outgoing fiber and an incoming fiber. The incoming signal is picked up with a photo transistor and converted to an electrical signal. The outgoing signal is converted from a train of electrical pulses to infrared light using a light emitting diode. On the fiber-optic cable segment the optical output of one hub is connected through the fiber-optic cable to the optical input of the other hub. Two fibers are needed for each segment.

Multimode fiber, with a graded index of refraction core and an outer cladding, is recommended for the Stagelink (see *Cable Recommendations* in this chapter.). The amount of light that gets into the fiber depends on the brightness of the light source and the area of the light carrying portion of the fiber. The amount of light that comes out the other end depends on the clarity of the glass, the distribution of the index of refraction, the condition of the fiber, and the attenuation of connectors. The amount of electrical signal generated depends on the light coming out of the fiber and the area and sensitivity of the photo transistor. Tracking all this is done by using a power budget (refer to the *System Considerations* section in this chapter).

The fiber is protected with *buffering* that is the equivalent of insulation on metallic wires and protects the cable from excessive bends. Mechanical stress can damage fibers. One way to protect the fiber is to spiral it on the inside of a tube filled with gel. A more reliable system uses tight buffering with precision tensioned Kevlar fibers which carry the stress of pulling and vertical runs.

Warning

Never look directly into a fiber. Although most fiber links use light emitting diodes which cannot damage the eyes, some longer fiber links use lasers which can cause permanent damage to the eyes.

Cable

- High quality fiber is recommended, especially for long distance links. It should be 62.5/125 optical cable as well.
- Cable attenuation should be between 3.0 and 3.3 dB/km at 850 nm, and around 1 to 1.2 dB/km at 1300 nm.
- The acrylate protective layer of the fiber should be specified with a 100 kpsi proof test and a 500 micrometer coating, rather than the 50 kpsi and 250 micrometer coating.
- Gel-filled (or *loose tube*) cables should not be used because of the special care required during installation, the difficulty of making terminations and problems of maintaining the gel seal, particularly in vertical runs where hydrostatic pressure can cause gel leakage.
- Use a high quality *break out* cable, which will make each fiber in itself sturdy cable that helps prevent too sharp bends.
- Combine the sub-cables with more strength and filler members to build up the cable for resisting mechanical stress and outside environment attack.

- In the *Specifications* section in this chapter), there are two sample specifications for fiber-optic cable; one without armor and one with armor. Rodent damage is one of the **major** causes of failure of optical cable. If there is a possibility of wire insulation damage from rodents, the armored cable should be chosen. Otherwise, the armor is not recommended because it is heavier, has a larger bend radius, is more expensive, attracts lightning currents, and has lower impact and crush resistance. Particularly for underground runs, a direct lightning strike through the earth to the cable shield can cause explosive formation of steam in damp earth that can mechanically damage the cable.
- Test the optical characteristics of the cable with either an optical time domain reflectometer (OTDR) which can be provided by the manufacturer or with a simpler device that compares light levels at both ends of the cable.
- Four-fiber-optic cables can be used to bring redundant communications to a central control room, or the extra fibers can be retained as spares. A less expensive option is to get the same cable with only two fibers.

Hubs

The type of hub described throughout this chapter is built particularly for ARCNET communications and has the proper impedance to match the ARCNET line (93 ohms). For this reason a fiber-optic cable hub intended for Ethernet, for example, will not function properly on the Stagelink. It consists of a power supply that runs from 120 or 220 volts ac 50 or 60 Hz. The two models can be converted by moving an internal jumper to accept the other voltage in case an error was made in ordering.

The rack contains a power supply with sufficient power for 4 *expansion* boards. Each board has two copper coax ports and two fiber-optic ports. A signal coming in on any port will be amplified and transmitted on the other three ports. Ordinarily only one board is used. If the system uses two fiber-optic cable segments, a second hub is recommended to improve the communications availability. On the board, normally only one copper port and one fiber port are used for the same reason. he fiber-optic ports in the hub's board have ST connectors which are the bayonet type. The light gray is the transmit port, the dark gray the receive port. In service a light gray connector always attaches to a dark gray one.

Connectors

Connectors come in two forms, SMA and ST. The ST connectors give less problems in the field because they ***are*** bayonet type and not subject to over tightening. Over tightening the SMA connector can chip the glass fiber surface causing problems with reflections and loss of transmission. The bayonet type effectively uses a spring to push the two connecting fibers together with the proper force.

Ceramic, glass filled plastic, or stainless steel are used to make the connectors. They come in three standard sizes to fit the different diameter fibers. Connectors for the 62.5/125 micron fiber are relatively easy to procure. The ceramic connectors can be precisely made and match the coefficient of expansion of glass.

System Considerations

Having two operator interface's in the central control room allows one to be down for maintenance while continuing control of the turbines from the control room from the remaining operator interface. Similarly, having two fiber-optic cable segments also allows for failure of one of the hubs, or the power to it. A failure of any one of the copper segments also retains control of all machines.

Often only operator interface's and possibly an <H> (Historian) will be near the central control room. It will have reliable ac, and if that ac is gone, control from that location stops. Therefore, reliable ac in the control room is satisfactory for the hubs as well.

Another system consideration is the optical power budget for the Stagelink. The total budget refers to the brightness of the light source divided by the sensitivity of the light receiver. These ratios of power are usually measured in dB to make calculations easier. The difference between the dB power of the source and the dB power of the receiver represents the total power budget. This must be compared to the link loss budget, which is made up of the loss in the connectors and optical cable. Installation of the fiber can decrease its performance over the new cable condition. The LED light source can get dimmer over time, the connections can get dirty, the cable loss increase with aging, and the receiver can become less sensitive. For all these reasons there must be a margin between the available power budget and the link loss budget of a minimum of 3 dB. A good installation, including using correct parts and cabling, preparing connectors properly, and laying the cable so as to avoid sharp bends and hot locations will help keep availability.

One fiber-optic cable segment is specified to operate as far as 6000 feet with 62.5/125 microns fiber-optic cable, and 9000 feet for the 100/140 microns fiber-optic cable, by the hub manufacturer. These distance limitation have been incorporated into the Stagelink layout rules. It is recommended that fiber-optic sections used in the Stagelink must not be longer than the specified 6,000 and 9,000 feet for the two fiber-optic cable diameters. If the application significantly exceeds these distances another hub must be added to amplify the optical signals.

Installation

- Install the fiber-optic cable in accordance with all local safety codes. Polyurethane and PVC are two possible options for cable materials that might meet local safety codes. See the *Specifications* section in this chapter for some examples of specific cables.
- Proper planning is extremely important. Layout for the level of redundancy needed, cable routing distances, proper application of the distance rules, and procurement of excellent quality hubs, UPS systems, fiber-optic cable, and connectors should all be included in planning the Stagelink.
- Install the system so that it will be strong enough for indoor and outdoor applications, including direct burial.
- Strictly adhere to the manufacturer's recommendations on the minimum bend radius and maximum pulling force.
- Test the installed fiber-optic cable to measure the losses caused by the cable and the connectors. A substantial measured power margin is the best proof of a high quality installation.
- The process of attaching the fiber-optic cable connectors involves stripping the buffering from the fiber-optic cable, inserting the end through the connector, and casting it into an epoxy or other plastic. This typically involves using a kit designed for the particular connector system. After the epoxy has hardened, the end of the fiber must be cut off, ground, and polished.
- The fiber-optic cable hubs need reliable power, and should be placed in a location that will minimize the amount of movement they must endure, yet keep them accessible for maintenance.

Specifications

The following sections provide specification information for Four-Fiber-optic cable with/without Armor, the Fiber-optic Hub, and Fiber-optic connectors.

Four Fiber-Optic Cable without Armor

Optical Cable Corporation Part (or its equivalent): RK920929-A

Fiber-optic cable and buffering:

Fiber-optic cable type:	Multimode
Core diameter:	62.5 microns
Cladding Diameter:	125 microns
Fiber proof test:	100 kpsi
Coating Diameter:	500 microns
Tight buffer diameter:	900 microns
Tight buffer material:	Hard elastomeric; plastic not acceptable.

Numerical aperture: 0.275

Attenuation & Bandwidth	**Attenuation**	**Bandwidth**
850 nm	3.5 dB/km	160 MHz km
1300 nm	1.3 dB/km	500 MHz km

Stripping ability: All layers can be easily removed with commercially available tools.

Sub Cables: Four sub-cables each with one fiber

Fiber strength member:	Aramid yarn
Sub-cable diameter:	2.5 ± 0.125 mm
Sub-cable jacket:	Elastomeric
Color coded:	Standard -- blue, orange, green, and brown

Cable construction: Sub-cables with filler/strength member

Jacket:	Tight bound pressure extruded Flame retardant polyurethane
Color:	Black

Cable:

Cable weight:	65 kg/km
Cable diameter:	8.0 mm
Strength members:	Aramid yarn with individual precise tensioning

Conductivity: No electrical conductors may be used.

Installation:

Min bend radius:	16 cm (when pulling)
Max tensile load:	2200 N
Location:	Aerial, direct burial, or duct
Pulling:	Ordinary cable grips

Operating:

Min bend radius:	8 cm
Max tensile load:	550 N
Temperature:	-40 °C to +85 °C
Immersion:	No damage
Storage:	-55 °C to +85 °C

Test specification: EIA-STD-RS-455 (or equivalent):

Impact resistance:	1500 impacts
Crush resistance:	2200 N/cm
Cyclic flexing:	2000 cycles

Four Fiber-Optic Cable with Armor

Optical Cable Corporation Part (or equivalent): RK920929-A-CST (consists of the same cable as described above, but surrounded with steel tape and polyethylene over jacket)

Fiber-optic cable and buffering:

Fiber-optic cable type:	Multimode
Core diameter:	62.5 microns
Cladding Diameter:	125 microns
Fiber proof test:	100 kpsi
Coating Diameter:	500 microns
Tight buffer diameter:	900 microns
Tight buffer material:	Hard elastomeric; plastic not acceptable.

Numerical aperture: 0.275

Attenuation & Bandwidth	**Attenuation**	**Bandwidth**
850 nm	3.5 dB/km	160 MHz km
1300 nm	1.3 dB/km	500 MHz km

Stripping ability: All layers easily removed with commercially available tools.

Sub Cables: Four sub cables each with one fiber

Fiber strength member:	Aramid yarn
Sub-cable diameter:	2.5 ± 0.125 mm
Sub-cable jacket:	Elastomeric
Color coded:	Standard -- blue, orange, green, and brown

Cable construction: Sub-cables with filler/strength member

Jacket:	Tight bound pressure extruded and flame retardant polyurethane
Color:	Black
Armor:	Steel tape nominal 0.155 mm
Armor overlap:	2 mm, Bonded, corrugations in register.
Over jacket:	Polyethylene 1 to 1.5 mm thick

Cable:

Cable weight:	174 kg/km
Cable diameter:	13.0 mm
Strength members:	Aramid yarn with individual precise tensioning

Installation:

Min bend radius:	26 cm (when pulling)
Max tensile load:	2660 N
Location:	Aerial, direct burial, or duct
Pulling:	Ordinary cable grips

Operating:

Min bend radius:	13 cm
Max tensile load:	532 N
Temperature:	-40 °C to +65 °C
Immersion:	No damage

Storage: -55 °C to +70 °C

Test specification: EIA-STD-RS-455:(or equivalent)

Impact resistance:	50 impacts
Crush resistance:	440 N/cm

Fiber-Optic Hub

The Hub Assembly is typically a metal box with a power supply and board slots. The Stagelink application typically calls for two hub assemblies each with one board. They can be ordered for table or flange mounting, and for 120 or 240 volt application. Moving an internal jumper can reconfigure for the other voltage if a mistake has been made.

Fiber-Optic Connectors

3M™ Connector model 6100 (or equivalent). This ST bayonet type zirconia connector is already filled with a thermoplastic material that is melted for the insertion of the fiber. The installation kit is model 6150A (or its equivalent). The filler is melted, fiber inserted, end cleaved and polished with only one paper. This connector makes fast and reliable connections and is gaining popularity.

Thomas & Betts Connector model 91810–125-2P (or equivalent). ST connector of composite polymer, glass capillary, crimp and polish termination. Filler is a fast drying epoxy. Assembly Polishing Kit model 91000AKP (or equivalent) includes all parts needed and instructions.

Amphenol Connector model 953-101-5010 (or equivalent). ST connector made of glass reinforced polymeric, ceramic ferrule, copper crimp ferrule, and PVC bend relief boot. Termination kit, model 927-100-5000 (or equivalent), includes stripper, curing oven, microscope, crimp tool, snips, polish board, training video. Add on termination kit has a cleave tool, polishing tool, cable preparation template and instructions. Filler is heat-cured epoxy.

Typical Stage Link Addresses

Table 10–1 shows typical Stagelink addresses as assigned by the factory. Any valid two digit hexadecimal number may be used for any Stagelink address except for <G> processor addresses. For information about using a <G> processor for Ethernet Communications with a DCS system, see the operator interface manual. How to assign a new operator interface processor node to an existing Stagelink is described in Chapter 3.

Table 10-1. Stagelink Addresses

Address	Description	
00	00 is reserved for broadcast messages.	
01	Addresses between 01 and the start of the <G> processor addresses are not reserved.	
02		
.		
.		
0F		
10	8th <G> processor	Reserved for communication with customer's DCS via Ethernet
11	7th <G> processor	
12	6th <G> processor	
13	5th <G> processor	
14	4th <G> processor	
15	3rd <G> processor	
16	2nd <G> processor	
17	1st <G> processor	
18	8th operator interface processor	Reserved for operator interface processor addresses.
19	7th operator interface processor	
1A	6th operator interface processor	
1B	5th operator interface processor	
1C	4th operator interface processor	
1D	3rd operator interface processor	
1E	2nd operator interface processor	
1F	1st operator interface processor	
Addresses between 20 and the start of the Communication Core addresses are not reserved.		
EE	.	Reserved for the Mark V LM Communication Core, <R>.
EF	.	
FA	.	
FB	5th Mark V LM	
FC	4th Mark V LM	
FD	3rd Mark V LM	
FE	2nd Mark V LM	
FF	1st Mark V LM	

Notes

Appendix A Hardware Jumpers

Introduction

Hardware jumpers are used to configure Mark V LM hardware (printed wiring boards and printed wiring terminal boards) to meet specific application requirements. The purpose of this appendix is to introduce the specific manner that the jumper customizing process is applied. It is provided in this order:

A hardware jumper consists of a pin, or series of pins mounted perpendicularly to a printed circuit board, and a plastic and metal jumper that can be manually inserted over pairs of pins. When the jumper is placed over two pins a connection is made and the function associated with those pins is enabled. When not in use, a jumper may be stored in proximity to a specific pin arrangement by placing the jumper over only one pin. This does not create a circuit connection, but will be available if a change is necessary.

Warning

Hardware jumpers perform a wide variety of functions. These devices regulate operations such as board frequency, memory storage, overspeed trip settings, and system grounding. Improper application of hardware jumpers can cause significant damage to the system or personnel.

Table Formatting

Tables have been used to show options available. Each table in Appendix A represents a breakdown of hardware jumpers that correspond to a specific printed wiring board (board) or printed wiring terminal board (TB). The tables are listed in alphabetical order.

For boards, tables are divided into five separate columns (see Figure A-1). Reading from left to right, the columns are as follows:

- The first column indexes the board that the table is referencing, such as TCCA or QTBA; the core(s) where the board is found such as <R5>; the location(s) of the board within these core(s) (identical boards may occupy multiple locations within multiple cores); and a board revision number (Rev.).
- The second column gives the number of the jumper being identified.
- The third column defines the position(s) to place a jumper for a specific pin configuration. This category is subdivided into separate listings when an individual pin configuration has multiple functions.
- The fourth column of the table (*Application Notes*) describes the functions of the various pin configurations.

Figure A-1. Table Formatting

ABCD	Jumper	Position		Application Notes
<R1>	J1	**default**	non-default	
Location 1	J2	**default**	non-default	
	J3	**default**	non-default	

Default Setting is a point of reference with regard to a jumper's pin configuration (see *Hardware Jumper Configurations* in this appendix) as it is shipped from the factory. This is done to relate as closely as possible to what is depicted by a board's silkscreen. A default position is **not** to be regarded as an absolute reference. Differing job applications may require jumper settings other than the default position setting.

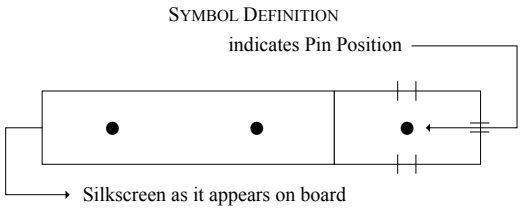
Note The default setting will be boldfaced in the table and will be located in the left position column in a slightly larger font than the rest of the table. Not all jumpers will have a default setting, therefore not all entries in the left position column will be defaults.

Shaded Sections indicate jumper functions that are not designed to be changed or do not vary with the requisition. These jumpers should not be changed.

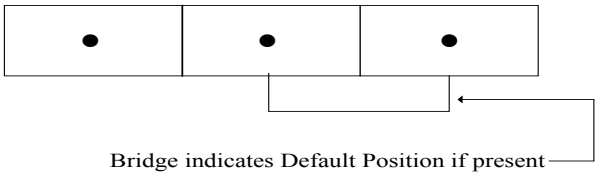
See the board layout figures in Chapter 5 for the locations of the hardware jumpers.

Hardware Jumper Configurations

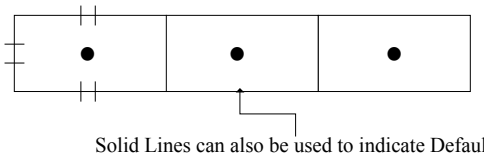
The following hardware jumper configuration examples show printed wiring board silkscreens and jumper positions. The | | should be taken as a symbol of a broken line.



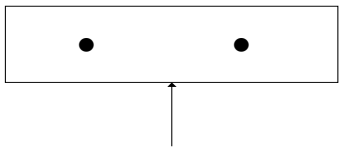
1. Three pin, two circuit:



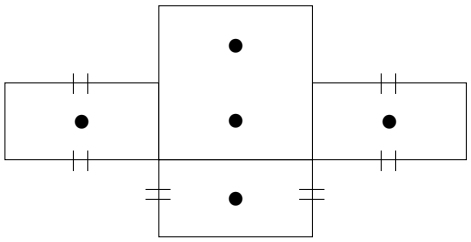
2. Three pin, two circuit:



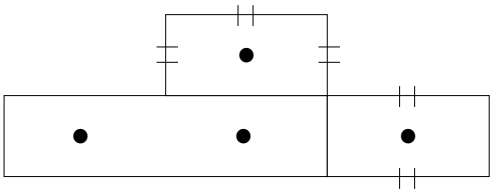
3. Two pin, one circuit:



4. Five pin, four circuit



5. Four pin, three circuit:



Note Board layouts and hardware jumper settings may change with product upgrades and revisions. Site specific hardware jumper settings are located on-line in the operator interface. Any field changes to these settings should be noted on the site specific operator interface hardware jumper screen.

CTBA	Jumper	Position		Application Notes
<R5> Location 6 Rev. CTBAG#A	BJ1 to BJ14	In = connects NEG of mA current inputs to DCOM	Out = mA input is not referenced to DCOM	If the hardware jumper is installed, the NEG terminal of the respective mA input is connected to DCOM. See Connection Examples in Appendix D of this manual
	BJ15	**Default connected**	DCOM not connected	DCOM connection for RS-232C Monitor Port (TIMN)

	Jumper	Isolates Inputs	Position		Application Notes
DTBA Location 6 and **DTBB** Location 7 <Q11>, <Q51>	BJ1	DTBA 1-9 DTBB 47-56	In = Connect +125 V dc Interrogation voltage to Contact Inputs	Out = Disconnect +125 V dc Interrogation voltage from Contact Inputs	Remove for testing only.
	BJ2	DTBA 10–18 DTBB 57-66			Isolates the 125 V dc positive bus from the output wiring to help troubleshoot ground faults on the 125 V dc system.
	BJ3	DTBA 19-27 DTBB 67-76			
Revisions: DTBAG#A and DTBBG#A	BJ4	DTBA 28-36 DTBB 77-86			
	BJ5	DTBA 37-46 DTBB 87-96			See Appendix D, Figure D-41 and Figure D-42 for more information.

	Jumper Pn & Mn	Position		Application Notes
DTBC <Q11>, <Q51> Location 8 Rev. DTBCG#A	1-18	**BOTH** In = Mark V LM supplies power to output. Solenoid Driver Output 1-18 Voltage depends on the application.	**BOTH** Out = "Dry" Contact Output 1-18	**ALWAYS INSTALL JUMPERS IN PAIRS** Install corresponding (Pn & Mn) Jumpers for Solenoid Driver Output. Example: Insert P8 and M8 for solenoid circuit 8. Remove corresponding (Pn & Mn) Jumpers for dry contact outputs. Example: Remove P10 and M10 for dry contact circuit 10. For more details, see Appendix D, Figure D-43.

DTBD <Q11>, <Q51> Location 9 Rev. DTBDG#A	Jumper Pn & Mn	Position		Application Notes
	1-16	**BOTH** In = Mark V LM supplies power to output. Solenoid Driver Output 31-46 Voltage depends on the application.	**BOTH** Out = "Dry" Contact Output 31-46	**ALWAYS INSTALL JUMPERS IN PAIRS** Install corresponding (Pn & Mn) Jumpers for Solenoid Driver Output. Example: Insert P31 and M31 for solenoid circuit 31. Remove corresponding (Pn & Mn) Jumpers for dry contact ouputs. Example: Remove P46 and M46 for dry contact circuit 46. For more details, see Appendix D, Figure D-44.

PTBA <P1> Location 6 Rev. CTBAG#A	Jumper	Position		Application Notes
	BJ1 ALM	In = Enabled	Out = Disabled	Local Audible Alarm Enable Remove to silence alarm.

QTBA <R1>, <R2>, <R3> Location 6 Rev. QTBAG#A	Jumper	Position		Application Notes
	J1	**Default 20 mA**	1mA	0–1 mA on 4–20 mA Input Signal Select Special MW Transducer Input* *See Appendix D, Figure D-18.

STCA <R1>, <R2>, <R3> <R5> Location 1 Rev. STCAG#AA	Jumper	Position		Application Notes
	JP2	**In = enable normal**	Out = disable	Processor Reset Enable = normal operation
	JP4	**1-2 = 5V normal**	2-3 = 12V	5V or 12V power for Flash Proms

TBCB <R5> Location 7 Rev. TBCBG#A	Jumper	Input Circuit	Position		Application Notes
	BJ1 to BJ22	1 to 22	In = connects NEG of mA current inputs to DCOM	Out = mA input is not referenced to DCOM	If the hardware jumper is installed, the NEG terminal of the respective mA input is connected to DCOM. See Connection Examples in Appendix D
	BJ23 to BJ30	15 to 22	In =4–20 mA input	Out = 0–1 mA input	Hardware Jumpers 23-30 modify the current range characteristics of circuits 15-22 (BJ 15-22)

	Jumper	Position		Application Notes
TBQB <R2>, <R3> Location 7 Revision TBQBG#A	BJ1 BJ2 BJ3 BJ4	All In = Fan one input	All Out = one input to each processor	Pressure Input #1 Transducer Configuration*
	BJ5 BJ6 BJ7	In = mA input, 250 ohm burden resistor installed; one for each input.	Out = voltage input, no burden resistor. If BJ1-BJ5 are in, BJ6 and BJ7 **MUST** be out.	Pressure Transducer Input #1 Current or Voltage Input Burden resistor (250 ohm) Configuration CSD inputs*
	BJ8	In = current	Out = Voltage input, no burden resistor	± 4–20 mA or ± 10 V dc
	BJ9	Not used	Not used	Burden Resistor (250 ohm)
	BJ10	Not used	Not used	Configuration
	BJ11	In = current	Out = Voltage input, no burden resistor	± 4–20 mA or ± 10 V dc
	BJ12	Not used	Not used	Burden Resistor (250 ohm)
	BJ13	Not used	Not used	Configuration
	BJ14	In = current input	Out = Voltage input, no burden resistor	± 4–20 mA or ± 10 V dc Burden Resistor (250 ohm) Configuration
	BJ15	In = current input	Out = Voltage input, no burden resistor	± 4–20 mA or ± 10 V dc Burden Resistor (250 ohm) Configuration

* See Appendix D, Figure D-26

	Jumper	Position		Application Notes
TBQC <R1>, <R2>, <R3> Location 9 Rev. TBQCG#A	BJ1 to BJ15	In = connects NEG of mA current inputs to DCOM	Out = mA input is not referenced to DCOM	If the hardware jumper is installed, the NEG terminal of the respective mA input is connected to DCOM. See Connection Examples in Appendix D.
	BJ16 and BJ17	**Default 20 mA Max**	200 mA Max	20/200 mA output current range select for TCQA mA outputs circuit 1 and circuit 2

	Jumper	Position		Application Notes
TBQE <R1> Location 7 Rev. TBQEG#B	BJ1 and BJ2	**Default 20 mA Max**	200 mA Max	20/200 mA output current range select for TCQE mA outputs circuit 1 and circuit 2

	Jumper	Position		Application Notes
TBSA <R2> Location 8 Rev. TBSAG#B	JP1 – JP2	**IN**	Out	Drive 1 Receive line termination and suppression jumpers
	JP3 – JP4	**IN**	Out	Drive 1 Transmit line termination and suppression jumpers
	JP5 – JP6	**IN**	Out	Drive 2 Transmit line termination and suppression jumpers
	JP7 – JP8	**IN**	Out	Drive 2 Receive line termination and suppression jumpers
	JP9 – JP10	**IN**	Out	Drive 3 Transmit line termination and suppression jumpers
	JP11 – JP12	**IN**	Out	Drive 3 Receive line termination and suppression jumpers
	JP13 – JP14	**IN**	Out	Drive 4 Receive line termination and suppression jumpers
	JP15 – JP16	**IN**	Out	Drive 4 Transmit line termination and suppression jumpers

	Jumper	Position	Application Notes
PANA <R> Location 1 Rev. PANAG#AB	IRQ1	**Factory Set**	Interrupts Channel 1 Based on internal panel software
	IRQ2	**Factory Set**	Interrupts Channel 2 Based on internal panel software
	ET1 A4 A5	**Factory Set**	Channel 1 I/O Address Based on internal panel software
	BET1 BA4 BA5	**Factory Set**	Channel 2 I/O Address Based on internal panel software
	A14 – A19	**Factory Set**	Channel 1 Memory Address Based on internal panel software
	BA14 – BA19	**Factory Set**	Channel 2 Memory Address Based on internal panel software
	NODEID (Switch)	**Factory Set**	Channel 1 COREBUS ARCNET Address
	BNODEID (Switch)	**Factory Set**	Channel 2 COREBUS ARCNET Address
	BEN	**Factory Set**	Factory test – Processor reset

	Jumper	Position		Application Notes
TCCA <R5> Location 2 Rev. TCCAG#A	J1 SCPT	**Default enable**	Disable	Disable Serial RS-232C Port Enable = normal operation
	J2 FTST	**in = enable**	out = disable	Oscillator Enable Enable = normal operation
	J3	**in = enable**	out = disable	Processor Reset Enable = normal operation

	Jumper	Position		Application Notes
TCCB <R5> Location 3 Rev. TCCBG#B	J1 J2 J3 J4	**1-2** **MKV LM**	2-3 EX2000	Generator and Bus PT Voltage Monitor
	J5	**1-2** **MKV LM**	EX2000	Generator and Bus CT Current Monitor
	J14	**Default connected**	DCOM not connected	DCOM connection for RS-232C Monitor Port (TIMN)
	J15	**in = enable**	out = disable	Oscillator Enable Enable = normal operation
	J16	**in = enable**	out = disable	Oscillator Enable Enable = normal operation

	Jumper	Position		Application Notes
TCDA <Q11>, <Q51> Location 1 Rev. TCCAG#B	J1	**enable**	disable	Disable Serial RS-232C Port Enable = normal operation
	J2 – J3	**in = terminated**	out = disable	IONET Termination Resistor
		0	1 Binary weighted value	
	J6 J5 J4	**0** **0** **0**	1 2 4	IONET Address These should be left as the factory set.
	J7	**1 = enable**	0 = disable	Enable Stall Timer Enable = normal operation
	J8	**In = operate**	Out = test mode	Test Enable In = normal operation

	Jumper	Position		Application Notes
TCPD <PD> Location 1 Rev. TCPDG#B	BJS	In = Provide ground reference for 125 V dc	Out = 125 V dc system already has ground reference point	Ground Reference Jumper Remove for systems with external ground refernce on 125 V dc system. For circuit drawing, see Appendix C, Power Distribution Core Drawings, Figure C-1.

Caution

It is GE Industrial Systems standard practice to have an ungrounded 125 V dc battery system. The BJS on the TCPD board should stay IN.

	Jumper	Position		Binary Value	Application Notes
TCEA <P1> X Loc. 1 Y Loc. 3 Z Loc. 5 Rev. TCEAG#B	J1	**Default 0**	1 = test	-	Test function: 1 = enable
	J2 J3	0	1 = term	-	IONET Termination Resistors 0 = resistors not connected
	J4 J5 J6	See Table A-3, below.		1 2 4	IONET Address This configuration varies for X, Y, Z
	J8 J9 J10 J11 J22 J23 J24 J25 J26 J27	Application Specific		1 2 4 8 16 32 64 128 256 512	Low Pressure Shaft Trip Frequency See Notes on TCEA, next page.
	J12 J13 J14 J15 J16 J17 J18 J19 J20 J21	Application Specific		1 2 4 8 16 32 64 128 256 512	High Pressure Shaft Trip Frequency See Notes on TCEA, next page.
	J28 J29	Application Specific		See Table A-2	Type of control application Dual Redundant System
	J30	1 = enable	0 = stall dis-able	-	Stall function: must be in 1 position
	J31	In	Out	-	Factory test. Install for proper field operation

Table A-1. X, Y, Z Card Definition Determined According to Binary Summation

Board	Address	J4	J5	J6
X	4	0	0	1
Y	5	1	0	1
Z	6	0	1	1

Table A-2. Binary Values for J28 and J29

Type of Control Application	J28	J29
Dual Redundant	1	0
Others	0	1

Notes on the TCEA Board:

The exact frequency (in Hertz) for the trip frequency is now set via the I/O Configurator. While in the I/O Configurator, the required settings for the jumpers will be displayed on screen. The binary value of the jumper settings MUST be equal to the selected trip frequency divided by 16.

The following tables document the structure for the HP and LP settings:

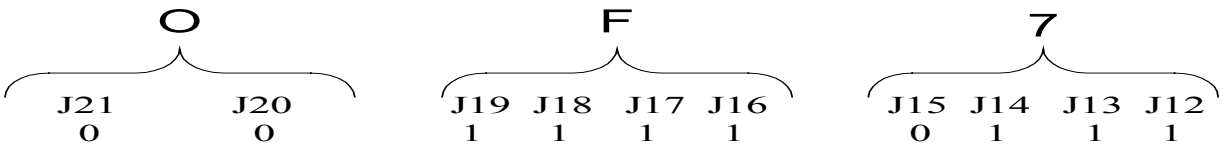
HP Trip (Hz)	Value (Dec)	Value (Hex)	J21 (512)	J20 (256)	J19 (128)	J18 (64)	J17 (32)	J16 (16)	J15 (8)	J14 (4)	J13 (2)	J12 (1)	
16383	1023	3FF	1	1	1	1	1	1	1	1	1	1	(Max)
16	1	001	0	0	0	0	0	0	0	0	0	1	(Min)
0	0	000	0	0	0	0	0	0	0	0	0	0	(Shaft not used)

LP Trip (Hz)	Value (Dec)	Value (Hex)	J27 (512)	J26 (256)	J25 (128)	J24 (64)	J23 (32)	J22 (16)	J11 (8)	J10 (4)	J9 (2)	J8 (1)	
16383	1023	3FF	1	1	1	1	1	1	1	1	1	1	(Max)
16	1	001	0	0	0	0	0	0	0	0	0	1	(Min)
0	0	000	0	0	0	0	0	0	0	0	0	0	(Shaft not used)

Example:

HP Shaft Overspeed Trip Frequency set to 3960 (110% of 3600)

3960/16 = 247.5 ⇒ round **DOWN** (always!) to 247 decimal = 0F7 Hex.



	Jumper	Position		Board Coord
TCQA <R1>, <R2>, <R3>	J1	**Default Simplex**	Not LM	20/200 mA Output Circuit #1 Mode Select
	J2	**Default Simplex**	Not LM (TMR)	20/200 mA Output Circuit #2 Mode Select
Location 2 Rev. TCQAG#B	J5 J6	**Default 20mA Max** **20mA Max**	200 mA Max 200 mA Max	Circuit #1 Current Range Circuit #2 Current Range
	J7	**Default normal**	disable port	RS-232C Port Enable Enable = Normal Operation
	J8	**In = enable**	Out = test	Oscillator Enable Enable = Normal Operation

	Jumper	Position		Application Notes
TCQC <R1>, <R2>, <R3> Location 4 Rev. TCQCG#B	BJ1 BJ2 BJ25 BJ26 BJ27	These hardware jumpers are used to select the output current range of the servo, from 10mA to 240 mA.		Regulator #1 See TCQC Table #1 for details.
	BJ3 BJ4 BJ28 BJ29 BJ30	These hardware jumpers are used to select the output current range of the servo, from 10mA to 240 mA.		Regulator #2 See TCQC Table #1 for details.
	BJ5 BJ6 BJ31 BJ32 BJ33	These hardware jumpers are used to select the output current range of the servo, from 10mA to 240 mA.		Regulator #3 See TCQC Table #1 for details.
	BJ7 BJ8 BJ34 BJ35 BJ36	These hardware jumpers are used to select the output current range of the servo, from 10mA to 240 mA.		Regulator #4 See TCQC Table #1 for details.
	BJ9 BJ10	These hardware jumpers are used to select the output current range of the servo, from 10mA to 40 mA.		Regulator #5 See TCQC Table #2 for details.
	BJ11 BJ12	These hardware jumpers are used to select the output current range of the servo, from 10mA to 40 mA.		Regulator #6 See TCQC Table #2 for details.
	BJ13 BJ14	These hardware jumpers are used to select the output current range of the servo, from 10mA to 40 mA.		Regulator #7 See TCQC Table #2 for details.
	BJ15 BJ16	These hardware jumpers are used to select the output current range of the servo, from 10mA to 40 mA.		Regulator #8 See TCQC Table #2 for details.
	BJ17	**Default** **1-2 = Connect**	2-3 = DCOM not connected	DCOM connection for RS-232C Monitor Port Connect = normal operation
	BJ18 BJ20	**In = No additional Current limit**	Out = Current limit supply voltage	Out for intrinisically safe installations; further limits P15 and N15 supply to proximity transducers. (LM installations)
	BJ21	**Default** **1-2 = Enabled**	2-3 = Disabled	Enable Stall timer. Enable = normal operation
	BJ22	**Default** **1-2 = Enabled**	2-3 = Disabled	Oscillator Enable Enable = normal operation
	BJ23 BJ24	**Out = termination resistor out.**	In = termination resistor in.	Not used.
	BJ38 BJ39	**Default** **1-2 = 0.5 gain**	2-3 = full gain	Pulse Rate Input Gain

TCQC Table #1 – Servo Outputs 1 – 4

Nominal Output (mA)	Servo Coil (Ohms)	BJ1,3,5,7					BJ2,4,6,8			BJ25,28,31,34		BJ26,29,32,35		BJ27,30,33,36	
		10	10X	20	40	80	DEF	Y	Z	DEF	A	DEF	B	DEF	C
10 (Gas Simplex)	1000		X				X			X		X		X	
10 (Other)	1000	X					X			X		X		X	
20	125			X				X		X		X		X	
40	62.5				X				X	X		X		X	
80	22					X			X		X	X		X	
120	40	X							X		X		X	X	
240	37.5	X							X		X		X		X

TCQC Table #2, Servo Outputs 5 – 8

Nominal Output (mA)	Servo Coil (Ohms)	BJ9,11,13,15				BJ10,12,14,16		
		10	10X	20	40	10	20	40
10 (Gas Simplex)	1000		X			X		
10 (Other)	1000	X				X		
20	125			X			X	
40	62.5				X			X

TCQC Servo Feedback Settings:

BJ2, BJ4, BJ6 and BJ8 select the feedback scaling, while the rest select the source output resistance and, hence the output current.

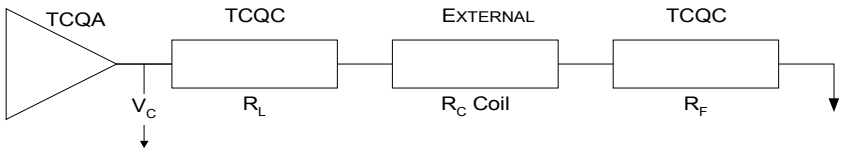


Figure A-1. Feedback Resistors

Table A-2. Feedback Resistors

Nominal Output (mA)	R_L Load (Ohms)	R_C Coil (Ohms)	R_F Fdek (Ohms)	V_C (Volts)
10	0.0	1000	200	12.0
20	332	125	100	11.1
40	162	89/62.5	50	12.0/11.0
80*	100	22	25	11.8
120*	0.0/0.0	75/40	16.8	11.0/6.8
240*	0.0	37.5	8.6	11.0

* Servo 1 – Servo 4 only

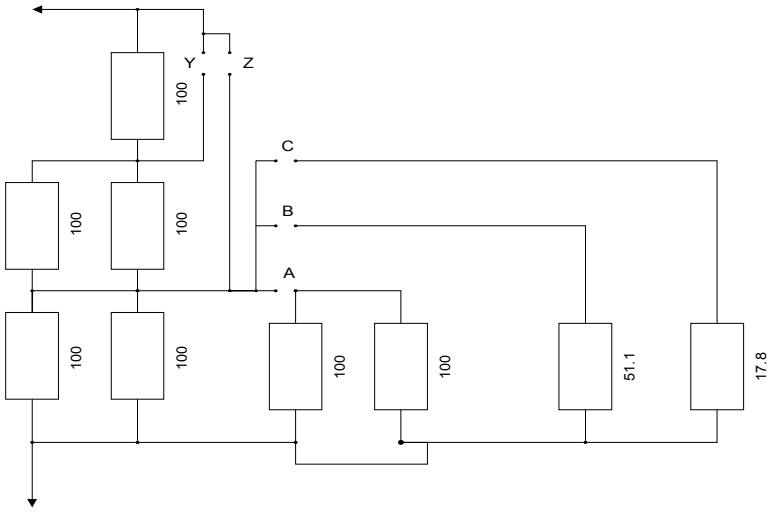


Figure A-3. Feedback Jumpers

Nominal Current (mA)	Y	Z	A	B	C	Feedback Resistance
10	–	–	–	–	–	200
20	√	–	–	–	–	100
40	–	√	–	–	–	50
80	–	√	√	–	–	25
120	–	√	√	√	–	16.8
240	–	√	√	√	√	8.6

Table A-4. Feedback Resistors and Jumpers (R_F)

	Jumper	Position		Application Notes
TCQE <R1> Location 3 TCQEG#A	JP1	**In = enable normal**	Out = disable	Oscillator Enable Enable = normal operation
	JP2	**Default** **Connect**	DCOM not connected	DCOM connection for RS-232C Monitor Port Connect = normal operation
	JP3	**In = enable normal**	Out = disable	Oscillator Enable Enable = normal operation
	JP4	**Default** **S = Simplex**	R = not LM	20/200 mA Output Circuit # 1 Mode Select
	JP5	**Default** **20 mA Max**	200 mA Max	Max current Circuit # 1 Mode Select
	JP6	**Default** **S = Simplex**	R = not LM	20/200 mA Output Circuit # 2 Mode Select
	JP7	**Default** **20 mA Max**	200 mA Max	Max current Circuit # 2 Mode Select
	JP8	**In = Enabled**	Out = Disabled	Enable Stall timer. Enable = normal operation

UCIB <R> Location 1 Rev. UCIBG#AC	Jumper	Position		Application Notes
	JP1	**In = enable clock**	Out = disable Factory Test	Clock Enable Enable = normal operation

UCPB <R>, <R1>, <R2>,<R3>, <R5> Location 1 Rev. UCPBG#A	Jumper	Position		Application Notes
	JP1	**Out = disable For Factory test**	In = enable	Oscillator Enable Enable = normal operation
	JP2	**In = 25/50 mhz**	Out = 33/100 mHz	486 local BUS speed selection
	JP3	**Out = disable For Factory test**	In = enable	Test out

Appendix B Hardware Documents

Introduction

This appendix should be used to check for proper cabling after the equipment is installed, but before beginning startup.

Cables that carry signals and power are categorized into four defining levels: **low**, **medium**, **high**, and **power**. Each level can include classes. Electrical noise from cabling of various voltage levels can interfere with microprocessor-based control systems, causing the drive to malfunction.

This appendix provides recommended cable separation practices to reduce **electrical noise**. The information is presented as follows:

Note If a situation at the installation site is not covered in this document, or if these guidelines cannot be met, please contact GE before installing the cable.

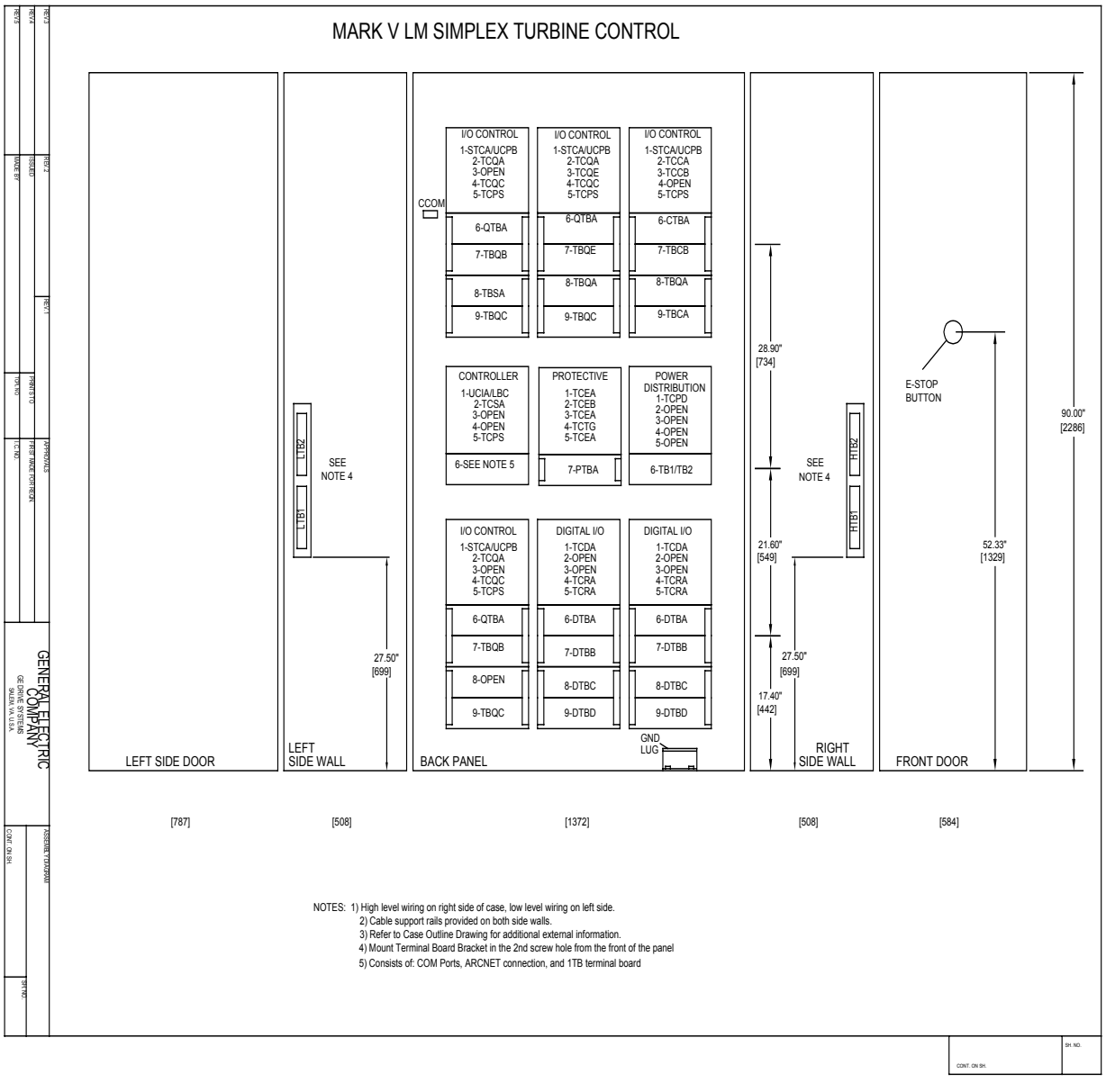


Figure B-1. Hardware Document Example – Panel Layout

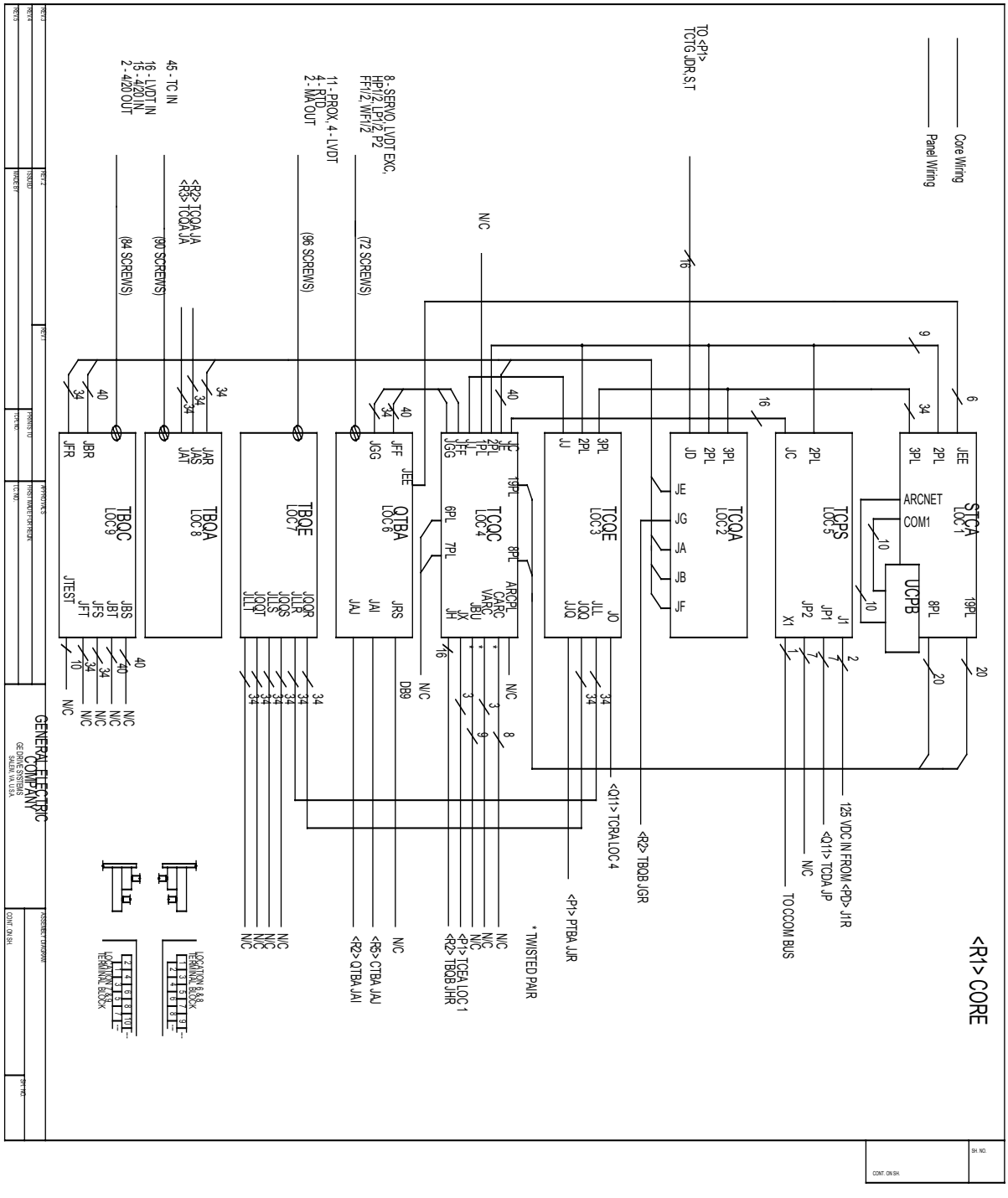


Figure B-2. Hardware Document Example – <R1> Core

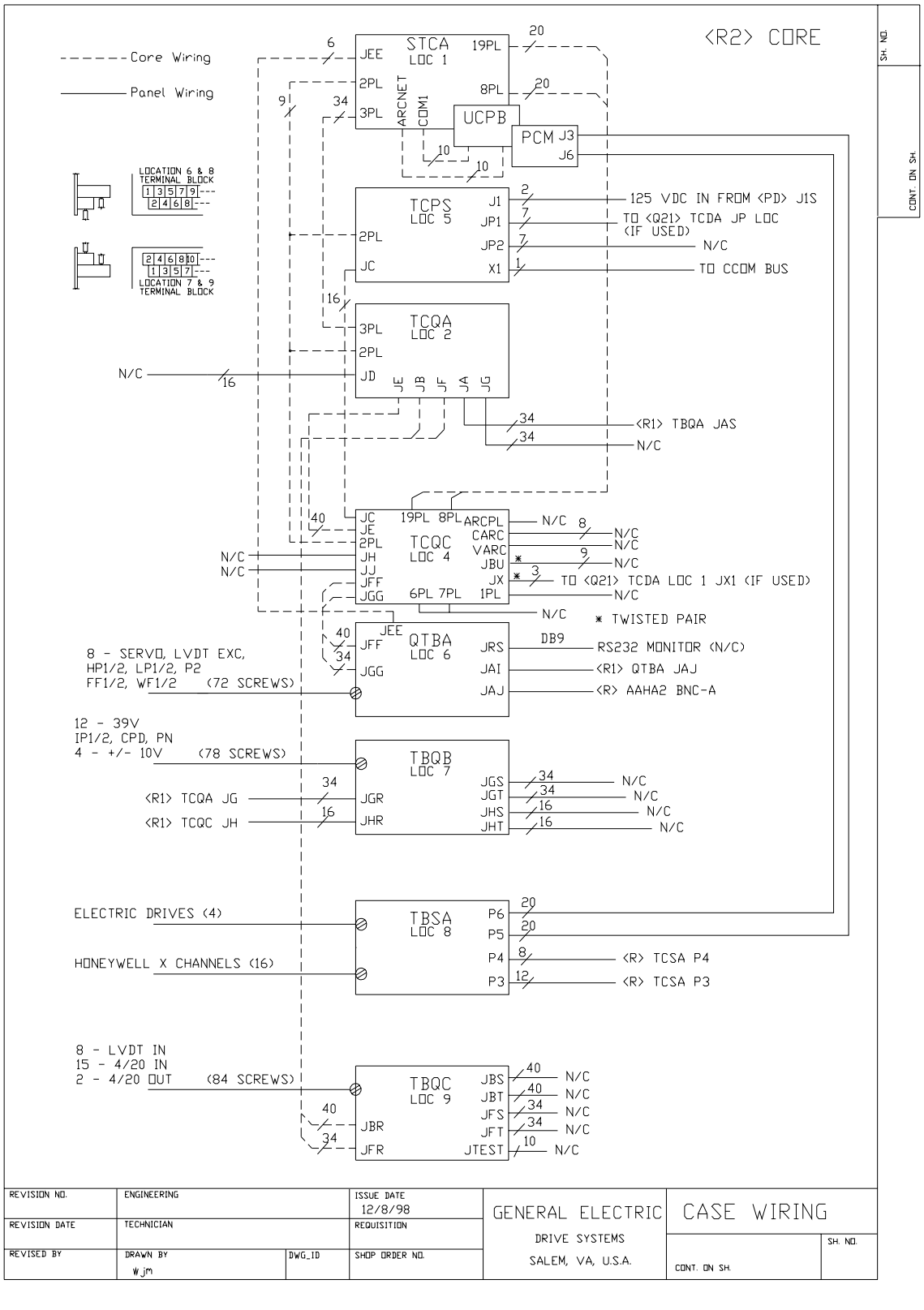


Figure B-3. Hardware document example – <R2> core

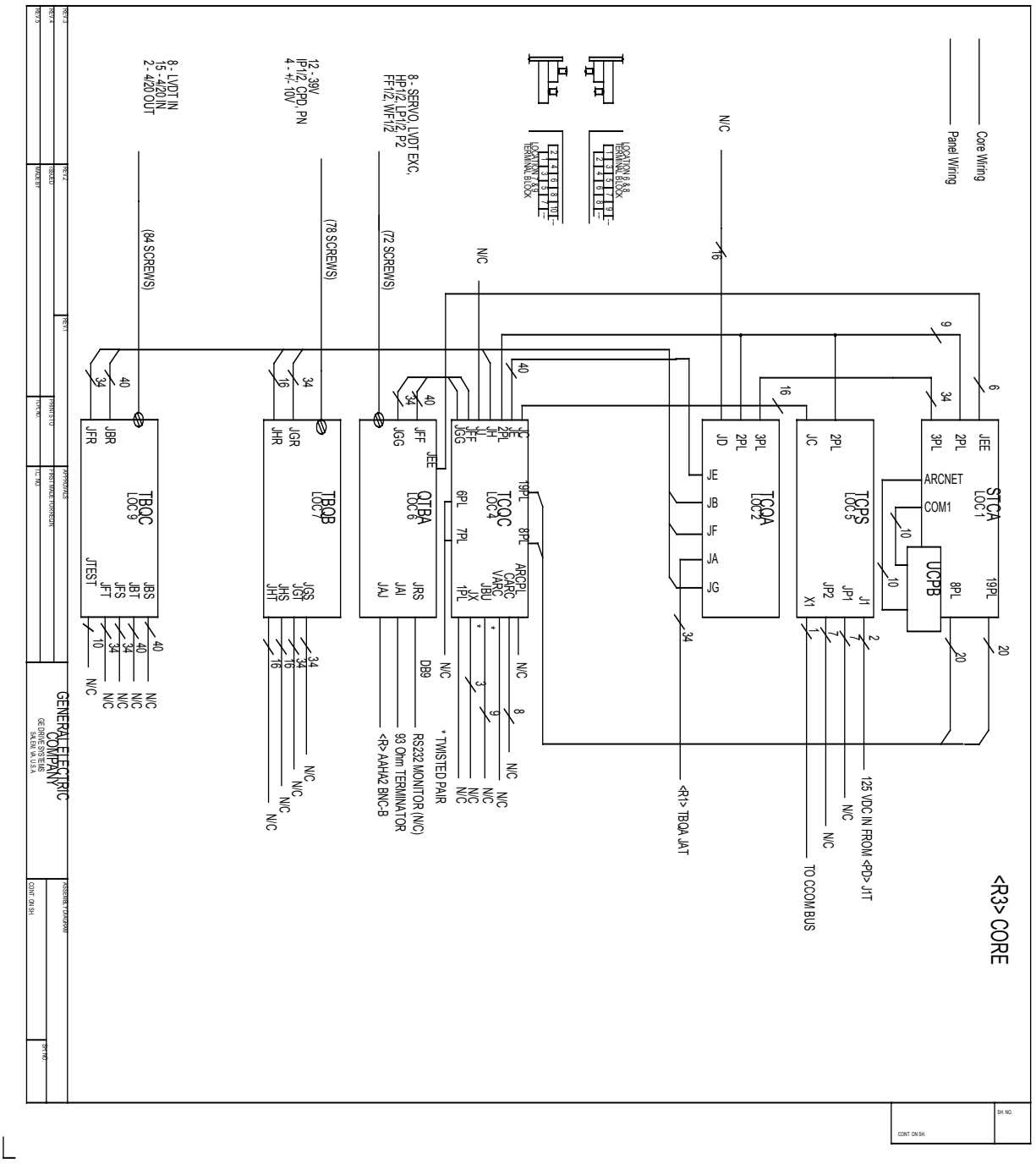


Figure B-4. Hardware Document Example – <R3> Core

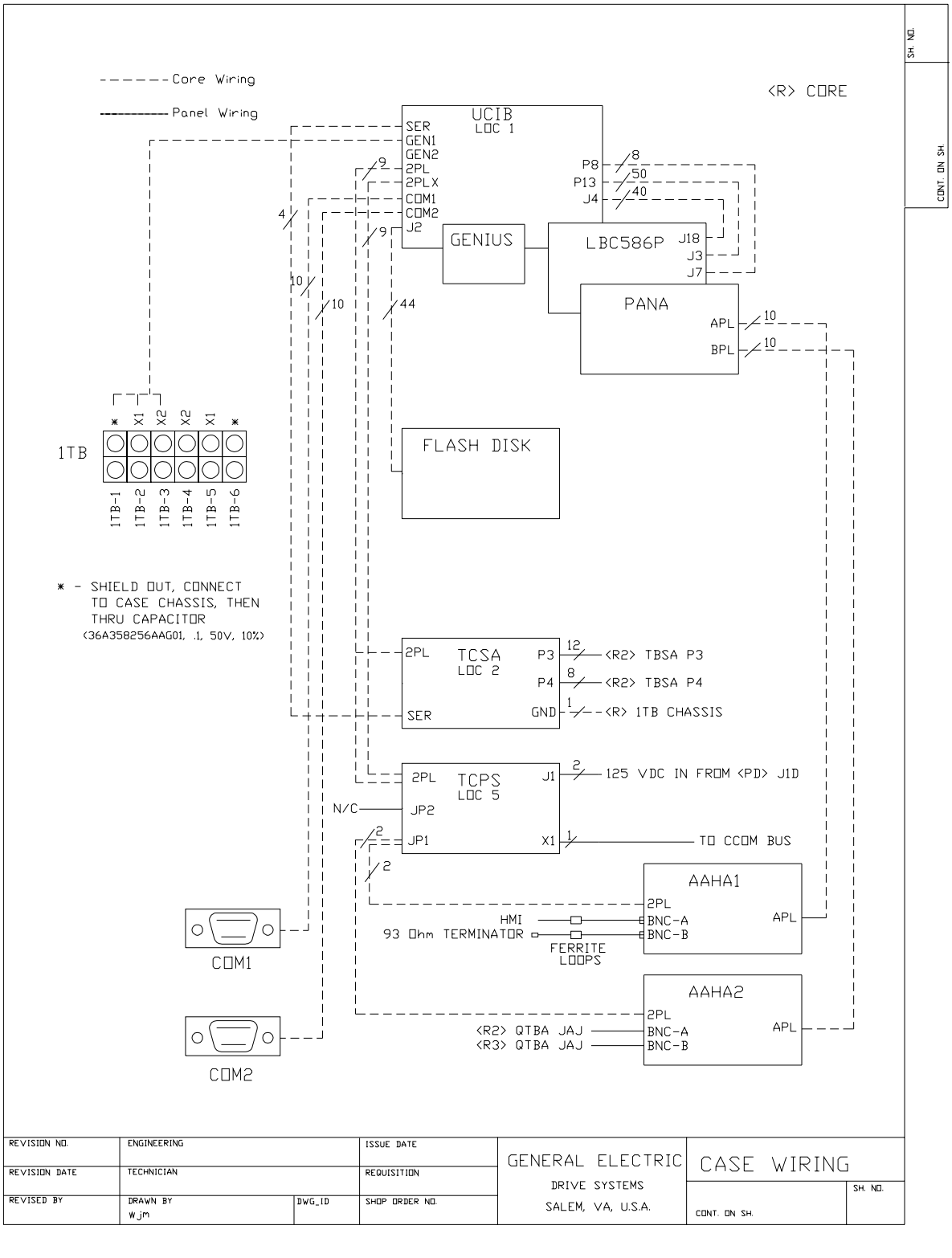


Figure B-5. Hardware Document Example – <R> Core

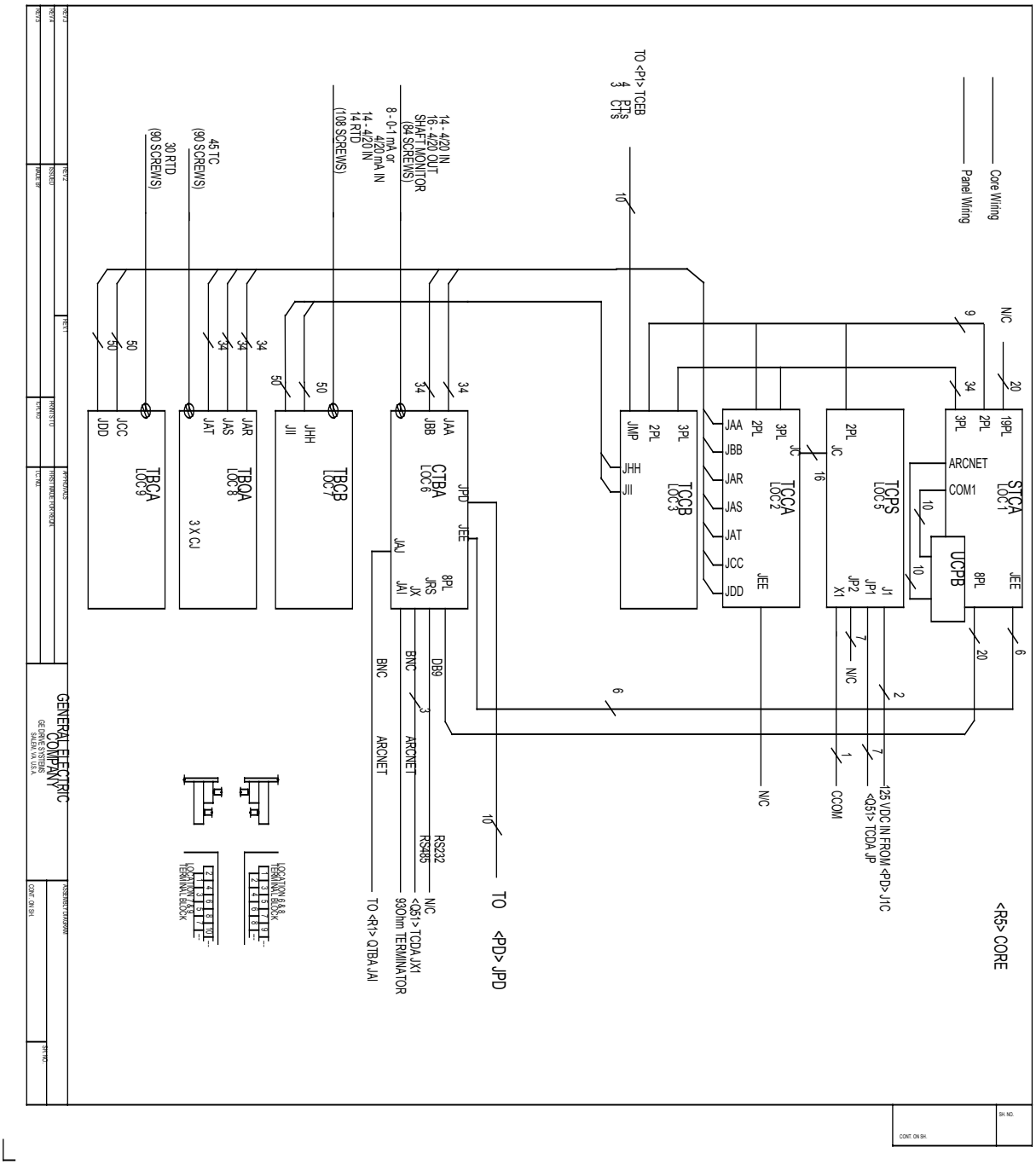


Figure B-6. Hardware Document Example – <R5> Core

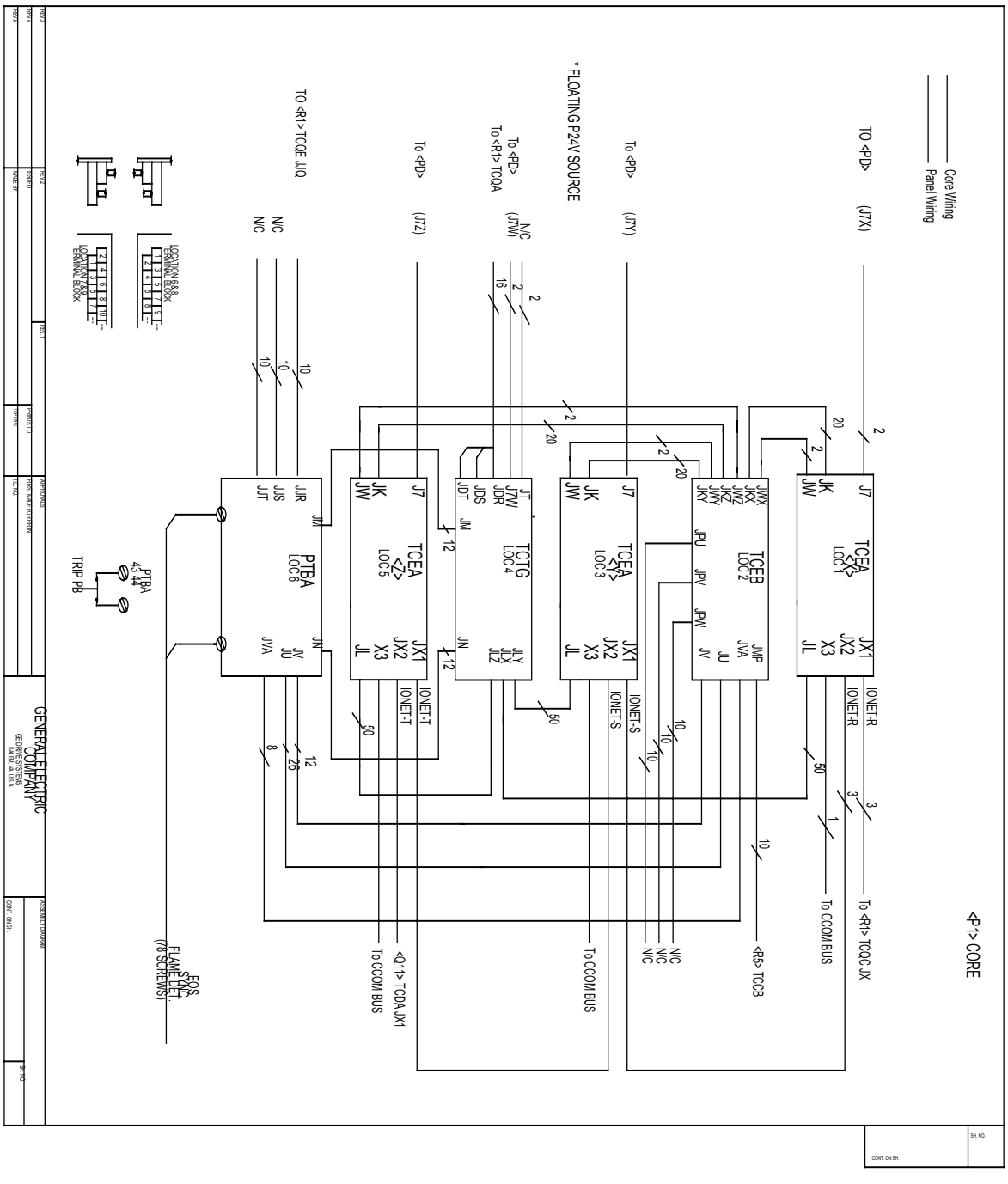


Figure B-7. Hardware Document Example – <P1> Core

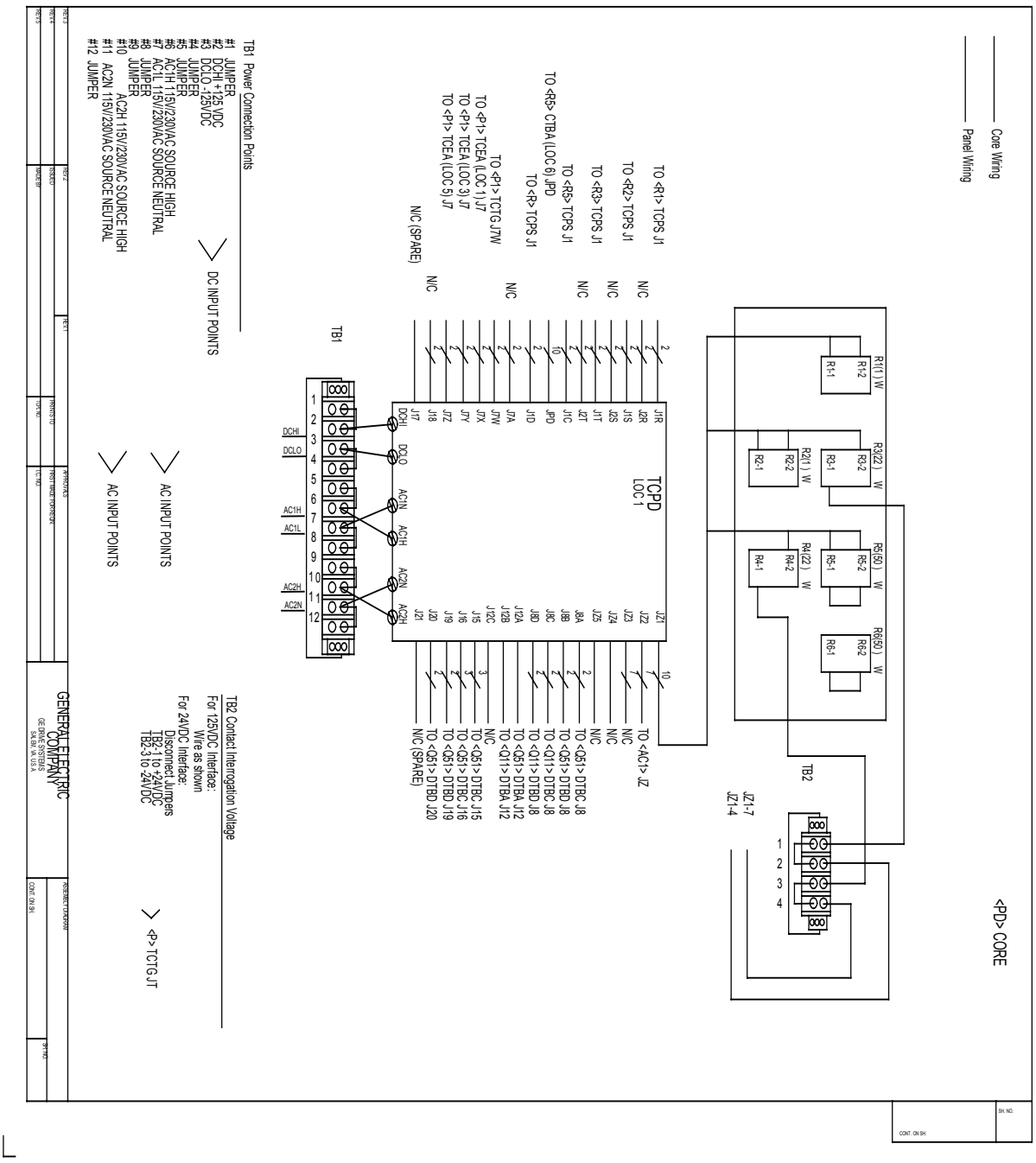


Figure B-8. Hardware Document Example – <PD> Core

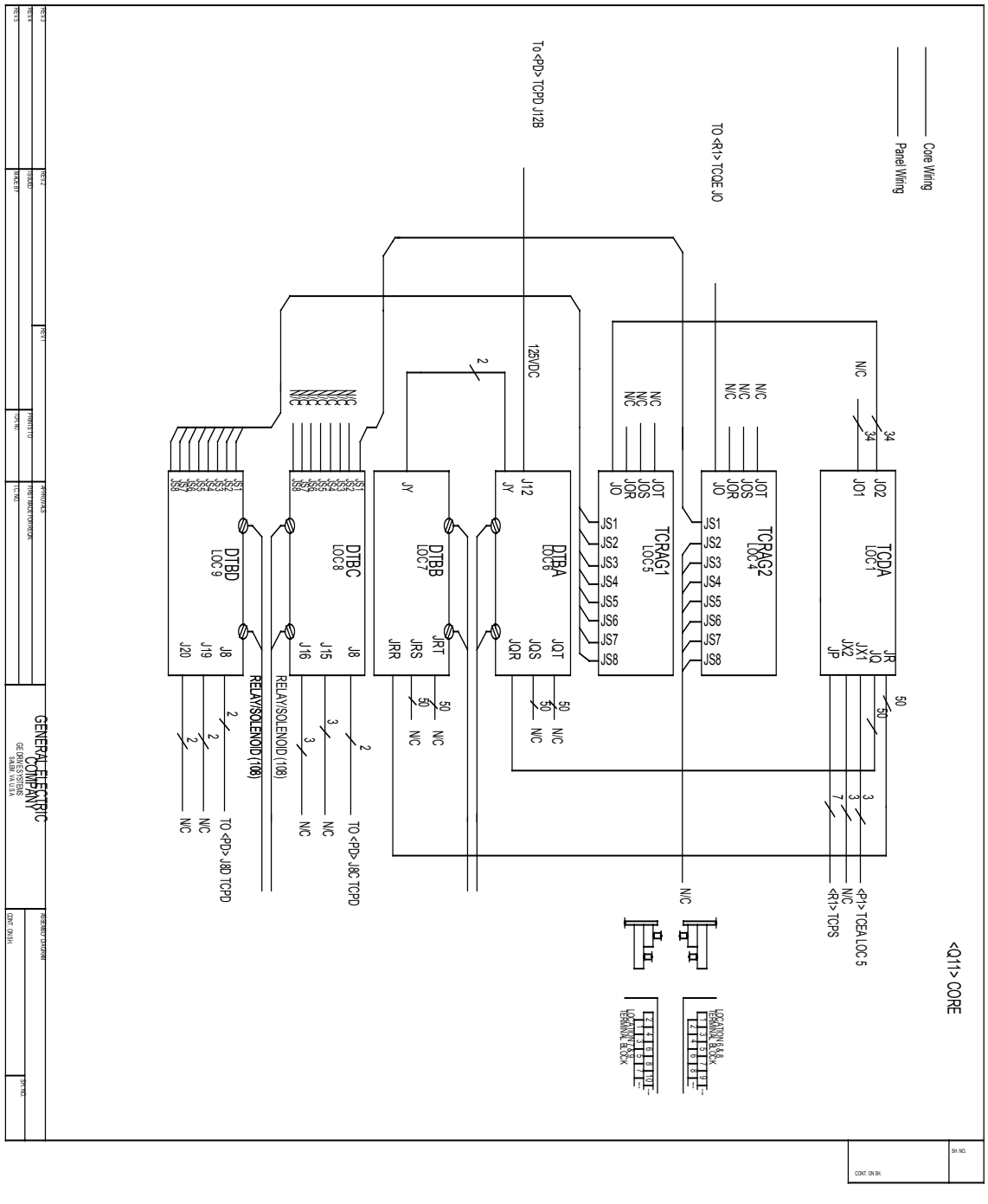
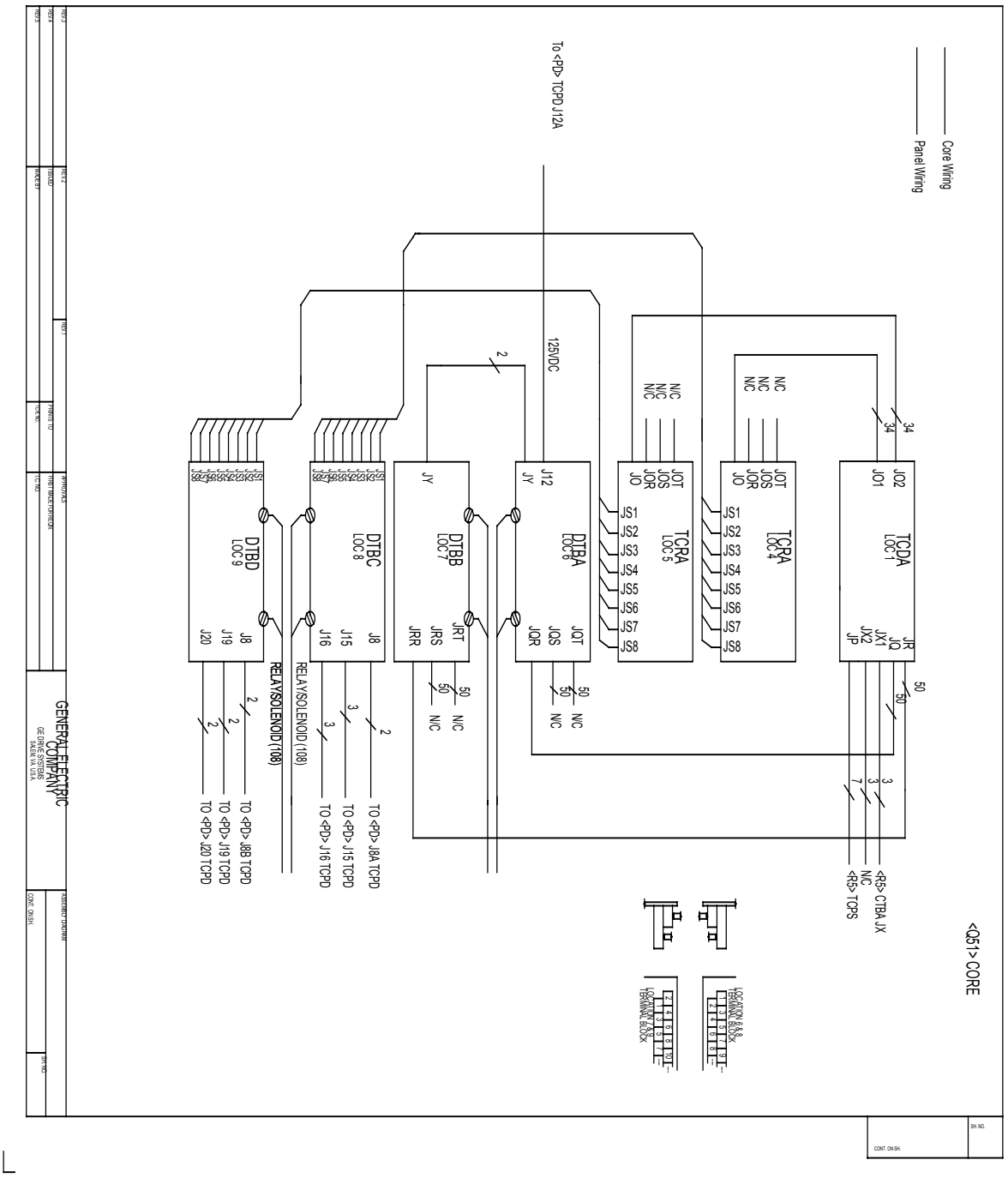


Figure B-9. Hardware Document Example – <Q11> Core



Note This document is labeled <Q51>, the actual core name is <Q51>.

Figure B-10. Hardware Document Example – <Q51> Core

Notes

Appendix C Power Distribution Core Diagrams

Introduction and Application Notes

The following pages are diagrams of the Power Distribution Core <PD>. For simplification, not every component is shown.

Since the ac supply voltage can be either 120 or 240 volts, the transformer and rectifier assembly must change.

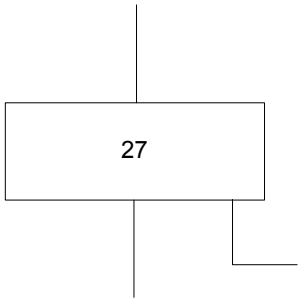
The JZ4 and JZ5 plugs are the auxiliary ac source connection point for applications that require an isolated input for an uninterruptable power source connection(s) and/or switched back up power source. The 'HOT' side can be isolated with external circuitry connected to these plugs, but the neutral cannot.

Caution

Care must be used when connecting auxiliary ac sources into the JZ4 and JZ5 plugs. The neutral of the auxiliary ac input (JZ4 and JZ5 plugs) is connected to the neutral of the critical ac input (TB1, points 7, 8, 11, and 12).

The 27 boxes (for ANSI standard designation number) are undervoltage devices that send a diagnostic alarm to the <R> core if either the ac or dc input voltagei s no longer present. The ac undervoltage boxes include an LED to give a visual indication of fuse status. In the dc circuits, the LED is in a separate circuit.

The following diagram is an example of the undervoltage detectors as shown on the figures of this Appendix:



If the green LED is off or the red LED is on, the fuse is open.

Switches are provided on newer revisions of the <PD> core. These should be used when it is necessary to remove power from only one core or board at a time.

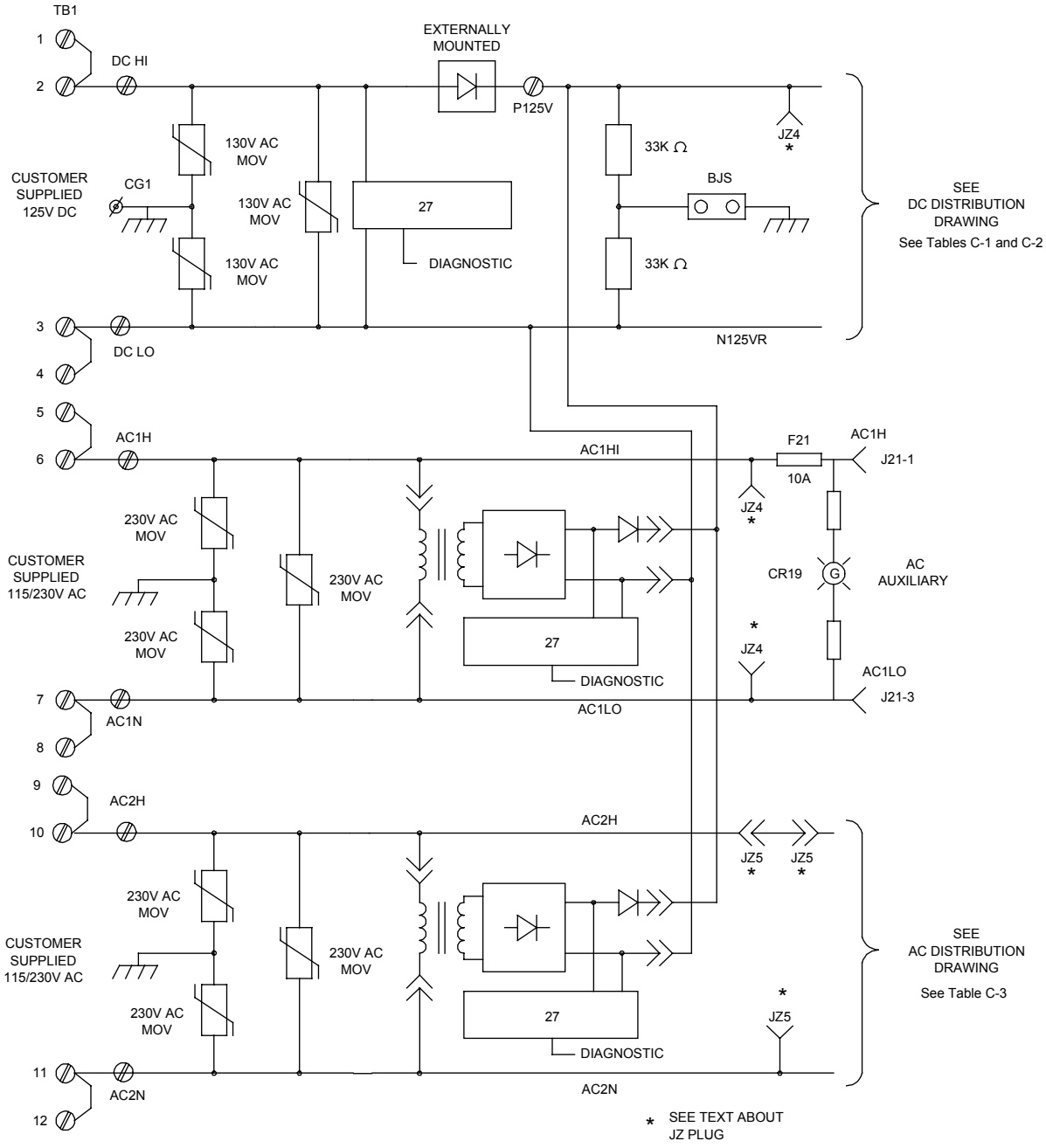


Figure C-1. <PD> Core Incoming AC and DC Circuits

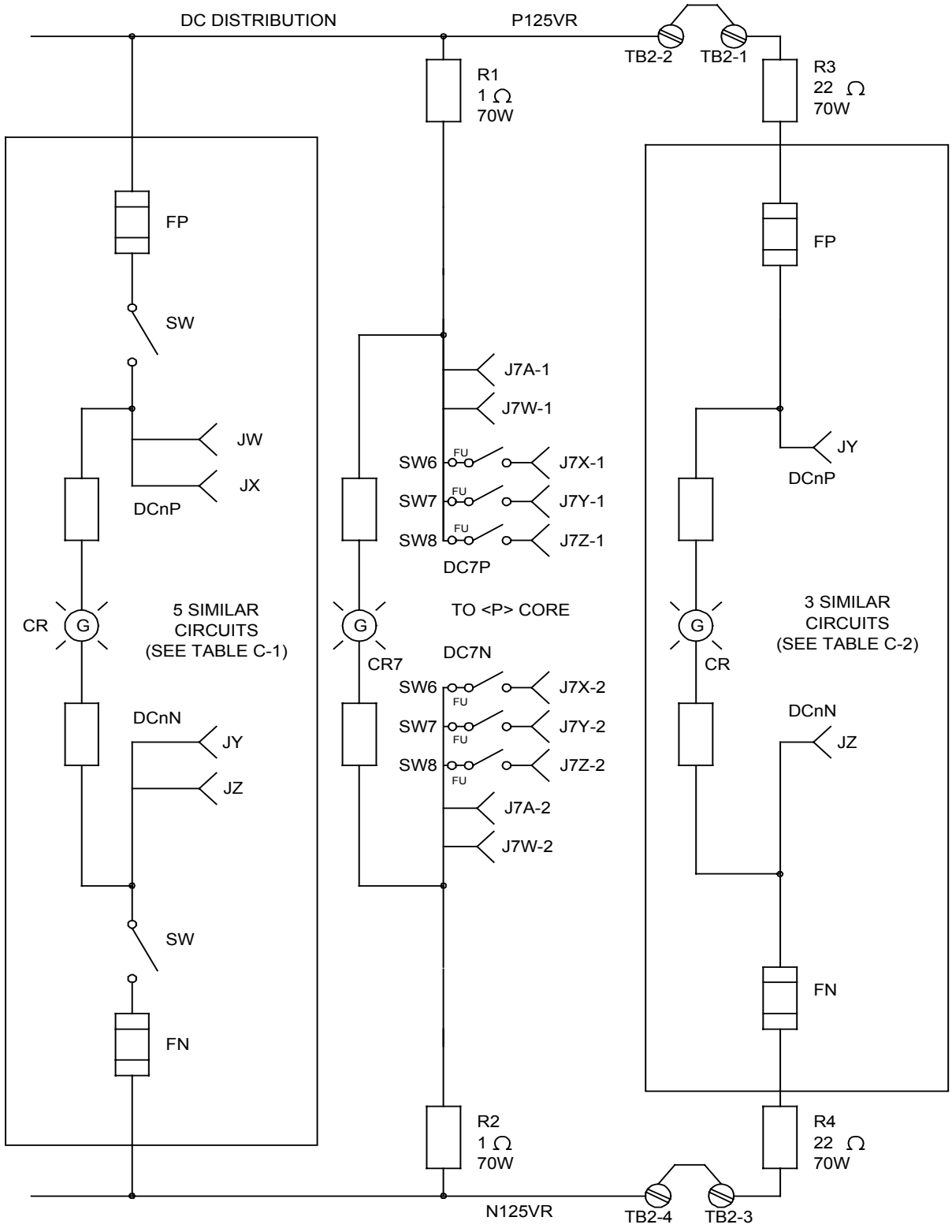


Figure C-2. <PD> Core DC Power Distribution

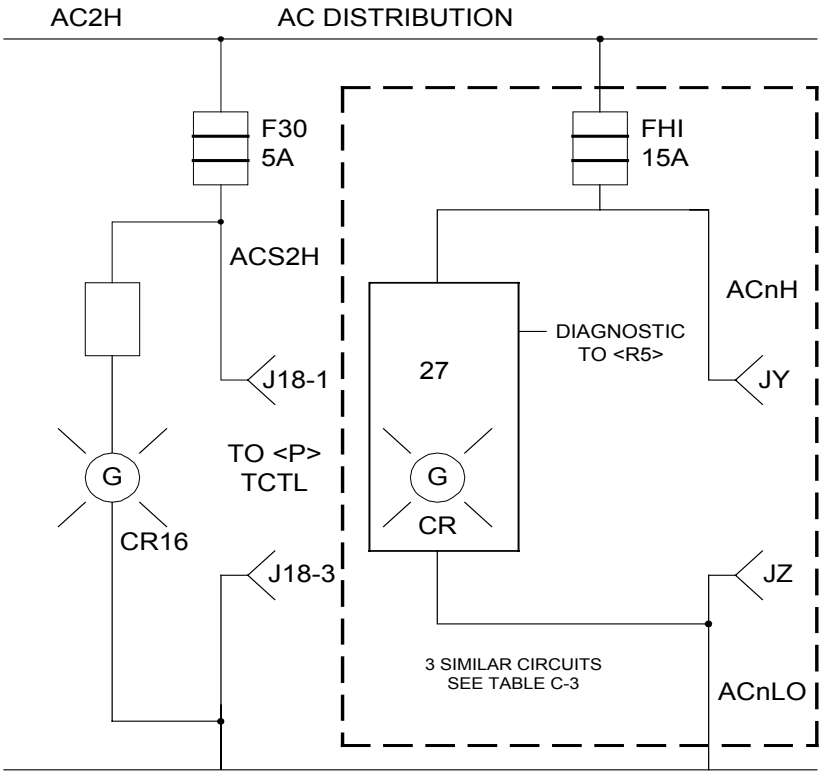


Figure C-3. <PD> Core AC Power Distribution

Table C-1. DC Distribution

Circuit	DcnP dcnNn	FP	FN	Amps	SW	CR	Pos. JW	Pos. JX	Neg. JY	Neg. JZ	Core
1	1	FU1	FU2	5	1	1	J1R-1	J2R-1	J1R-2	J2R-2	R1
2	2	FU3	FU4	5	2	2	J1S-1	J2S-1	J1S-2	J2S-2	R2
3	3	FU5	FU6	5	3	3	J1T-1	J2T-1	J1T-2	J2T-2	R3
4	4	FU7	FU8	5	4	4	J1C-1	N/A	J1C-2	N/A	R5
5	5	FU9	FU10	5	5	5	J1D-1	N/A	J1D-2	N/A	R
6	8	FU13	FU14	15	N/A	8	J8A-1	N/A	J8A-2	N/A	Q51
7	9	FU15	FU16	15	N/A	9	J8B-1	N/A	J8B-2	N/A	Q51
8	10	FU17	FU18	15	N/A	10	J8C-1	N/A	J8C-2	N/A	Q11
9	11	FU19	FU20	15	N/A	11	J8D-1	N/A	J8D-2	N/A	Q11
10	TP	N/A	N/A	5	N/A	7	J7W-1	N/A	J7W-2	N/A	TCTG
11	7X	FU34	FU35	5	6	27	J7X-1	N/A	J7X-2	N/A	X
12	7Y	FU36	FU37	5	7	28	J7Y-1	N/A	J7Y-2	N/A	Y
13	7Z	FU38	FU39	5	8	29	J7Z-1	N/A	J7Z-2	N/A	Z

Table C-2. DC Distribution

Circuit	DcnP dcnNn	FP	FN	Amps	CR	Positive JY	Negative JZ	Core
1	12	FU21	FU22	1.5	12	J12A-1	J12A-2	Q51
2	13	FU23	FU24	1.5	13	J12B-1	J12B-2	Q11

Table C-3. AC Distribution

Circuit	AcnH AcnLOn	FHI	Amps	CR	"HOT" JY	Neutral JZ	Core
1	1	FU29	15	15	J17-1	J17-3	AUX
2	3	FU31	15	17	J19-1	J19-3	R51
3	4	FU32	15	18	J20–1	J20-3	R51

AC3H and AC4H are used for the ignition transformers.
The ac distribution voltage depends on the application.

Special Use Contact Outputs and Related Components

Two contact output circuits contain unique components for special applications. LM applications do not require these unique components, which are bypassed by a jumper. Figure C-4 shows contact output 16, Figure C-5 shows contact output 17, and Figure C-6 shows contact output 18.

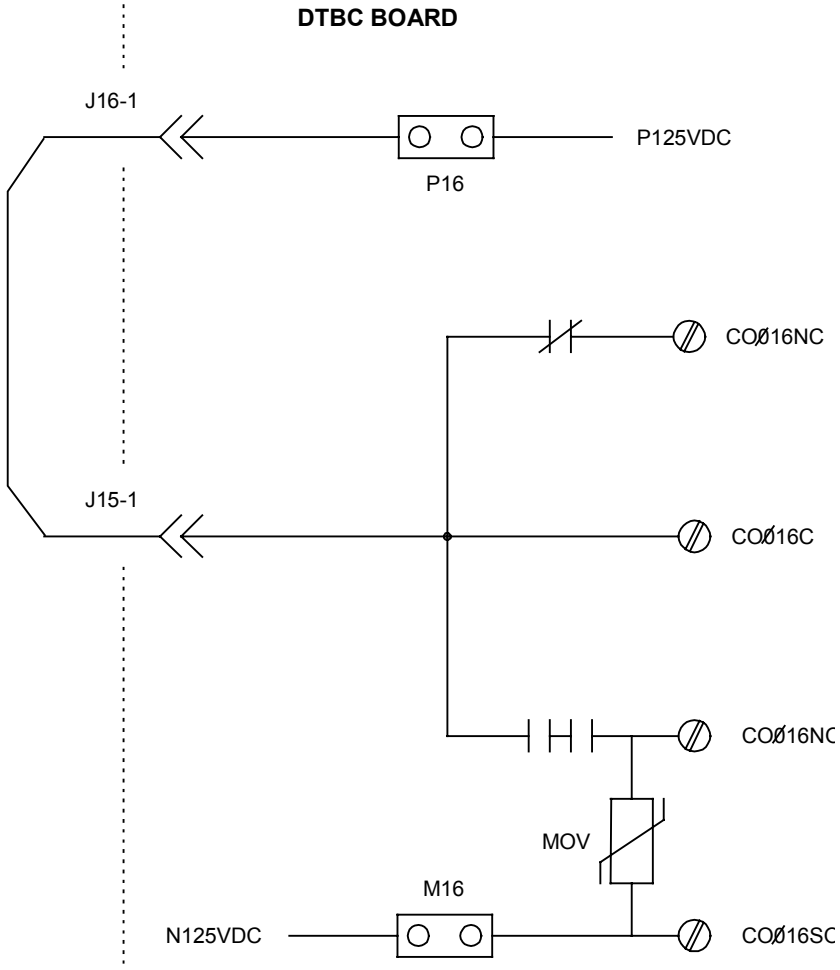


Figure C-4. Contact Output 16 Circuit

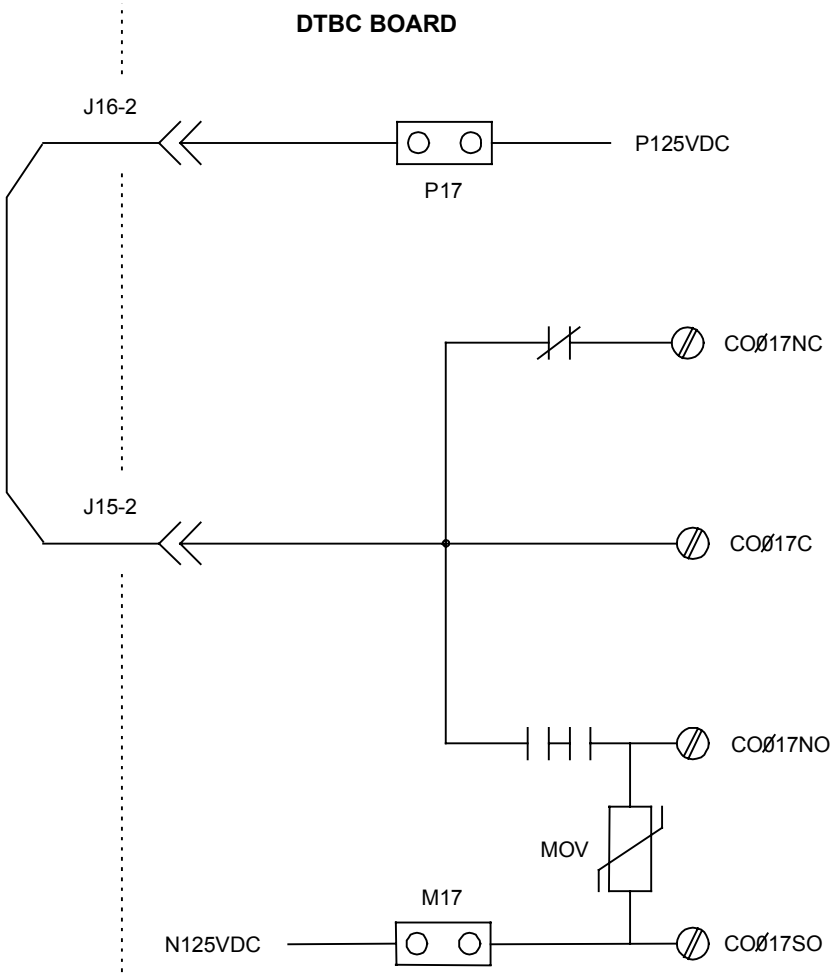


Figure C-5. Contact Output 17 Circuit

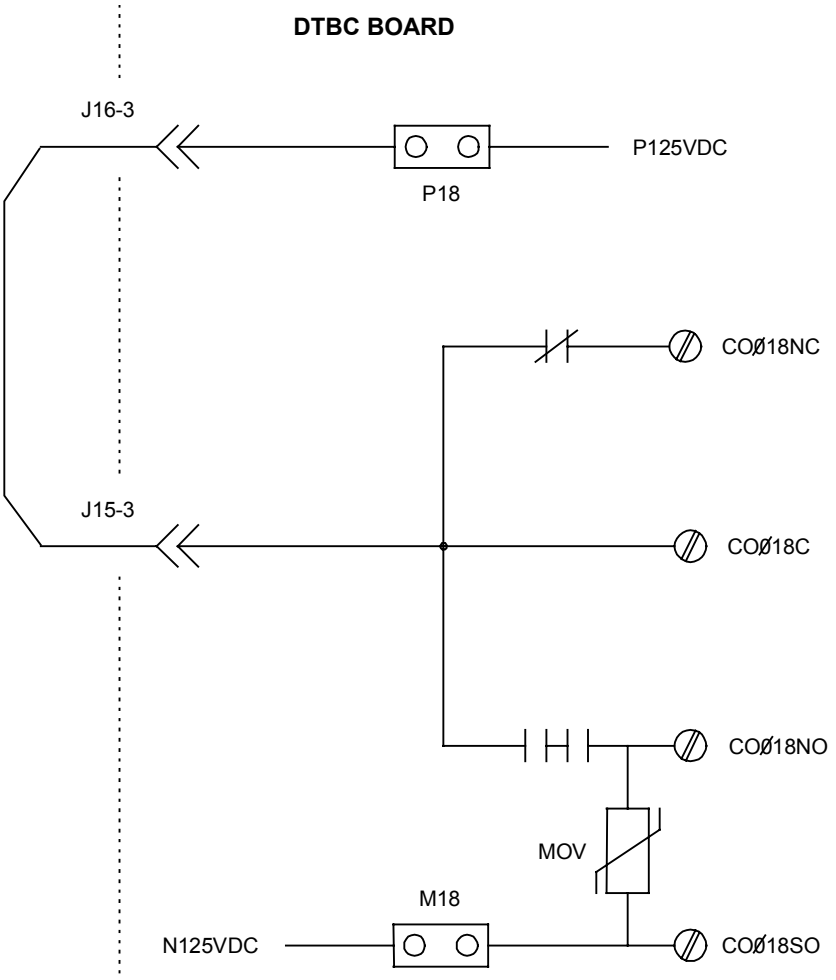


Figure C-6. Contact Output 18 Circuit

Appendix D Signal Flow Diagrams

Section **Page**

Definitions of Abbreviations

Boxes on the diagrams in Appendix D contain the following abbreviations.

A/D	Analog-to-digital converter
CL	Current limit
CTR	Counter
D/A	Digital-to-analog converter
MP	Microprocessor
MUX	Multiplexer, switches multiple inputs to one output
RD	Relay driver
USART	Universal synchronous/asynchronous receiver/transmitter
VCO	Voltage-controlled oscillator

(VCO and CTR combined are the same as an A/D Converter)

Signal Flow Diagrams

Table D-1. Milliamp Input Tables, <R5> Core, CTBA Board Location 6

	Generic Signal Name (from left column of IO.ASG file)	Signal Termination Points			JBB Pin Numbers		Hardware Jumper BJ
		POS	NEG	EXC			
<R5> Core	R5TCCA_MAI01	37	38	39	1	2	1
CTBA Board Location 6	R5TCCA_MAI02	41	42	40	3	4	2
	R5TCCA_MAI03	43	44	45	5	6	3
	R5TCCA_MAI04	47	48	46	7	8	4
	R5TCCA_MAI05	49	50	51	9	10	5
	R5TCCA_MAI06	53	54	52	11	12	6
	R5TCCA_MAI07	55	56	57	13	14	7
	R5TCCA_MAI08	59	60	58	15	16	8
	R5TCCA_MAI09	61	62	63	17	18	9
	R5TCCA_MAI10	65	66	64	19	20	10
	R5TCCA_MAI11	67	68	69	21	22	11
	R5TCCA_MAI12	71	72	70	23	24	12
	R5TCCA_MAI13	73	74	75	25	26	13
	R5TCCA_MAI14	77	78	76	27	28	14

Table D-2. Milliamp Input, <R5> Core, TBCB Board Location 7

	Generic Signal Name (from left column of IO.ASG file)	Signal Termination Points			JHH Pin Numbers		Hardware Jumper Range	
		POS	NEG	EXC			BJ	BJ
<R5> Core	R5TCCB_MAI01	1	2	3	1	2	1	
TBCB Board Location 7	R5TCCB_MAI02	5	6	4	3	4	2	
	R5TCCB_MAI03	7	8	9	5	6	3	
	R5TCCB_MAI04	11	12	10	7	8	4	
	R5TCCB_MAI05	13	14	15	9	10	5	
	R5TCCB_MAI06	17	18	16	11	12	6	
	R5TCCB_MAI07	19	20	21	13	14	7	
	R5TCCB_MAI08	23	24	22	15	16	8	
	R5TCCB_MAI09	25	26	27	17	18	9	
	R5TCCB_MAI10	29	30	28	19	20	10	
	R5TCCB_MAI11	31	32	33	21	22	11	
	R5TCCB_MAI12	35	36	34	23	24	12	
	R5TCCB_MAI13	37	38	39	25	26	13	
	R5TCCB_MAI14	41	42	40	27	28	14	
	R5TCCB_MAI15	43	44	45	29	30	15	23
	R5TCCB_MAI16	47	48	46	31	32	16	24
	R5TCCB_MAI17	49	50	51	33	34	17	25
	R5TCCB_MAI18	53	54	52	35	36	18	26
	R5TCCB_MAI19	55	56	57	37	38	19	27
	R5TCCB_MAI20	59	60	58	39	40	20	28
	R5TCCB_MAI21	61	62	63	41	42	21	29
	R5TCCB_MAI22	65	66	64	43	44	22	30

Table D-3. Milliamp Input, <R1> Core, TBQC Board Location 9

	Generic Signal Name (from left column of IO.ASG file)	Signal Termination Points			JB Pin Numbers		Hardware Jumper BJ
		POS	NEG	EXC			
<R1> Core	Q1TCQA_MAI01	35	36	37	1	2	1
TBQC Board Location 9	Q1TCQA_MAI02	39	40	38	3	4	2
	Q1TCQA_MAI03	41	42	43	5	6	3
	Q1TCQA_MAI04	45	46	44	7	8	4
	Q1TCQA_MAI05	47	48	49	9	10	5
	Q1TCQA_MAI06	51	52	50	11	12	6
	Q1TCQA_MAI07	53	54	55	13	14	7
	Q1TCQA_MAI08	57	58	56	15	16	8
	Q1TCQA_MAI09	59	60	61	17	18	9
	Q1TCQA_MAI10	63	64	62	19	20	10
	Q1TCQA_MAI11	65	66	67	21	22	11
	Q1TCQA_MAI12	69	70	68	23	24	12
	Q1TCQA_MAI13	71	72	73	25	26	13
	Q1TCQA_MAI14	75	76	74	27	28	14
	Q1TCQA_MAI15	77	78	79	29	30	15

Table D-4. Milliamp Input, <R2> Core, TBQC Board Location 9

	Generic Signal Name (from left column of IO.ASG file)	Signal Termination Points			JB Pin Numbers		Hardware Jumper BJ
		POS	NEG	EXC			
<R2> Core	Q2TCQA_MAI01	35	36	37	1	2	1
TBQC Board Location 9	Q2TCQA_MAI02	39	40	38	3	4	2
	Q2TCQA_MAI03	41	42	43	5	6	3
	Q2TCQA_MAI04	45	46	44	7	8	4
	Q2TCQA_MAI05	47	48	49	9	10	5
	Q2TCQA_MAI06	51	52	50	11	12	6
	Q2TCQA_MAI07	53	54	55	13	14	7
	Q2TCQA_MAI08	57	58	56	15	16	8
	Q2TCQA_MAI09	59	60	61	17	18	9
	Q2TCQA_MAI10	63	64	62	19	20	10
	Q2TCQA_MAI11	65	66	67	21	22	11
	Q2TCQA_MAI12	69	70	68	23	24	12
	Q2TCQA_MAI13	71	72	73	25	26	13
	Q2TCQA_MAI14	75	76	74	27	28	14
	Q2TCQA_MAI15	77	78	79	29	30	15

Table D-5. Milliamp Input, <R3> Core, TBQC Board Location 9

	Generic Signal Name (from left column of IO.ASG file)	Signal Termination Points			JB Pin Numbers		Hardware Jumper BJ
		POS	NEG	EXC			
<R3> Core	Q3TCQA_MAI01	35	36	37	1	2	1
TBQC Board Location 9	Q3TCQA_MAI02	39	40	38	3	4	2
	Q3TCQA_MAI03	41	42	43	5	6	3
	Q3TCQA_MAI04	45	46	44	7	8	4
	Q3TCQA_MAI05	47	48	49	9	10	5
	Q3TCQA_MAI06	51	52	50	11	12	6
	Q3TCQA_MAI07	53	54	55	13	14	7
	Q3TCQA_MAI08	57	58	56	15	16	8
	Q3TCQA_MAI09	59	60	61	17	18	9
	Q3TCQA_MAI10	63	64	62	19	20	10
	Q3TCQA_MAI11	65	66	67	21	22	11
	Q3TCQA_MAI12	69	70	68	23	24	12
	Q3TCQA_MAI13	71	72	73	25	26	13
	Q3TCQA_MAI14	75	76	74	27	28	14
	Q3TCQA_MAI15	77	78	79	29	30	15

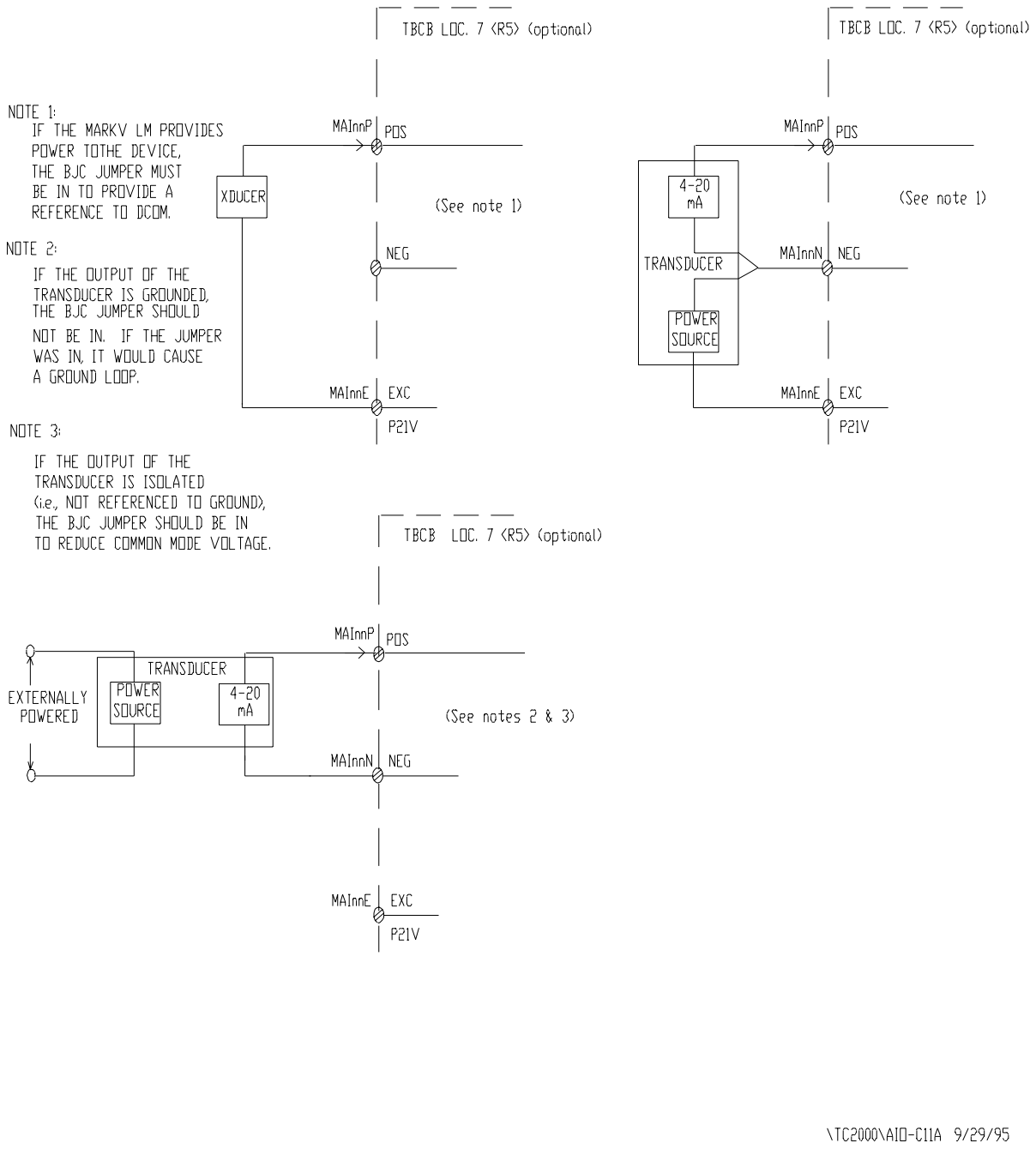


Figure D-1. Milliamp Input Connection Examples and Notes

Note Refer to the tables D-1 through D-5 for connection points and hardware jumpers.

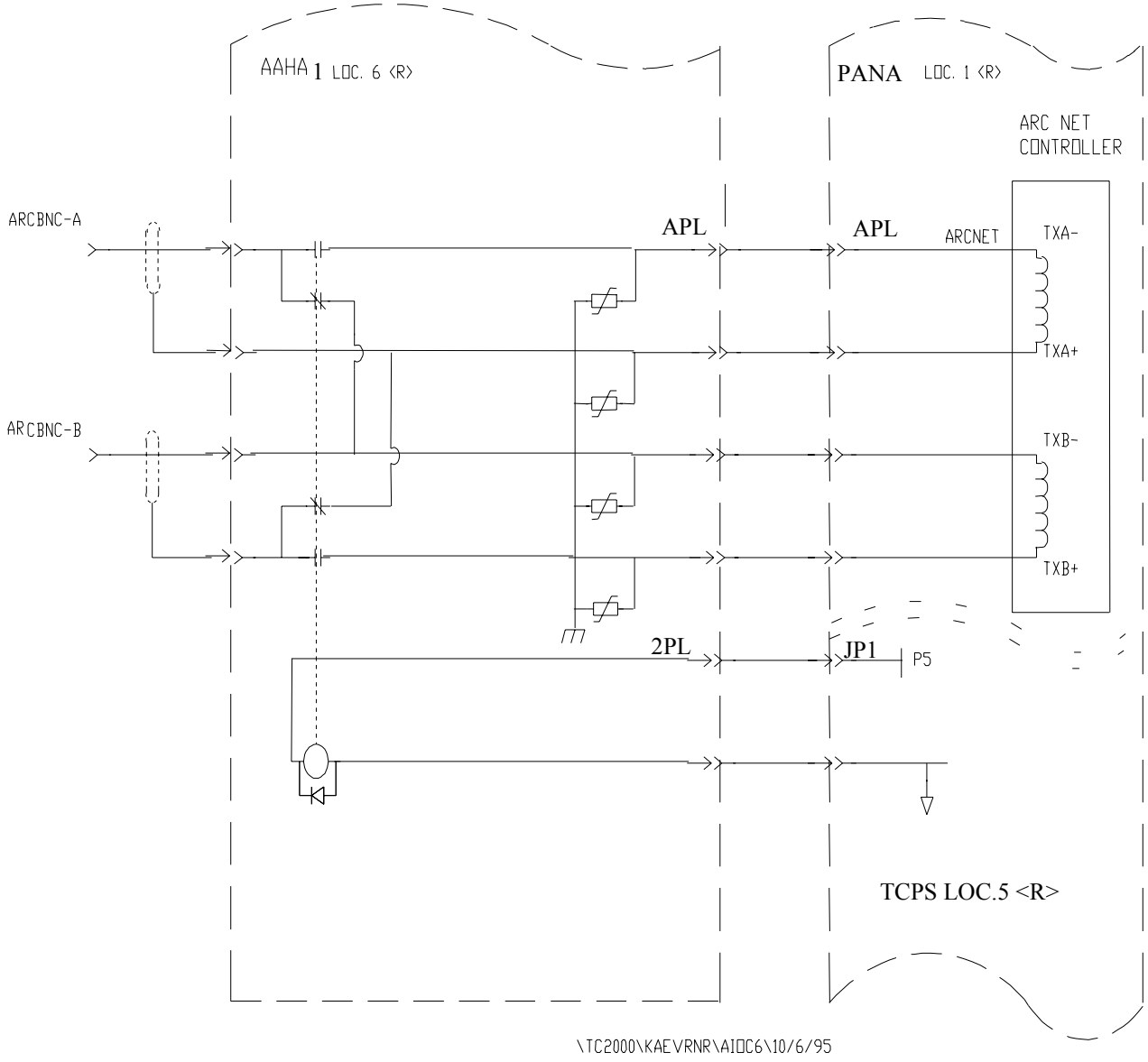


Figure D-2. <R> Core – Stage Link Connections AAHAI/PANA

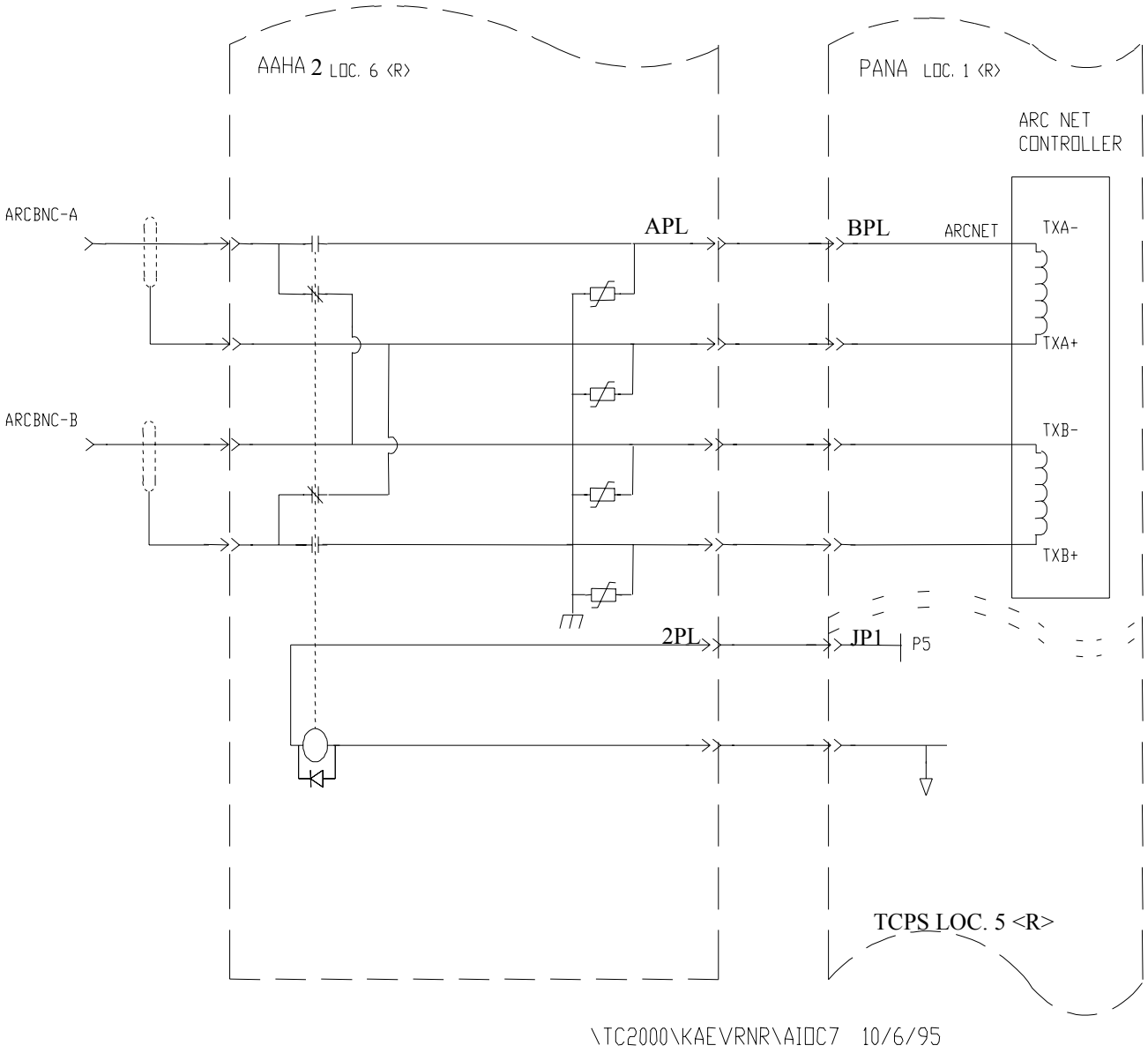
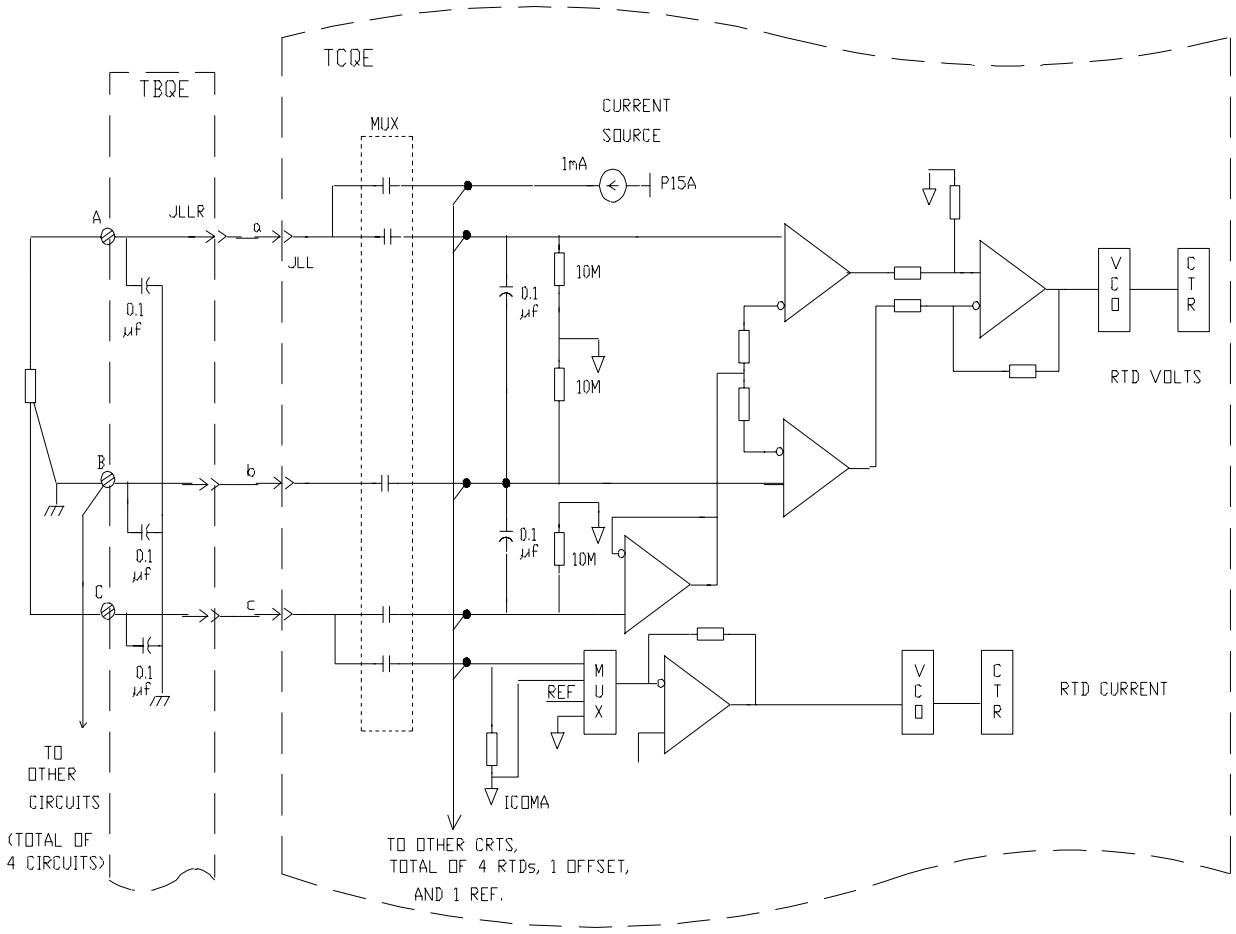


Figure D-3. <R> Core – COREBUS Connections AAHA2/PANA



DEVICE	TERMINATION TBCB			JLLR		
	A	B	C	a	b	c
RTD1	61	62	63	23	24	25
RTD2	64	65	66	26	27	28
RTD3	67	68	69	29	30	31
RTD4	70	71	72	32	33	34
				JLLS		
RTD5	73	74	75	23	24	25
RTD6	76	77	78	26	27	28
				JLLT		
RTD7	79	80	81	23	24	25
RTD8	82	83	84	26	27	28

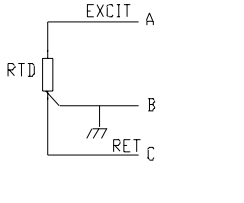


Figure D-4. <R1> Core – RTD Inputs TBQE/TCQE

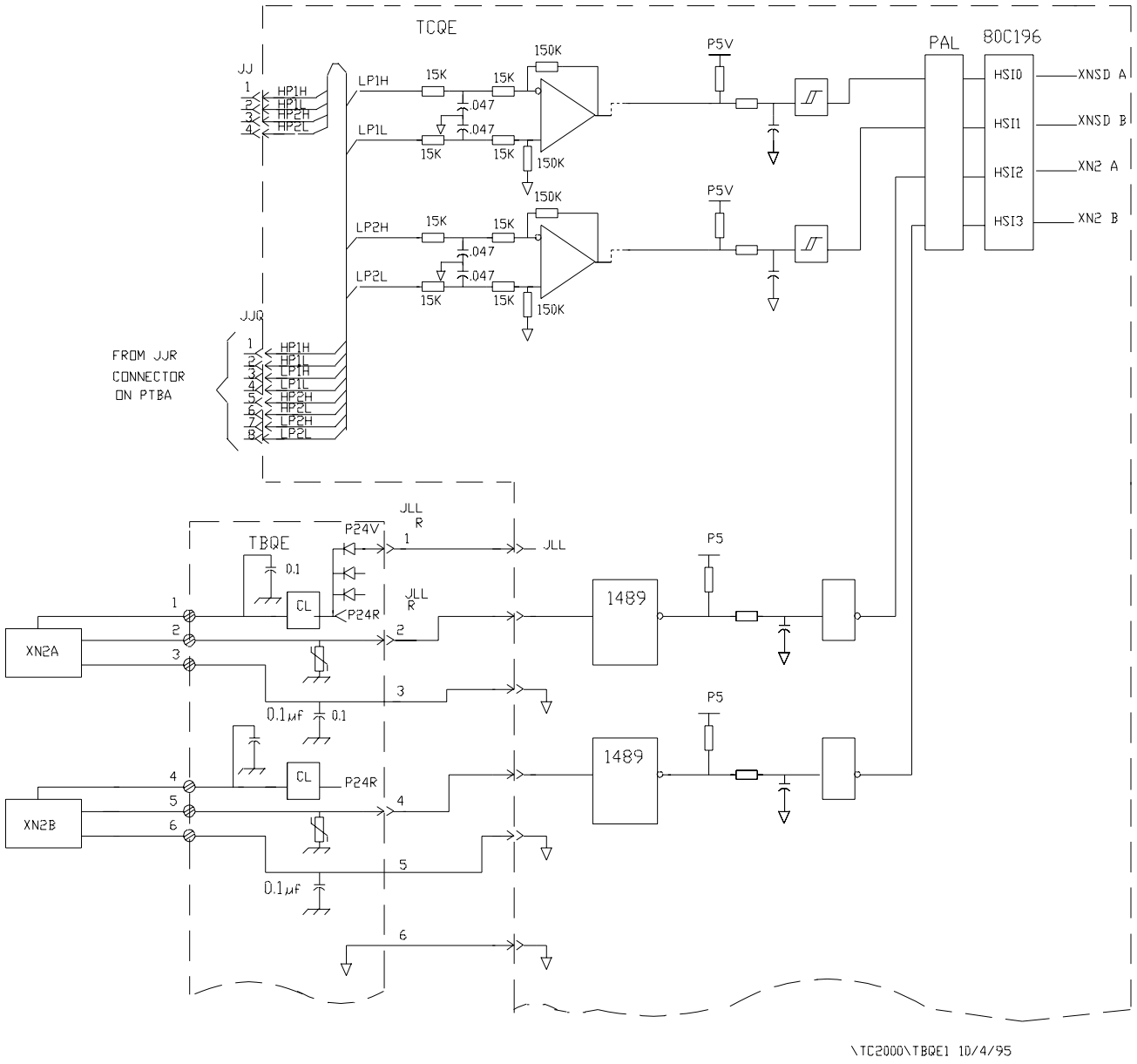
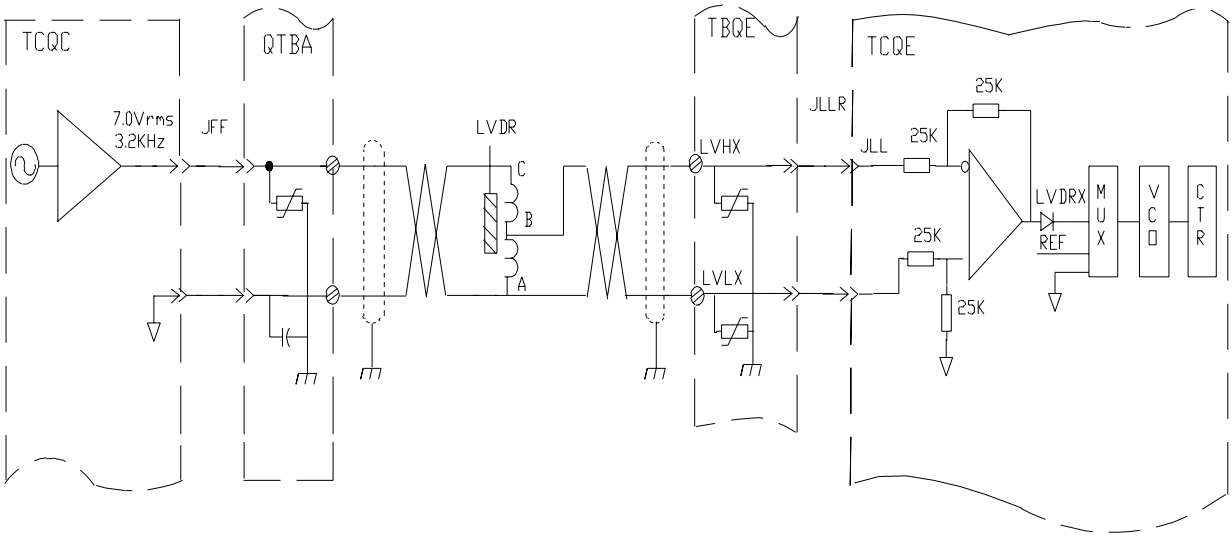


Figure D-5. <R1> Core – Pulse Rate Inputs on TBQE



DEVICE	INPUT (TBQE) TERMINATION	EXCITATION (QTBA) TERMINATION	JLL PIN #	COMMENT
LVDR17	7,8	<S> 13,14	7,8	
LVDR18	9,10	<T> 13,14	9,10	
LVDR19	11,12	<R> 15,16	11,12	
LVDR20	13,14	<S> 15,16	13,14	

\TC2000\TBQE2 10/4/95

Figure D-6. <R1> Core – LVDT/R Excitation and Feedback Signal on QTBA/TBQE

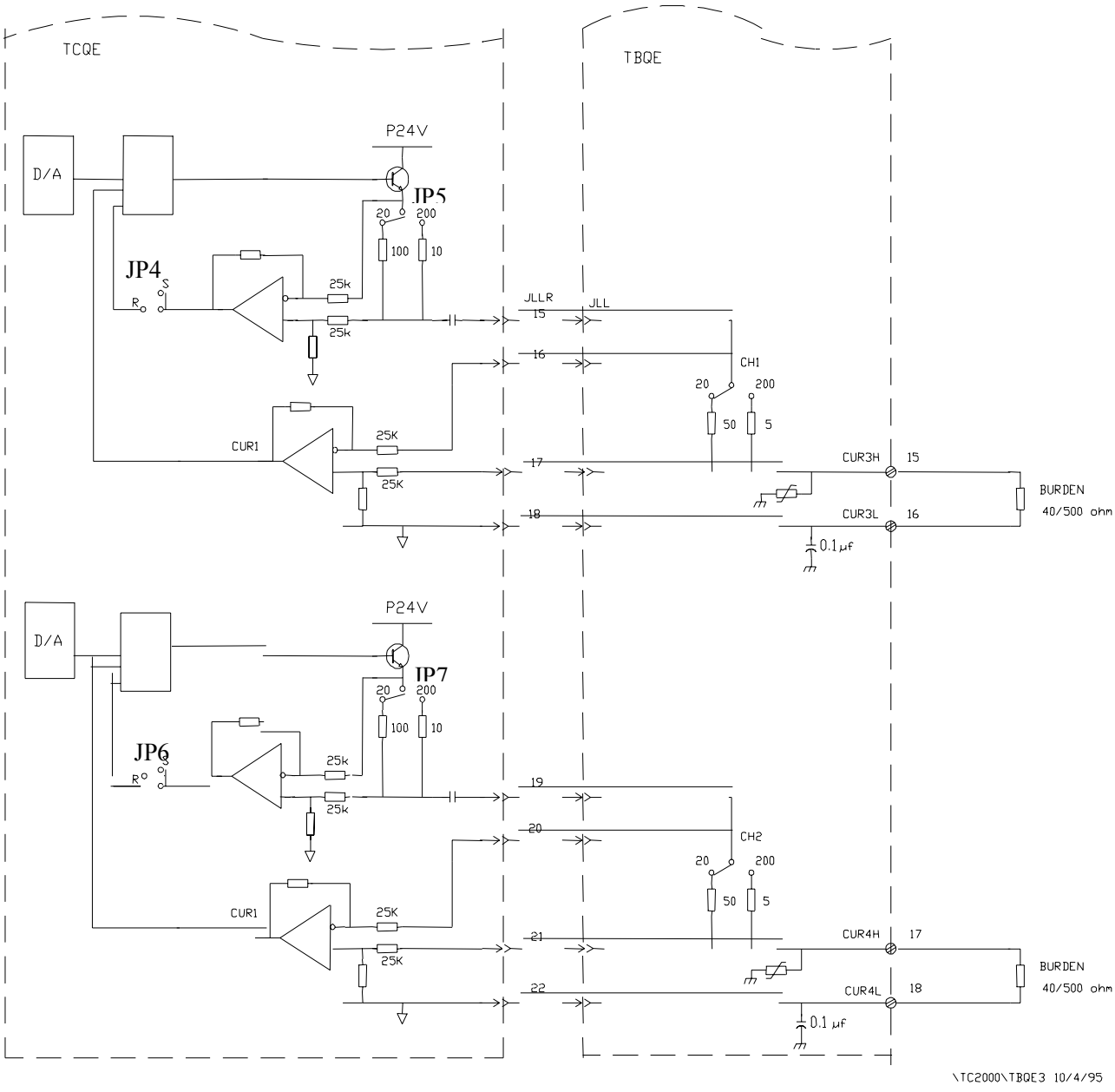


Figure D-7. <R1> Core – 4–20/200 mA Outputs on TBQE

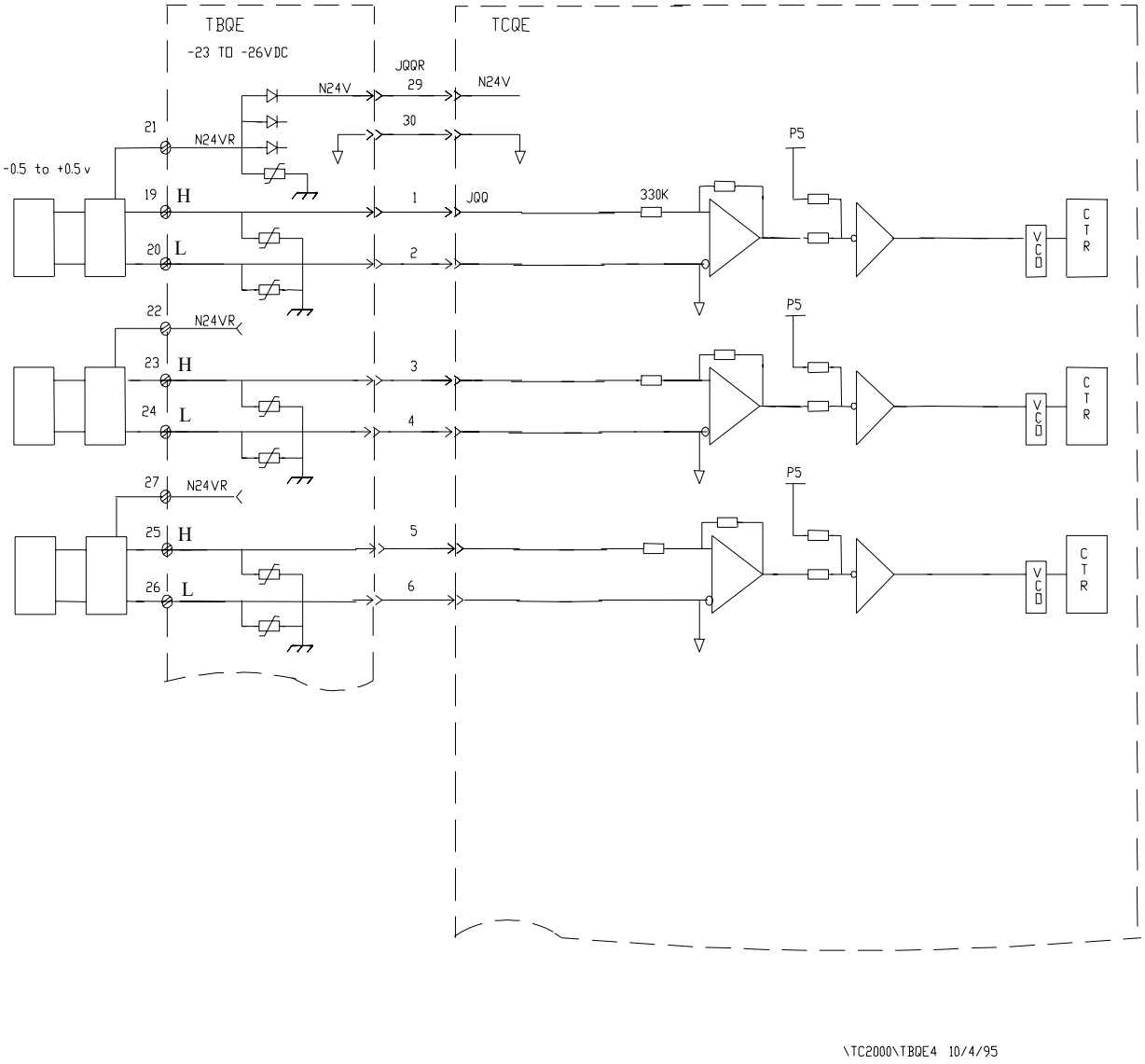
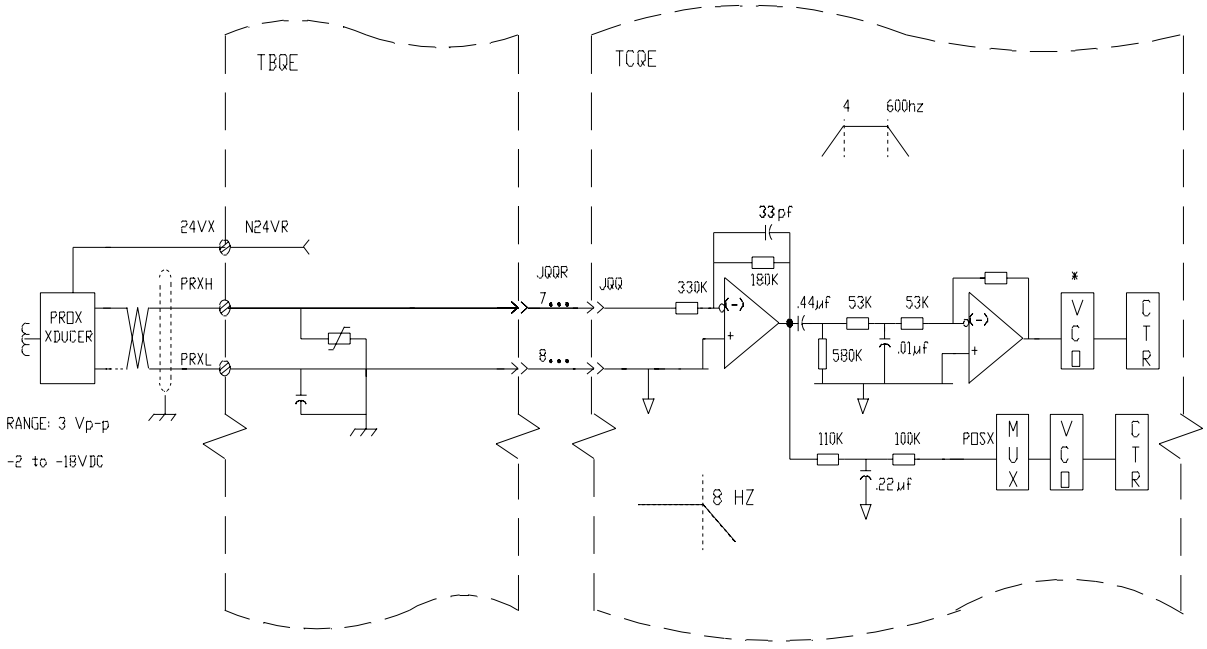


Figure D-8. <R1> Core – Vibration Inputs on TBQE

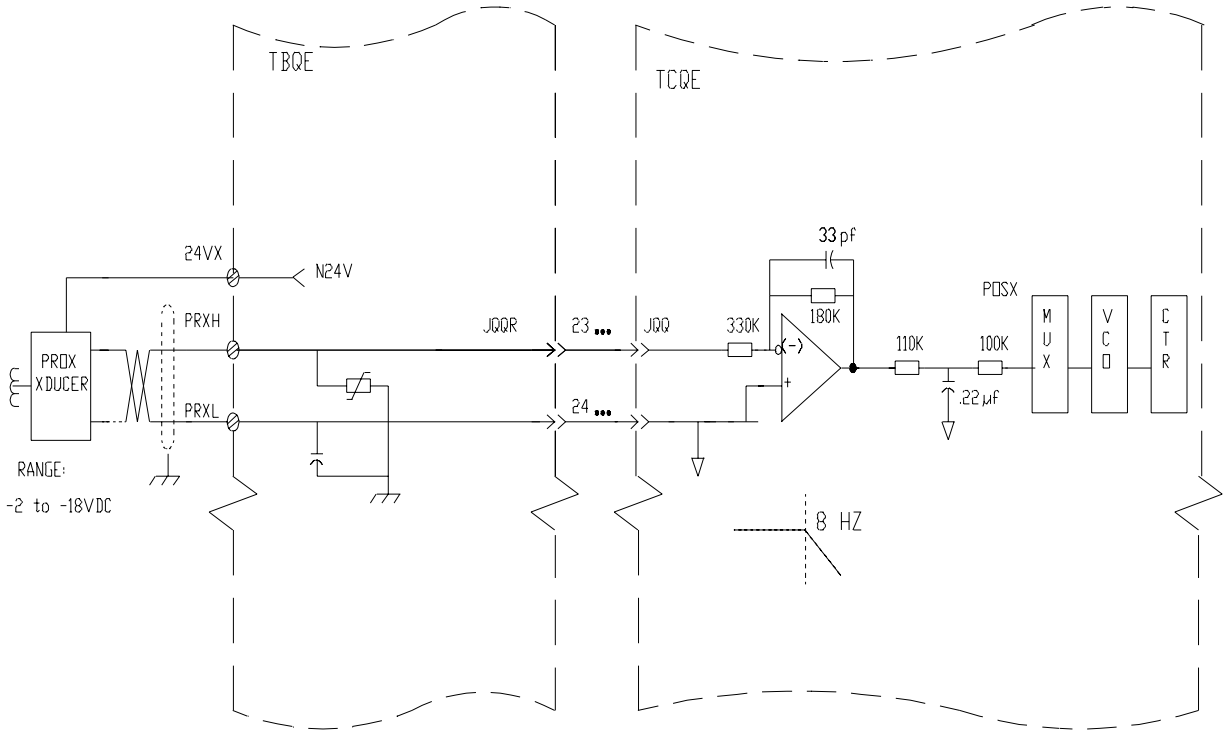


24XV

DEVICE	SIGNAL TERMINATION PRXH	SIGNAL TERMINATION PRXL	EXCITATION TERMINATION	JKK
PROX1	29	30	28	7,8
PROX2	31	32	33	9,10
PROX3	35	36	34	11,12
PROX4	37	38	39	13,14
PROX5	41	42	40	15,16
PROX6	43	44	45	17,18
PROX7	47	48	46	19,20
PROX8	49	50	51	21,22

\TC2000\TBQE5 10/4/95

Figure D-9. <R1> Core – Proximity Transducer Inputs on TBQE

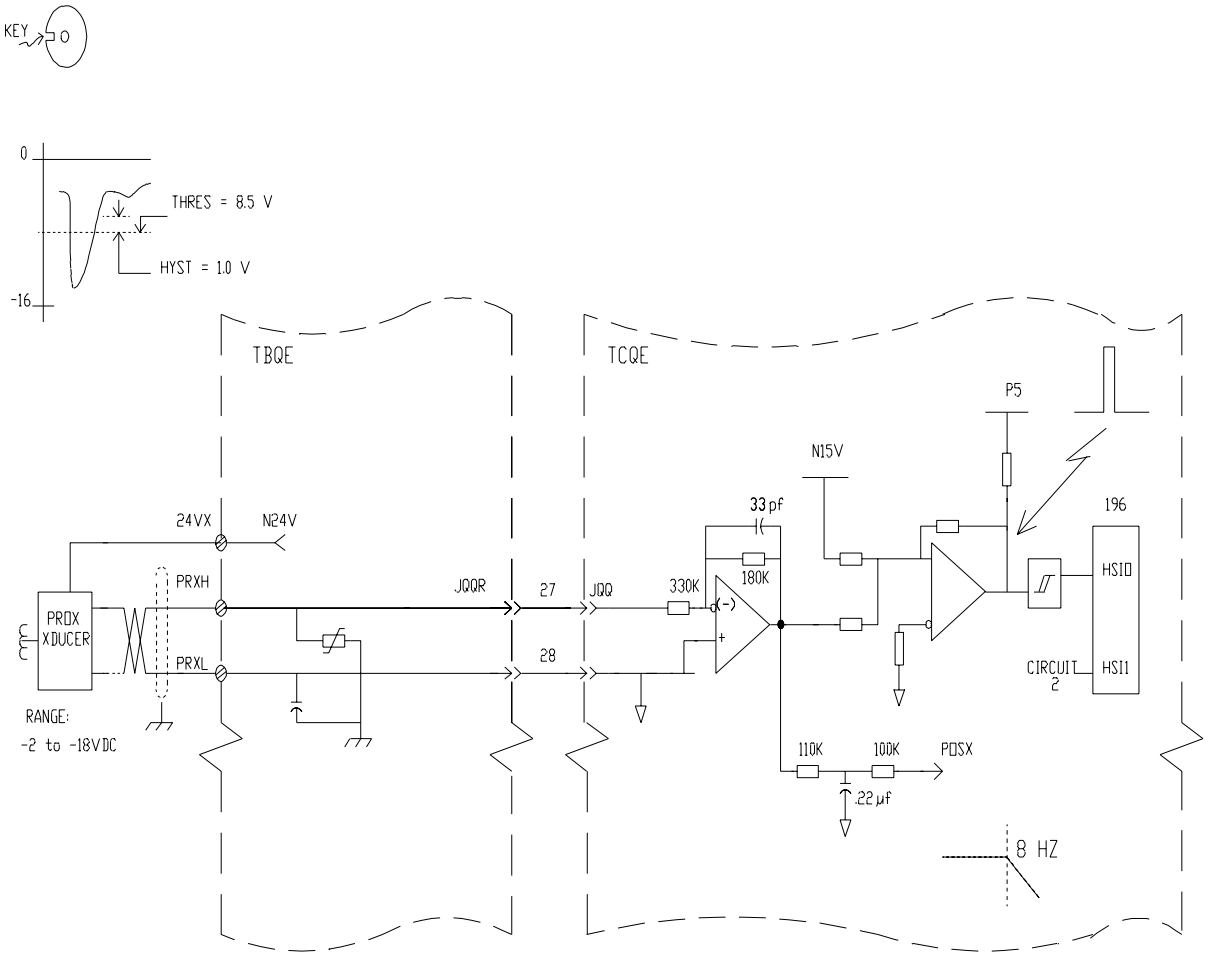


24VX

DEVICE	SIGNAL TERMINATION PRXH	SIGNAL TERMINATION PRXL	EXCITATION TERMINATION	JKK
PROX9	53	54	52	23,24
PROX10	55	56	57	25,26

\TC2000\TBQE6 10/4/95

Figure D-10. <R1> Core – Proximity Transducer Inputs on TBQE



DEVICE	SIGNAL TERMINATION		24VX EXCITATION TERMINATION	COMMENT	JKK
	PRXH	PRXL			
PROX11	59	60	58	GEN SHAFT	27,28

\TC2000\TBQE7 10/4/95

Figure D-11. <R1> Core – Proximity Transducer Inputs on TBQE

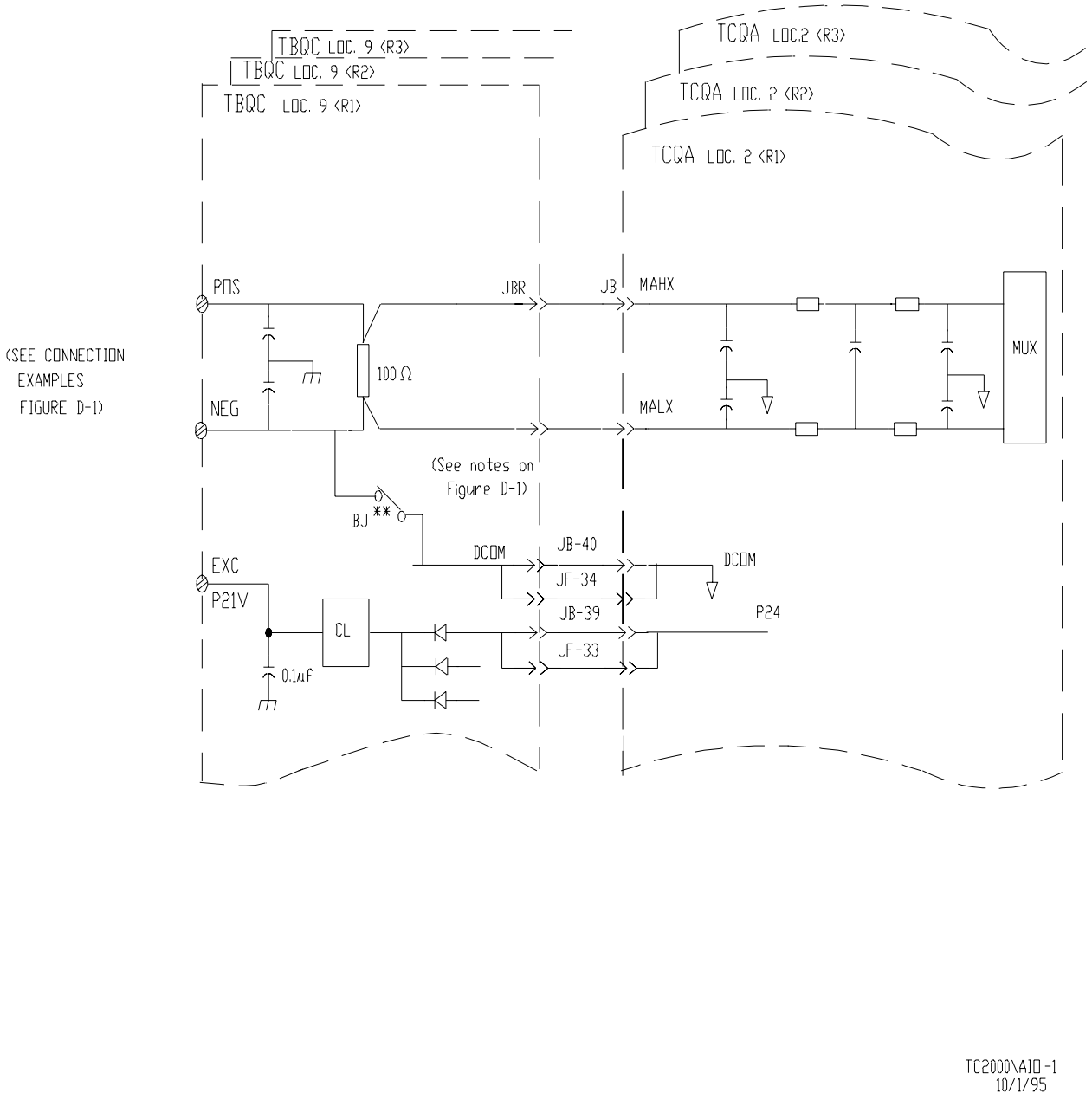


Figure D-12. <R1>, <R2>, and <R3> Cores: 4 – 20 mA Inputs on TBQC

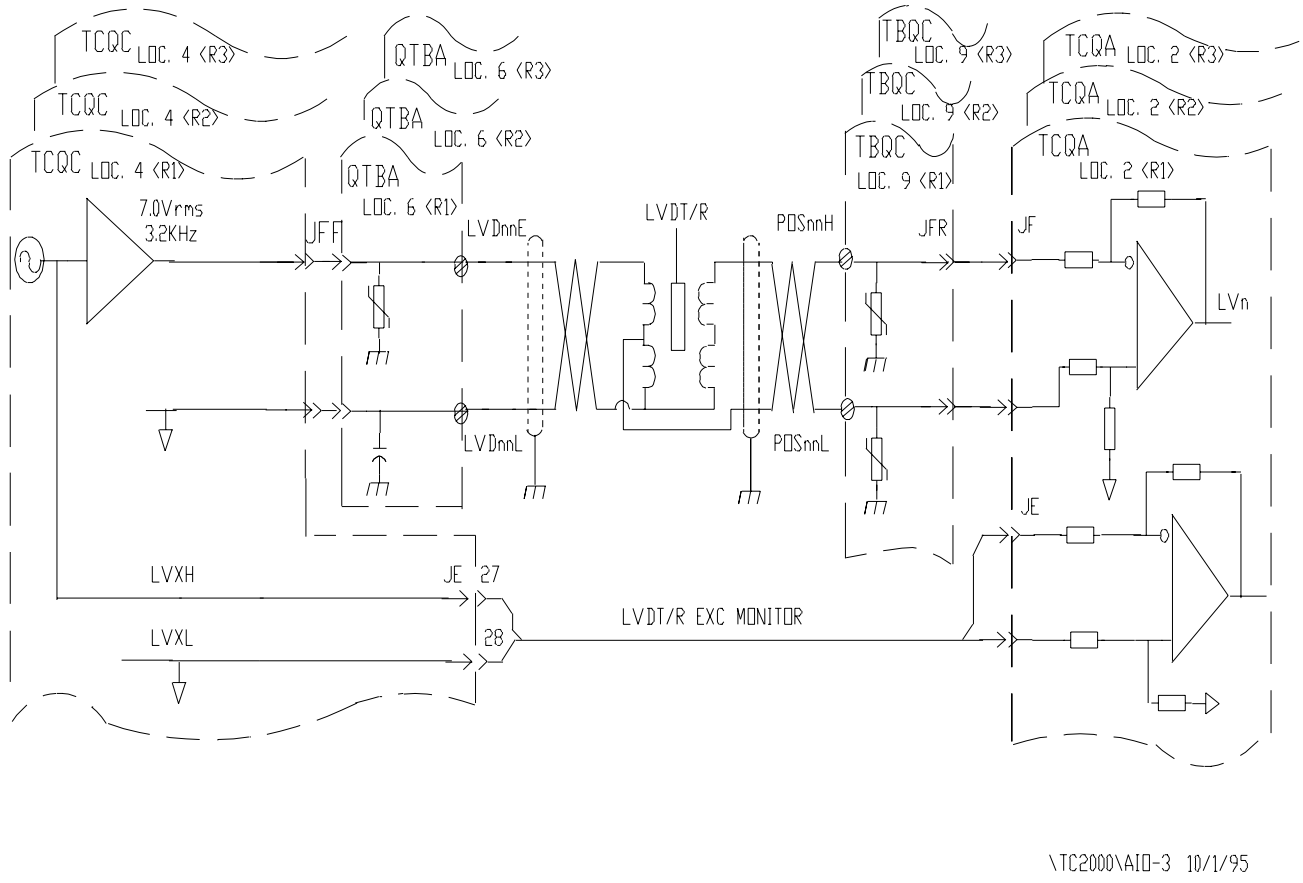


Figure D-13. <R1>, <R2>, and <R3> Cores: LVDT/R Excitation and Feedback on QTBA/TBQC

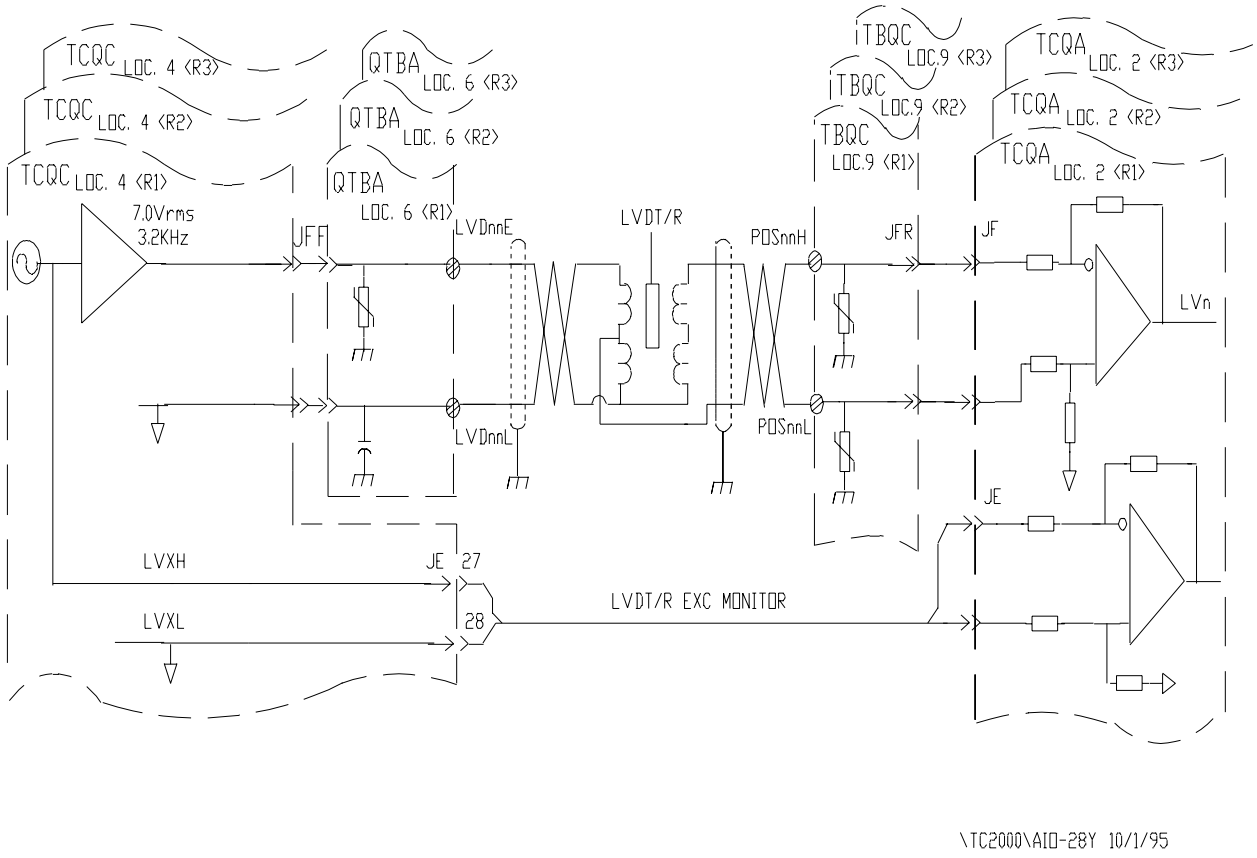
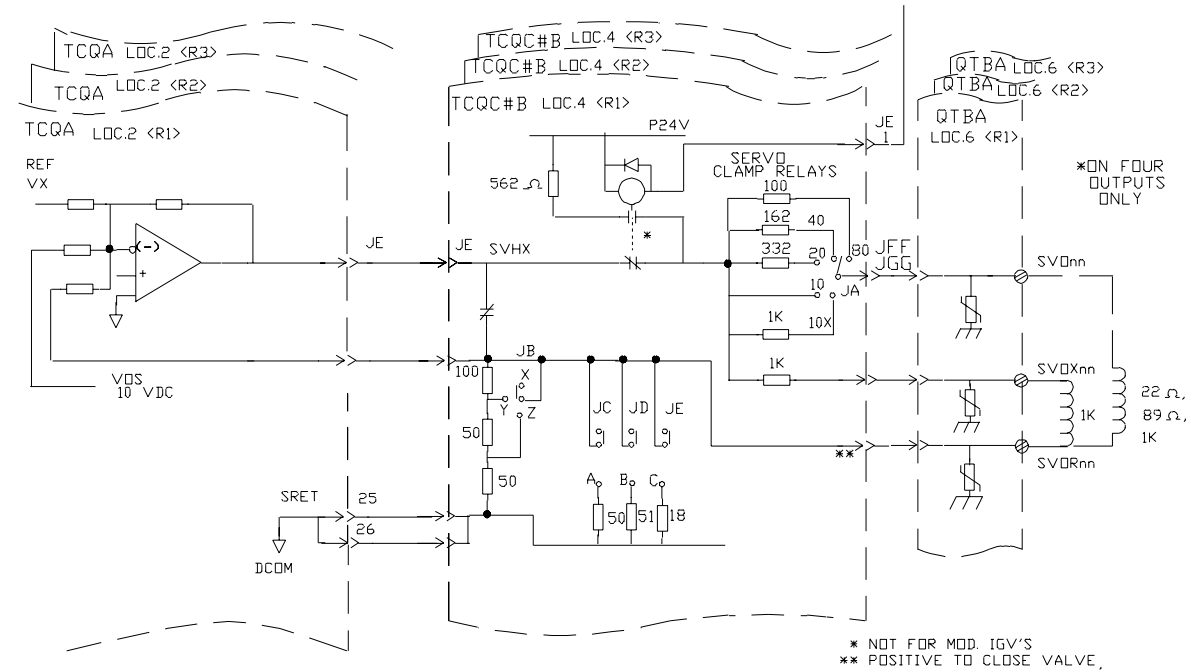
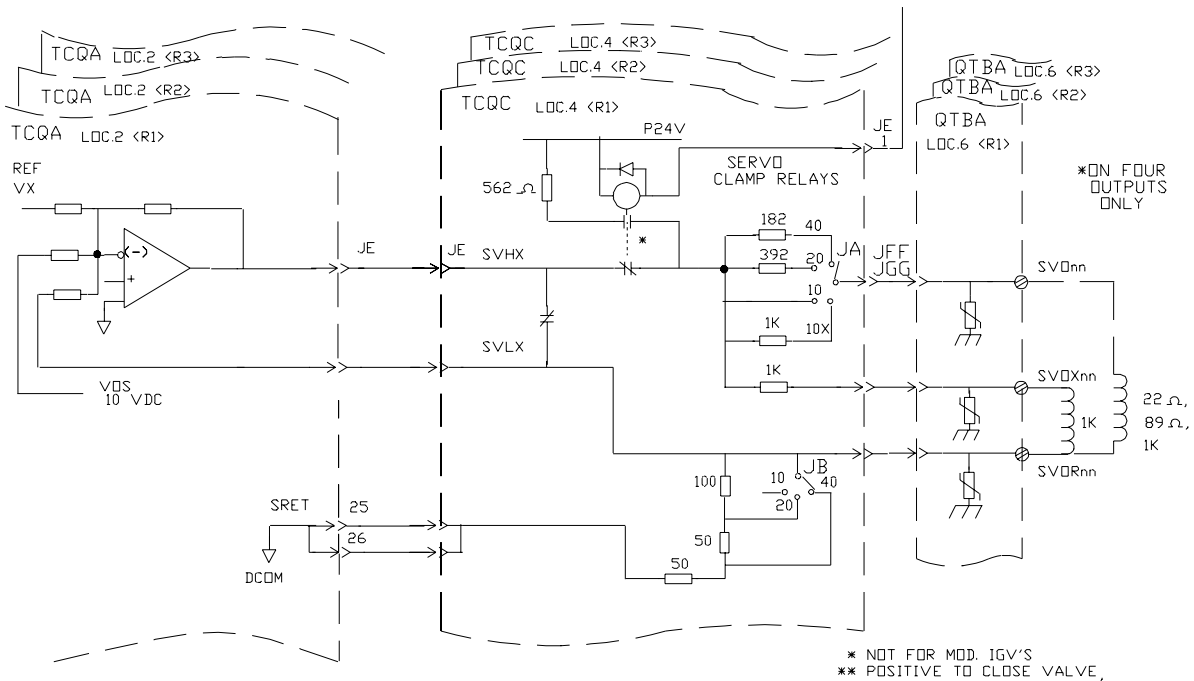


Figure D-14. <R1>, <R2>, and <R3> Cores: LVDT/R Excitation and Feedback on QTBA/TBQC



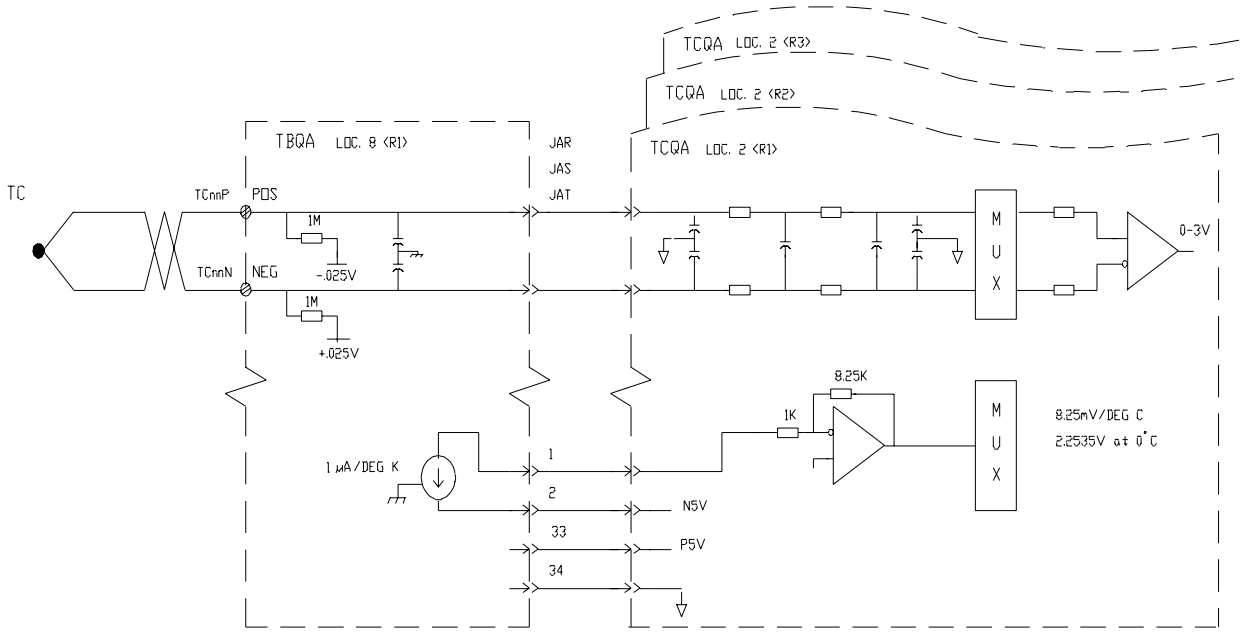
DEVICE	TERMINATION SCREWS			JE (TCQC) JE (TCQA)		JUMPERS				
	SVOnn**	SVOXnn	SVORnn	SVLX	SVHX	JA	JB	JC	JD	JE
* SV01	27	28	29	10	9	BJ1	BJ2	BJ25	BJ26	BJ27
* SV02	30	31	32	12	11	BJ3	BJ4	BJ28	BJ29	BJ30
* SV03	33	34	35	14	13	BJ5	BJ6	BJ31	BJ32	BJ33
* SV04	36	37	38	16	15	BJ7	BJ8	BJ34	BJ35	BJ36

Figure D-15. <R1>, <R2>, and <R3> Cores: Servo Outputs on QTBA/TCQC



DEVICE	TERMINATION SCREWS			JE (TCQC) JE (TCQA)		JUMPERS	
	SVOnn**	SVOXnn	SVORnn	SVLX	SVHX	JA	JB
SV05	39	40	41	18	17	BJ9	BJ10
SV06	42	43	44	20	19	BJ11	BJ12
SV07	45	46	47	22	21	BJ13	BJ14
SV08	48	49	50	24	23	BJ15	BJ16

Figure D-16. <R1>, <R2> and, <R3> Cores: Servo Outputs on QTBA/TCQC



<R1> DEVICE	TBQA TERMINATION		<R2> DEVICE	TBQA TERMINATION		<R3> DEVICE	TBQA TERMINATION	
TB DESIGNATION	POS	NEG	TB DESIGNATION	POS	NEG	TB DESIGNATION	POS	NEG
TC01	1	2	TC16	31	32	TC31	61	62
TC02	3	4	TC17	33	34	TC32	63	64
TC03	5	6	TC18	35	36	TC33	65	66
TC04	7	8	TC19	37	38	TC34	67	68
TC05	9	10	TC20	39	40	TC35	69	70
TC06	11	12	TC21	41	42	TC36	71	72
TC07	13	14	TC22	43	44	TC37	73	74
TC08	15	16	TC23	45	46	TC38	75	76
TC09	17	18	TC24	47	48	TC39	77	78
TC10	19	20	TC25	49	50	TC40	79	80
TC11	21	22	TC26	51	52	TC41	81	82
TC12	23	24	TC27	53	54	TC42	83	84
TC13	25	26	TC28	55	56	TC43	85	86
TC14	27	28	TC29	57	58	TC44	87	88
TC15	29	30	TC30	59	60	TC45	89	90

\TC2000\AIO-11 10/1/95

Figure D-17. <R1>, <R2>, and <R3> Cores: Thermocouple Inputs on TBQA

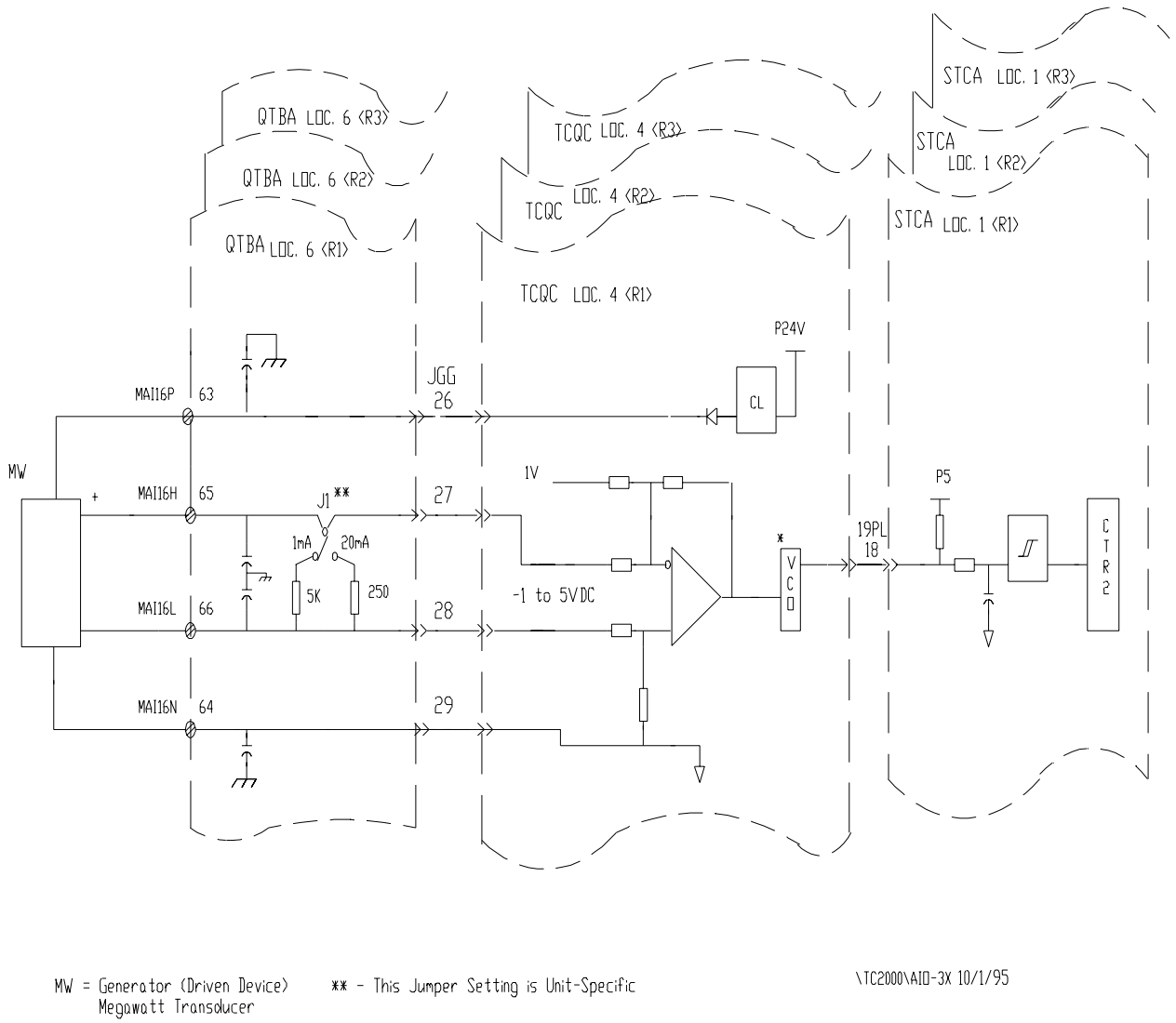


Figure D-18. <R1>, <R2>, and <R3> Cores: Megawatt Transducer Inputs on QTBA

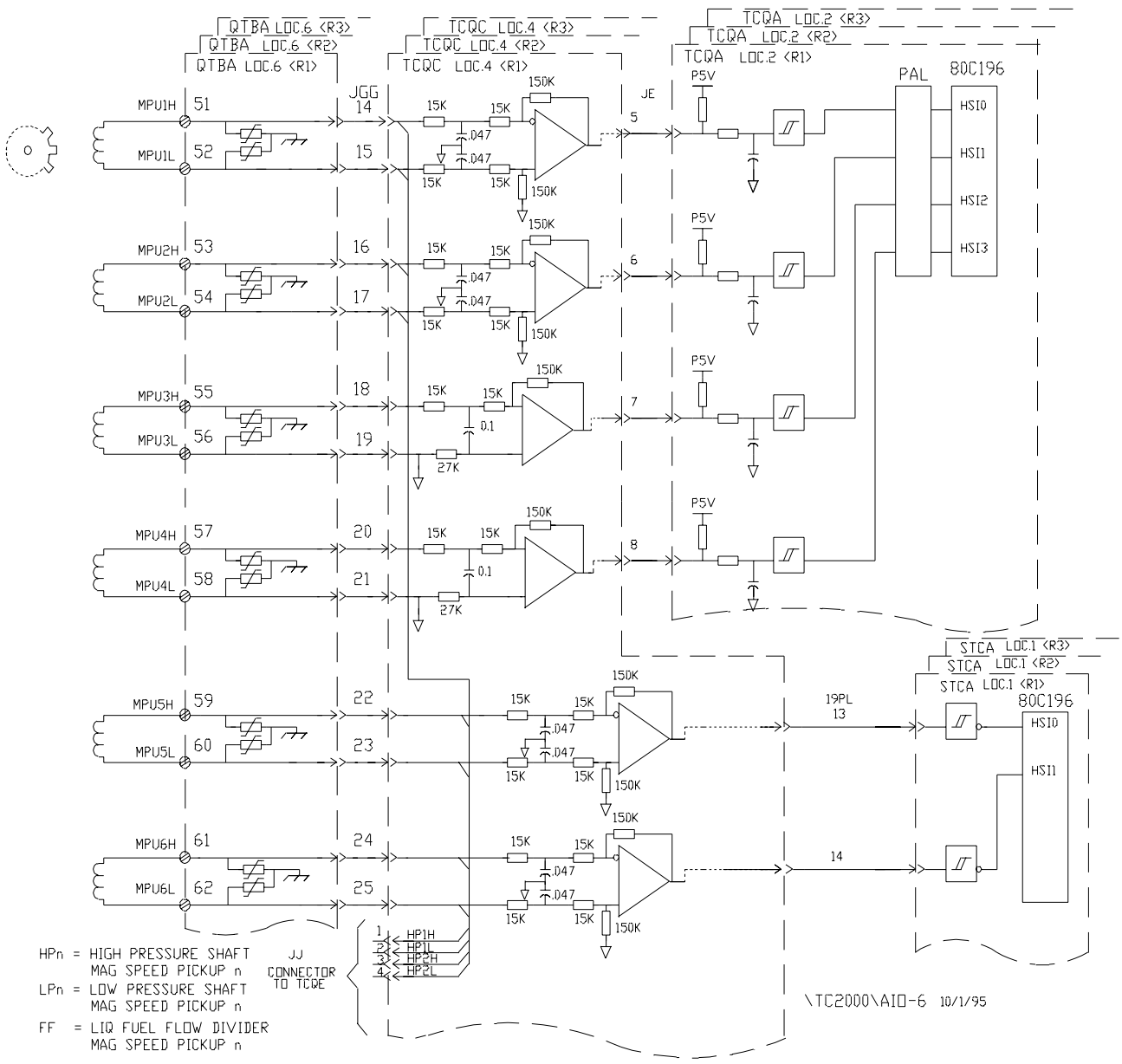


Figure D-19. <R1>, <R2>, and <R3> Cores: Pulse Rate Inputs on QTBA

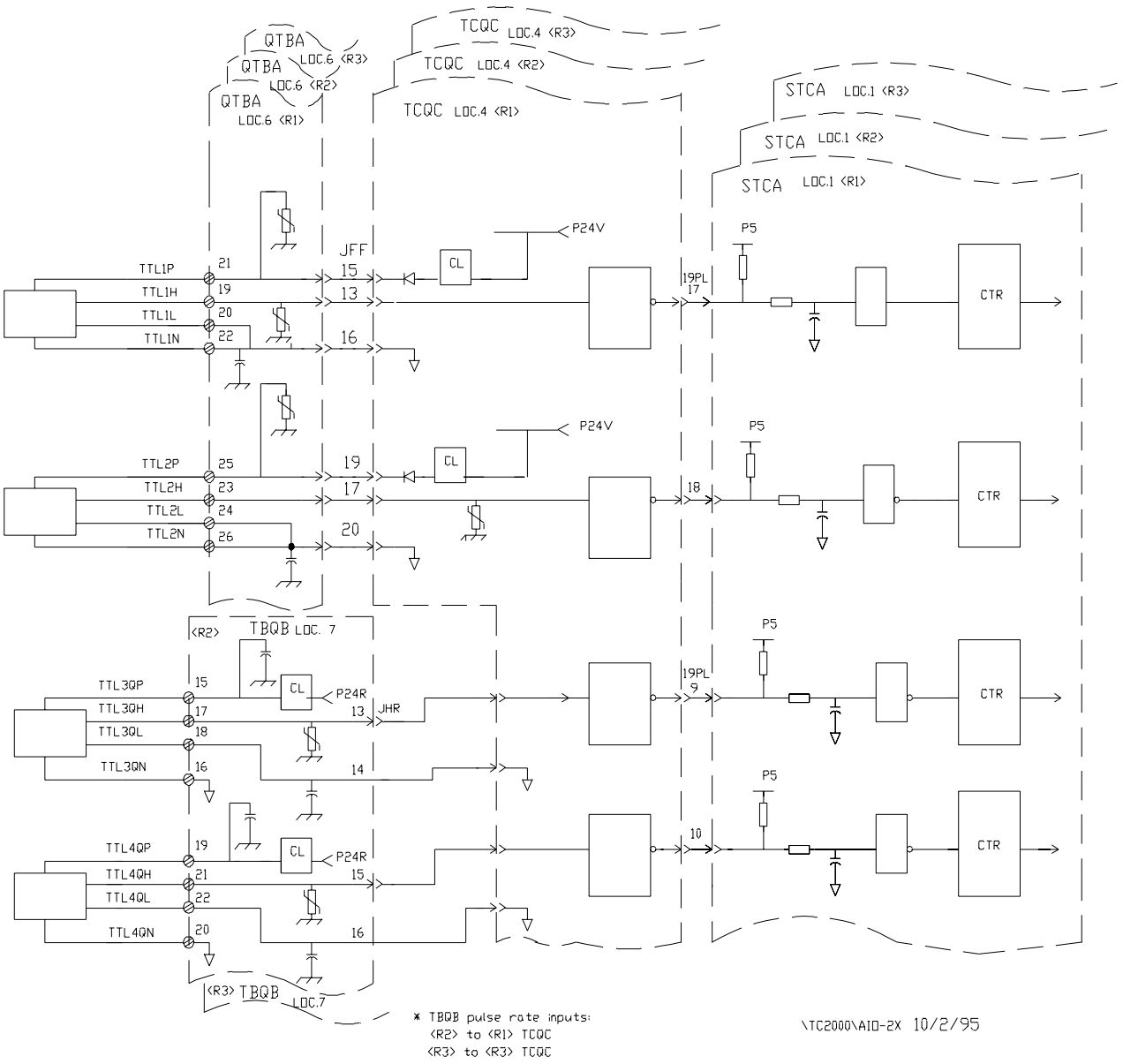


Figure D-20. <R1>, <R2> and <R3> Cores: Pulse Rate Inputs on QTBA

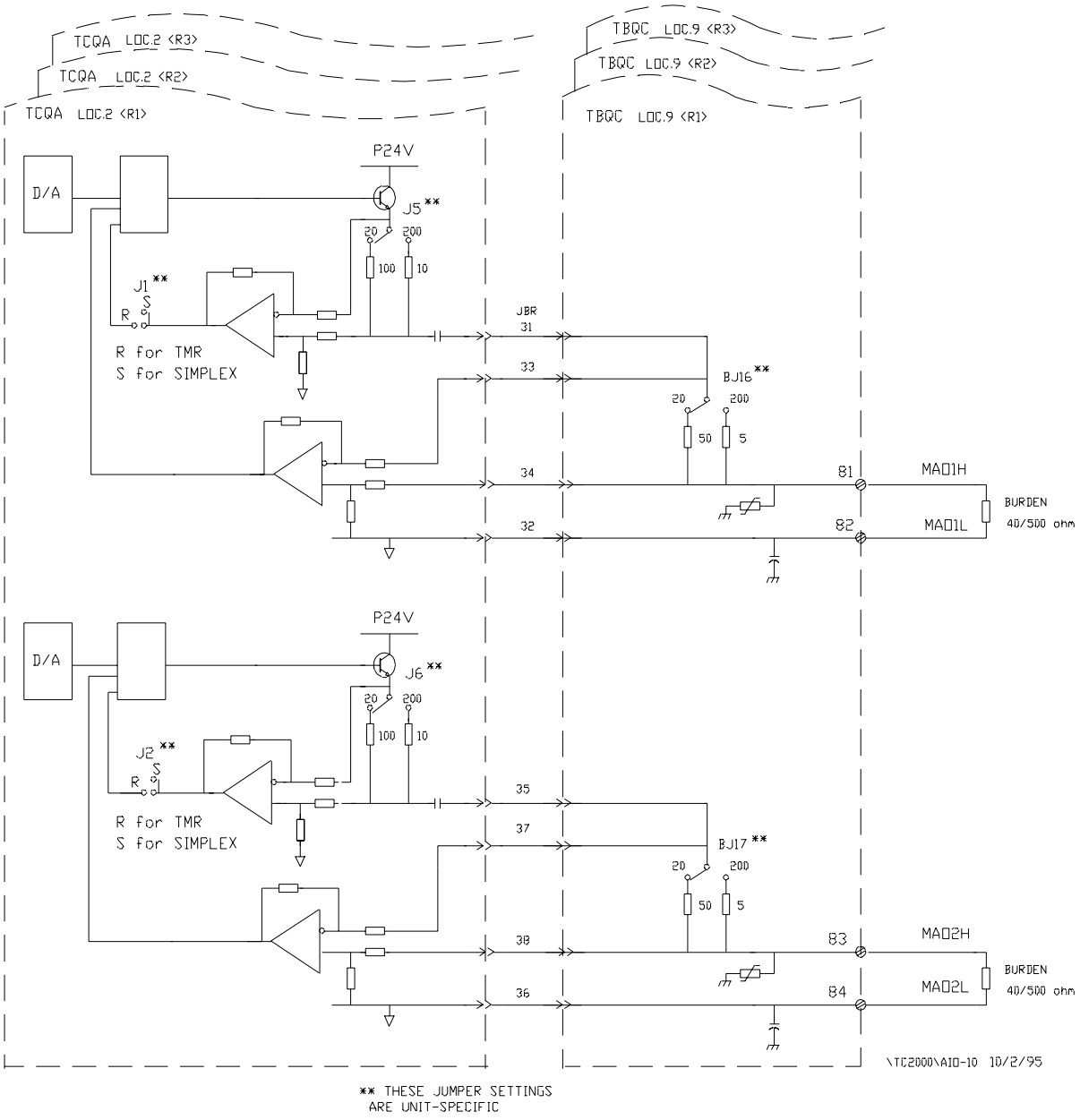


Figure D-21. <R1>, <R2> and <R3> Cores: 4 – 20 mA Outputs on TBQC

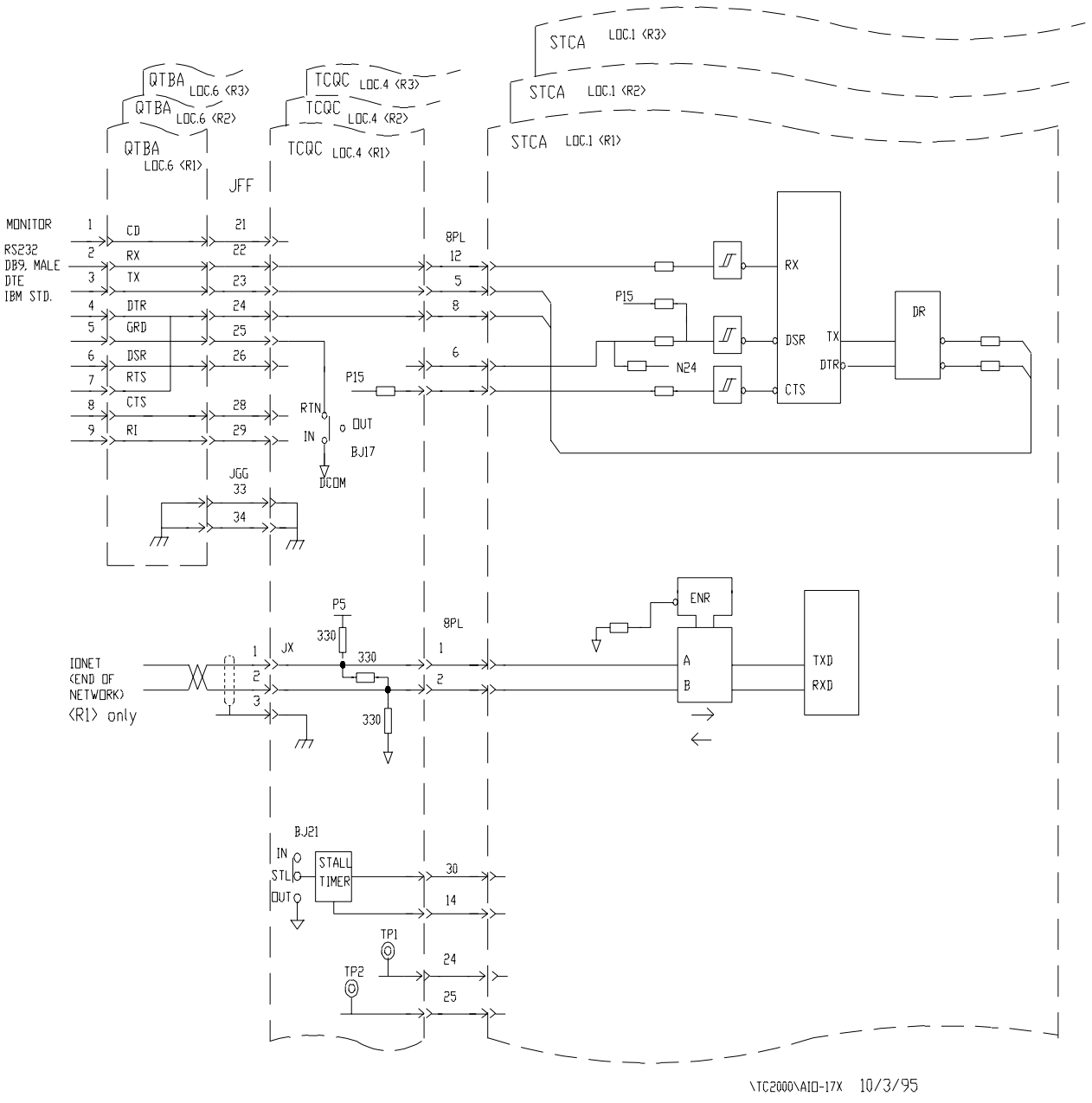


Figure D-22. <R1>, <R2>, and <R3> Cores: TIMN Monitor and IONET Connections on QTBA

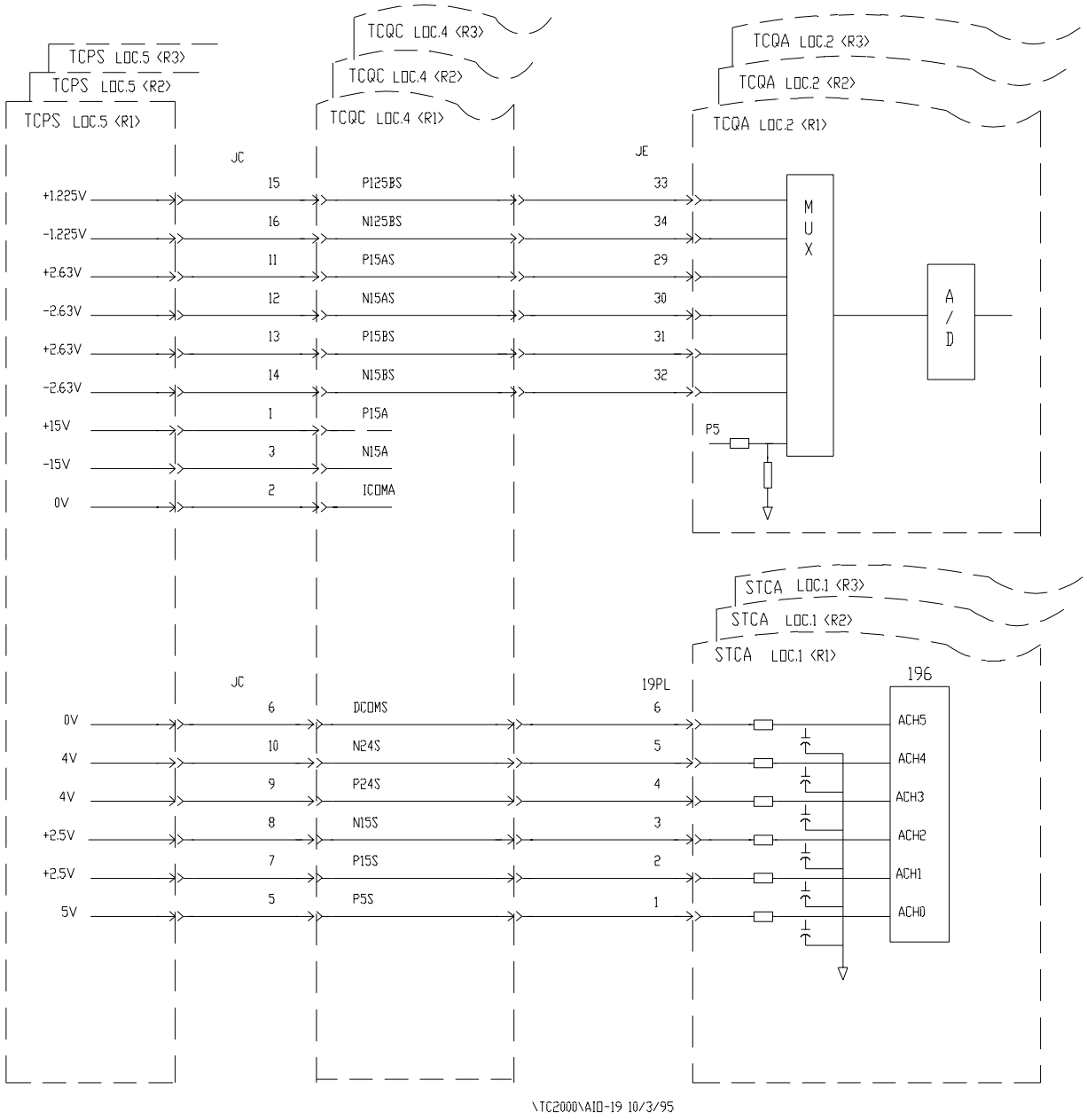
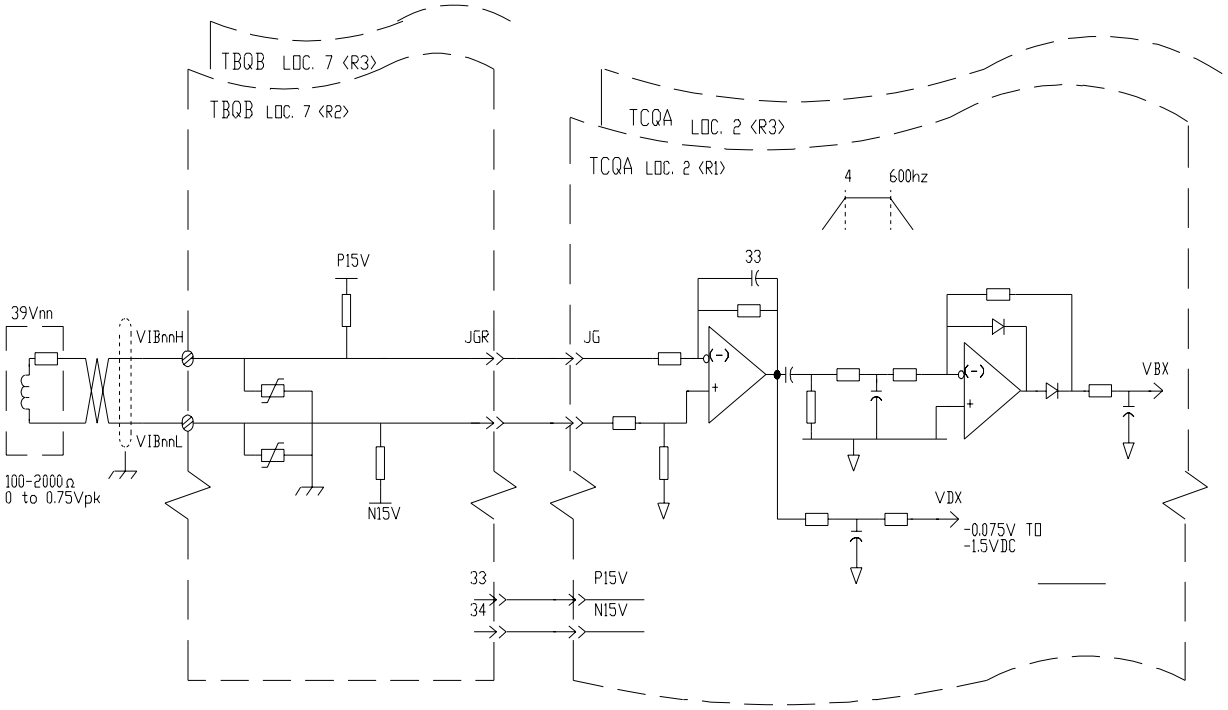


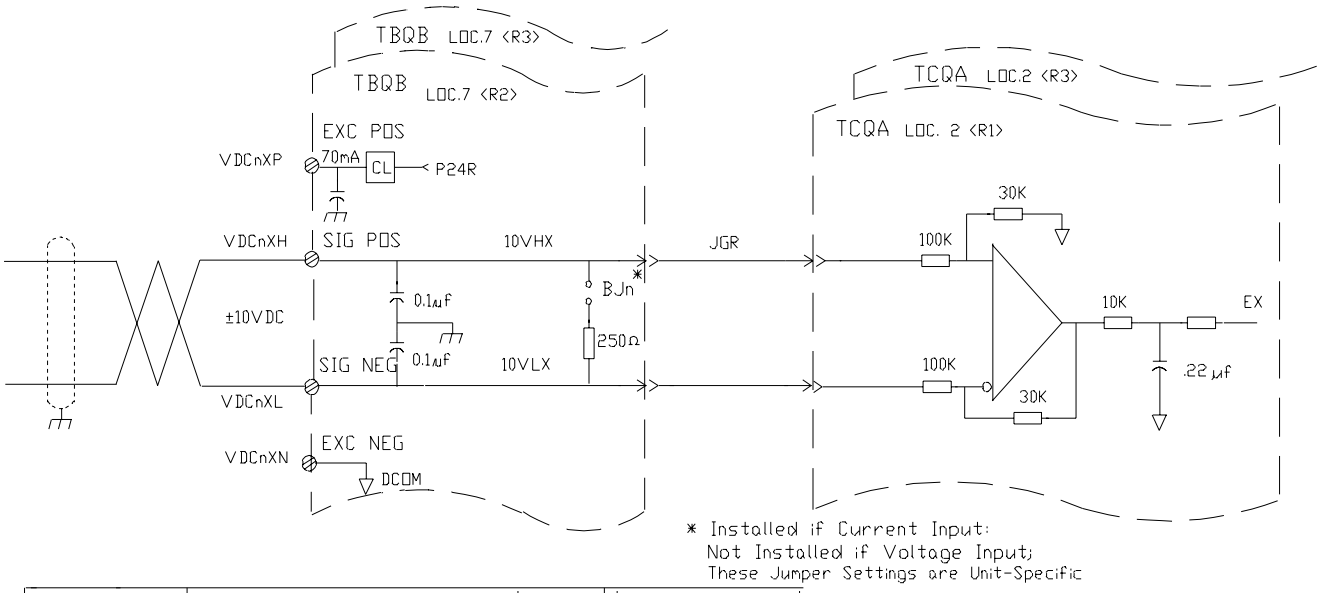
Figure D-23. <R1>, <R2>, and <R3> Cores: Power Supply Monitoring



\TC2000\AIO-7X 10/1/95

DEVICE TB DESIGNATION	TERMINATION SCREW VIBnnH VIBnnL	JG PIN #
39V01	51,52	9,10
39V02	53,54	11,12
39V03	55,56	13,14
39V04	57,58	15,16
39V05	59,60	17,18
39V06	61,62	19,20
39V07	63,64	21,22
39V08	65,66	23,24
39V09	67,68	25,26
39V10	69,70	27,28
39V11	71,72	29,30
39V12	73,74	31,32

Figure D-24. <R1> and <R3> Cores: Vibration Inputs on TBQB



DEVICE	TERMINATION, TBQB				BJn *	JG
	SIGNAL		EXCITATION			CONNECT PIN
TB DESIGNATION	POS	NEG	POS	NEG	JUMPERS	SIGNAL
VDC1	25	26	23	24	BJ8	JGR-1, 2
VDC2	37	38	35	36	BJ11	JGR-3, 4
VDC3	47	48	-	-	BJ14	JGR-5, 6
VDC4	49	50	-	-	BJ15	JGR-7, 8

\TC2000\AIO-6X 10/2/95

Figure D-25. <R1> and <R3> Cores: Analog Current and Voltage Inputs on TBQB

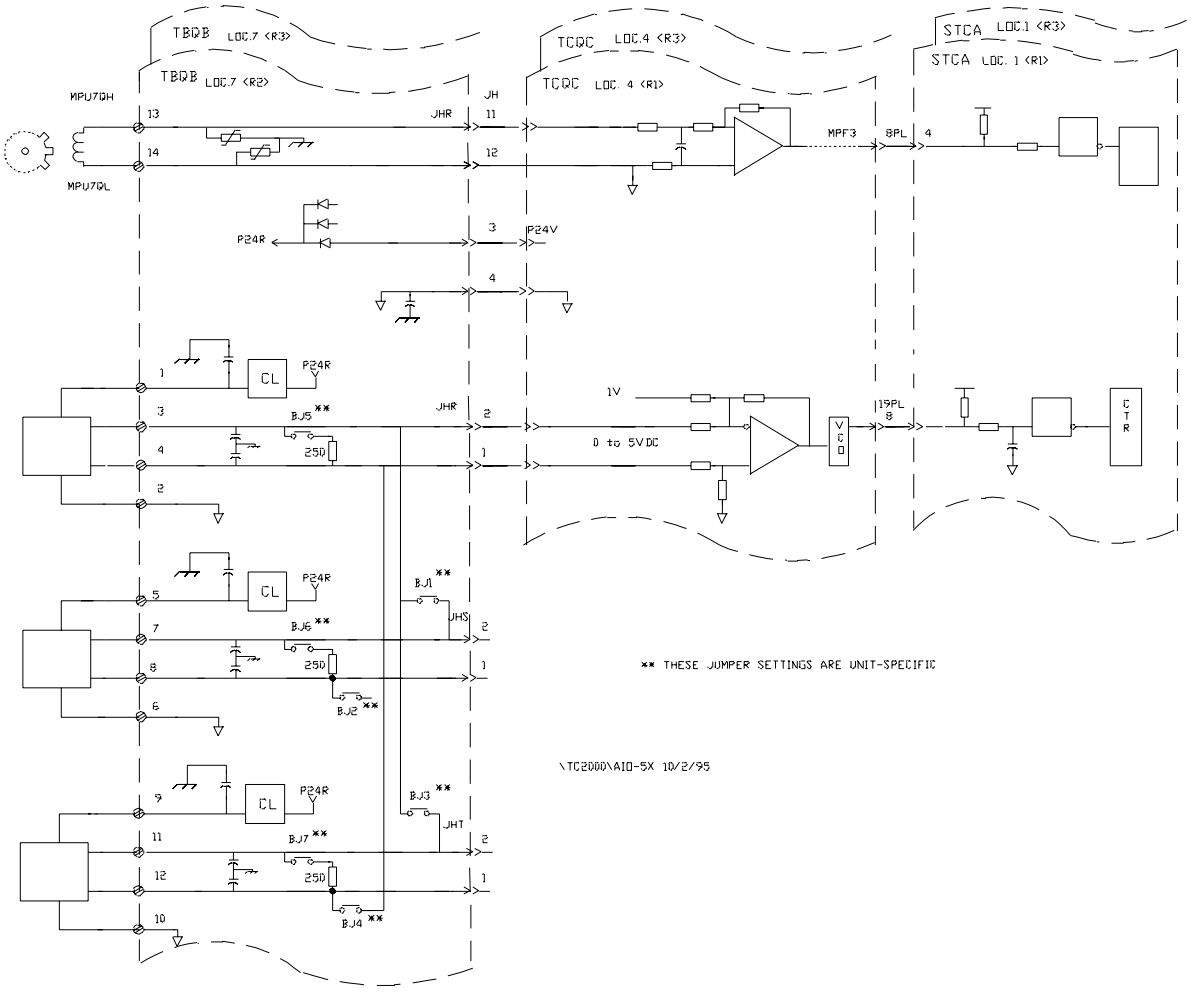


Figure D-26. <R1> and <R3> Cores: Pulse Inputs/Milliamp Input on TBQB

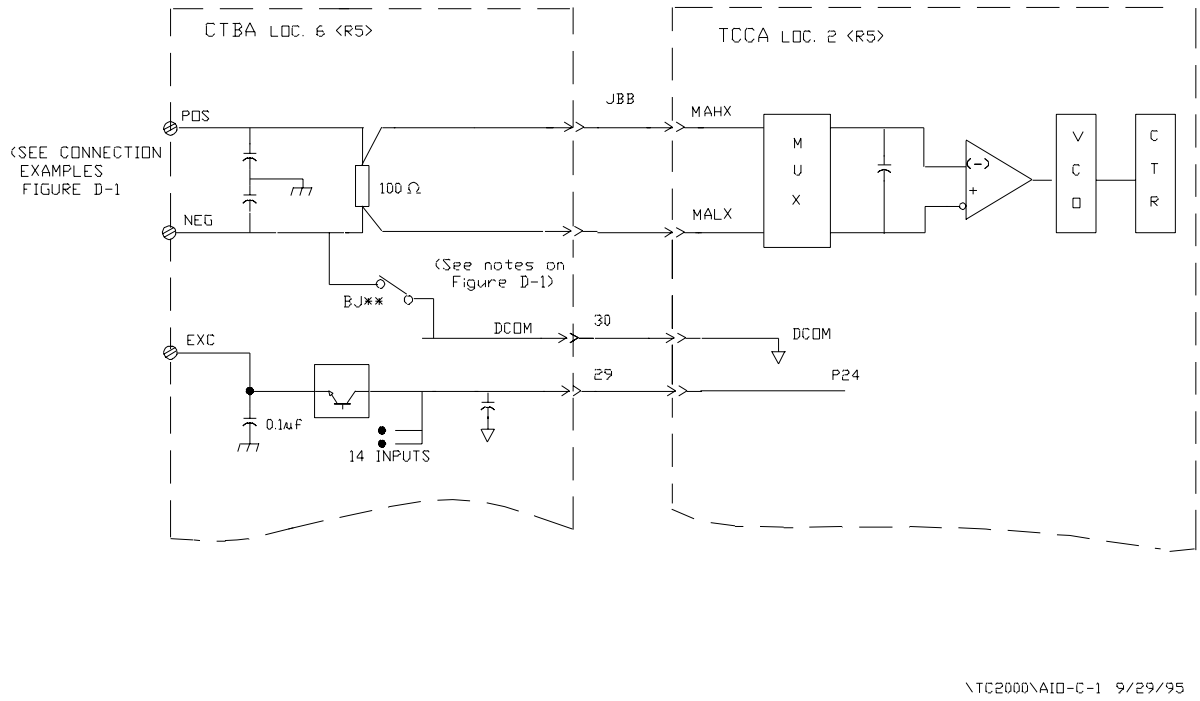


Figure D-27. <R5> Core: 4–20 mA Inputs on CTBA

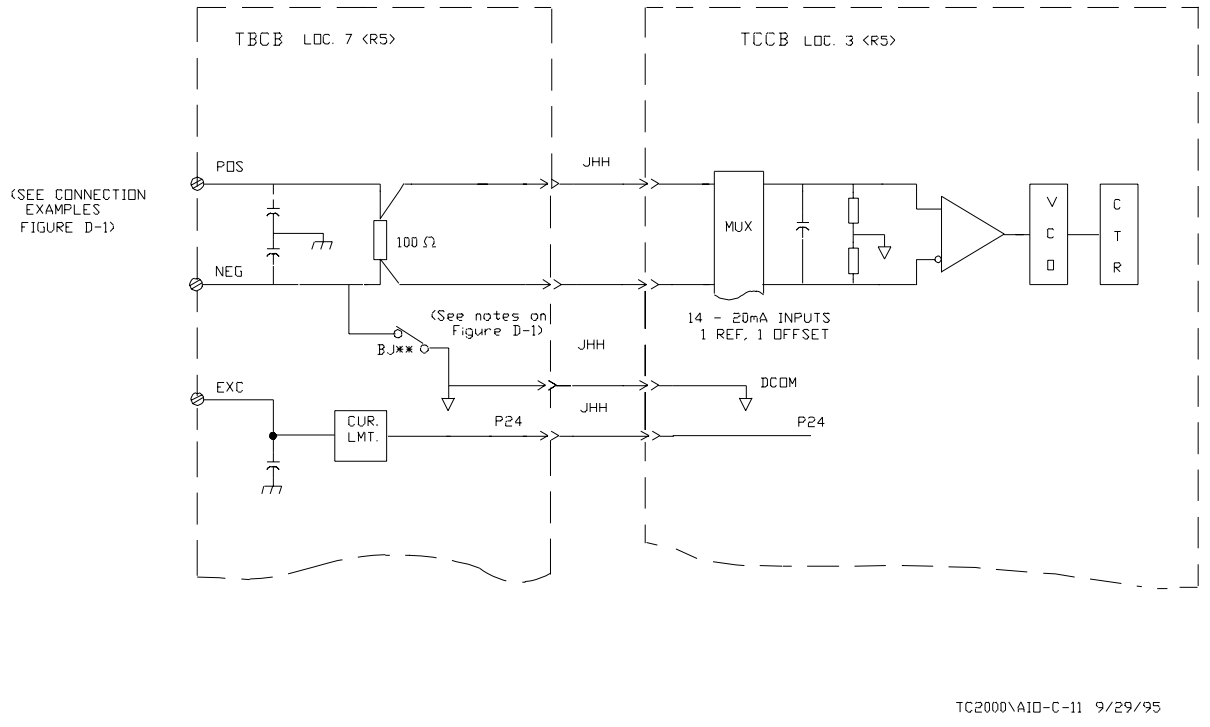


Figure D-28. <R5> Core: 4 – 20 mA Inputs on TBCB

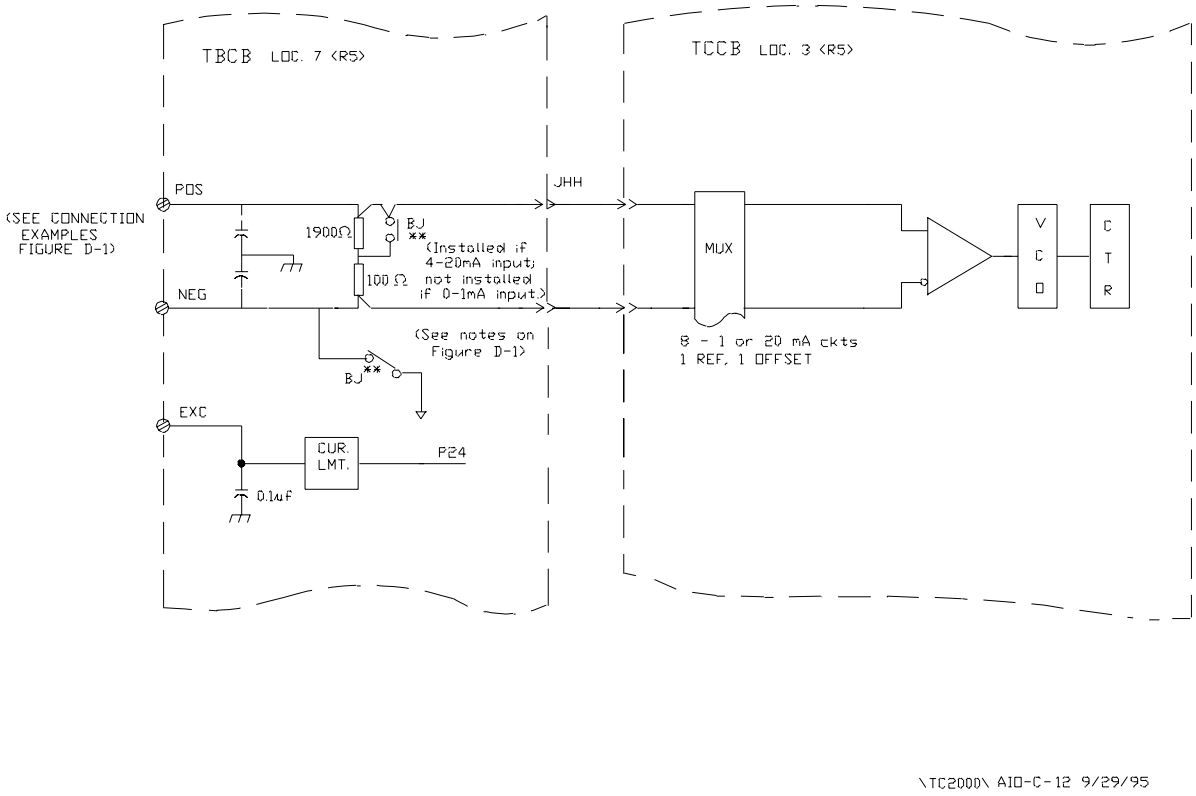
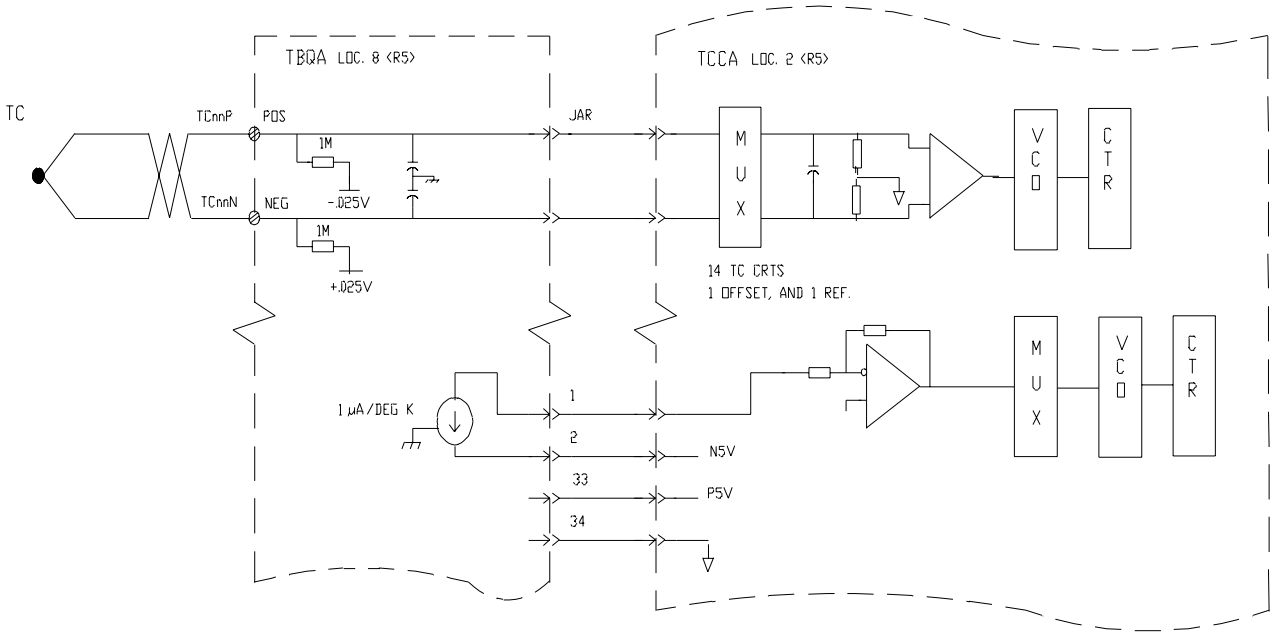


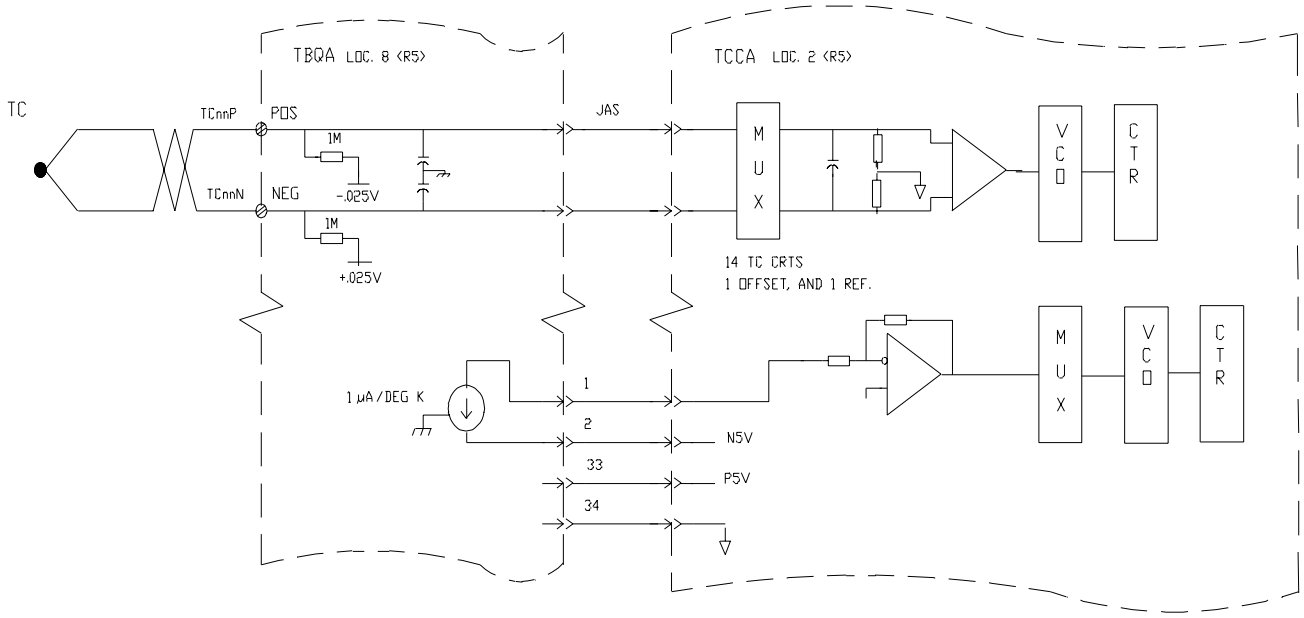
Figure D-29. <R5> Core: 0 – 1 and 4 – 20 mA Inputs on TBCB



DEVICE TB DESIGNATION	TERMINATION, TBQA		JAR PIN
	POS	NEG	
TC01	1	2	3,4
TC02	3	4	5,6
TC03	5	6	7,8
TC04	7	8	9,10
TC05	9	10	11,12
TC06	11	12	13,14
TC07	13	14	15,16
TC08	15	16	17,18
TC09	17	18	19,20
TC10	19	20	21,22
TC11	21	22	23,24
TC12	23	24	25,26
TC13	25	26	27,28
TC14	27	28	29,30
TC15	29	30	31,32

\TC2000\AIO-C-8 10/6/95

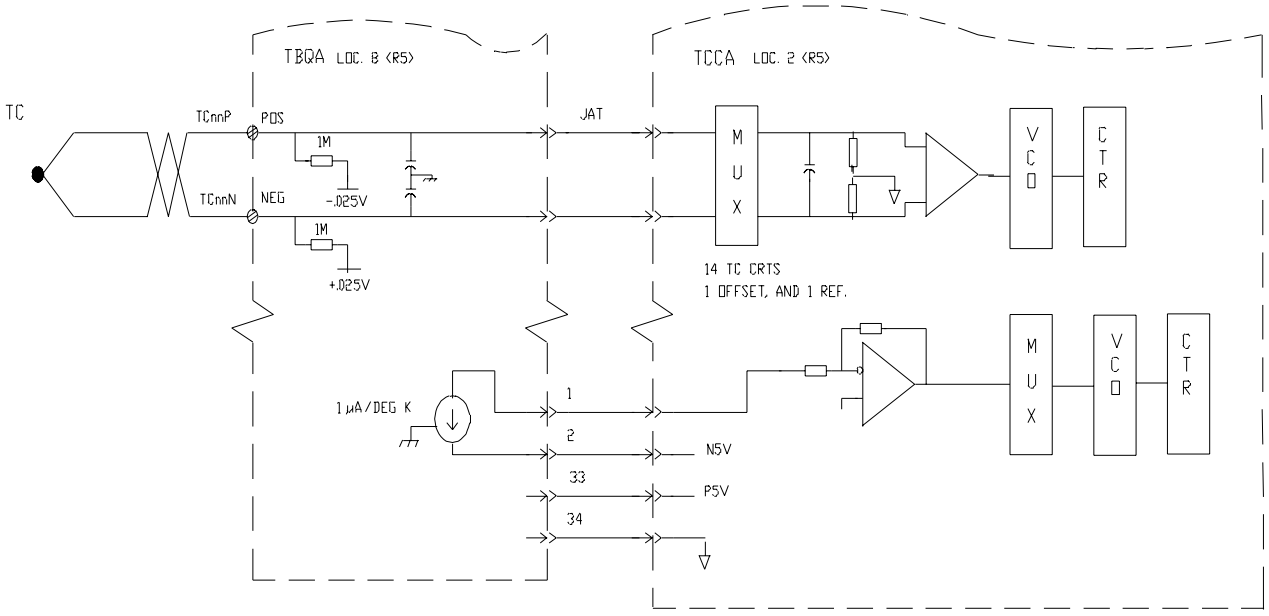
Figure D-30. <R5> Core: Thermocouple Inputs on TBQA/TCCA



\TC2000\AIO-C-9 10/6/95

DEVICE TB DESIGNATION	TERMINATION, TBQA		JAS PIN
	POS	NEG	
TC16	31	32	3,4
TC17	33	34	5,6
TC18	35	36	7,8
TC19	37	38	9,10
TC20	39	40	11,12
TC21	41	42	13,14
TC22	43	44	15,16
TC23	45	46	17,18
TC24	47	48	19,20
TC25	49	50	21,22
TC26	51	52	23,24
TC27	53	54	25,26
TC28	55	56	27,28
TC29	57	58	29,30
TC30	59	60	31,32

Figure D-31. <R5> Core: Thermocouple Inputs on TBQA/TCCA



DEVICE TB DESIGNAITON	TERMINATION TBQA POS	TERMINATION TBQA NEG	JAT PIN
TC31	61	62	3,4
TC32	63	64	5,6
TC33	65	66	7,8
TC34	67	68	9,10
TC35	69	70	11,12
TC36	71	72	13,14
TC37	73	74	15,16
TC38	75	76	17,18
TC39	77	78	19,20
TC40	79	80	21,22
TC41	81	82	23,24
TC42	83	84	25,26

\TC2000\AIO-C-10 10/6/95

Figure D-32. <R5> Core: Thermocouple Inputs on TBQA/TCCA

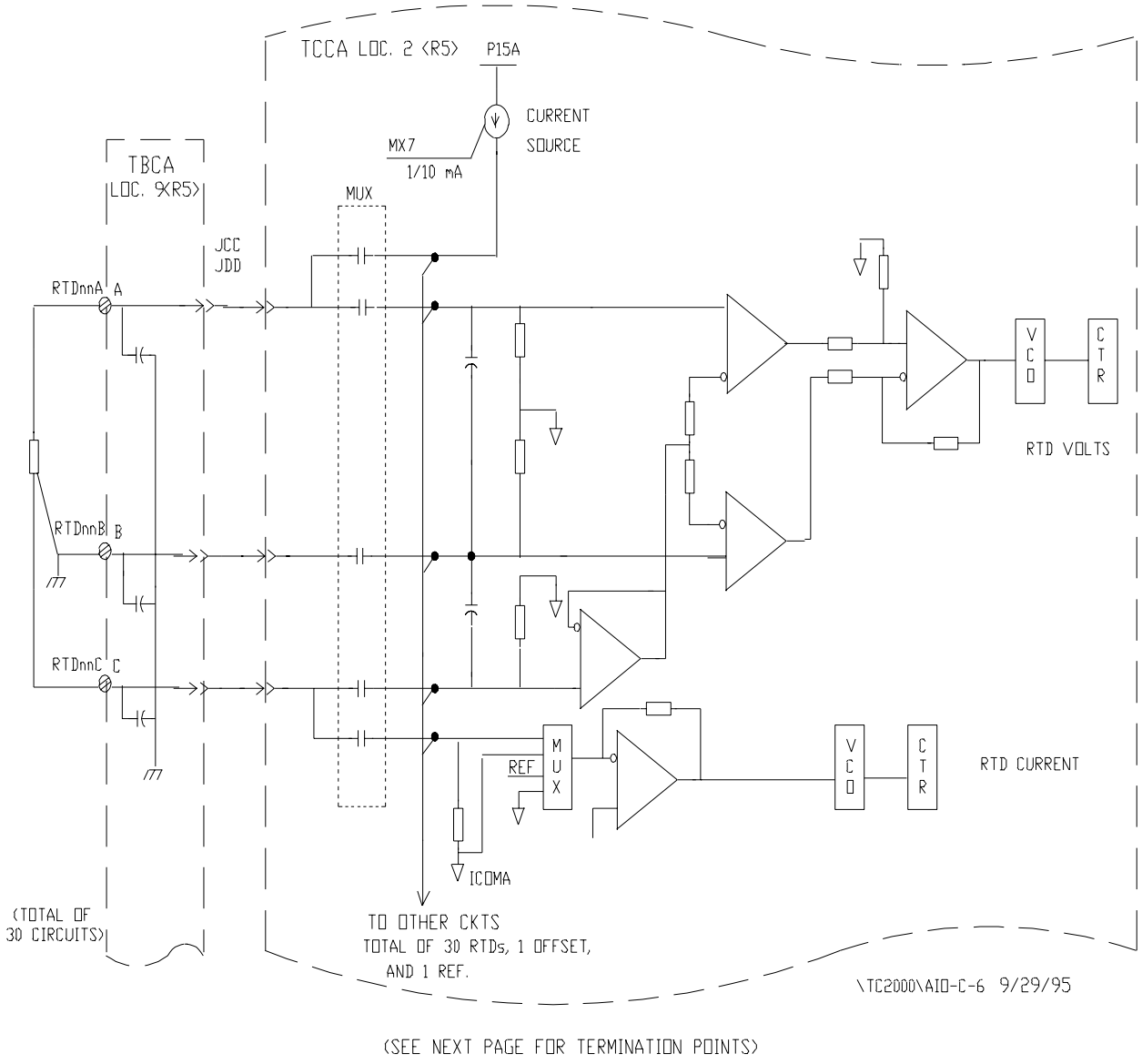
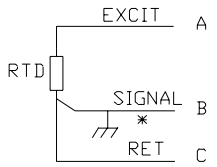


Figure D-33. <R5> Core: RTD Inputs on TBCA/TCCA

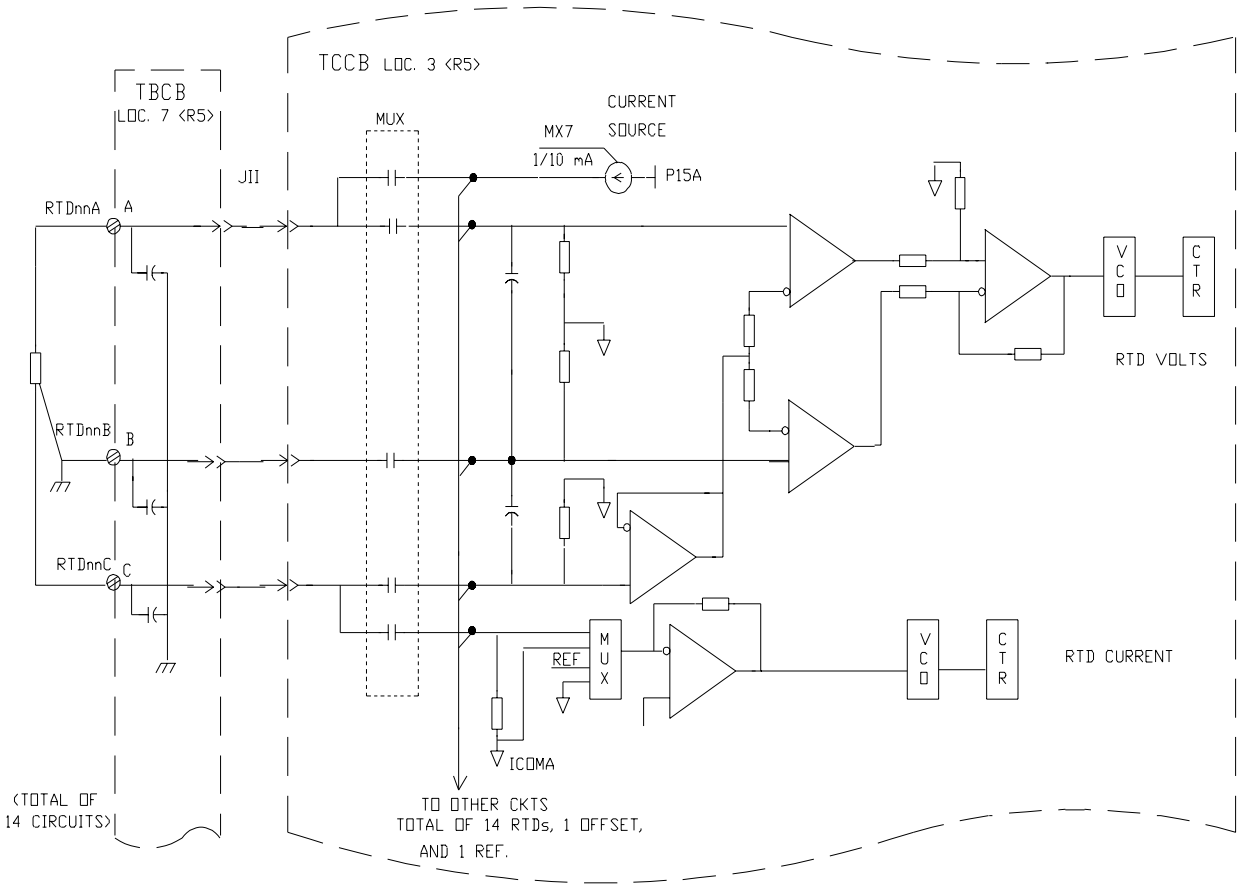


DEVICE TB DESIGNATION	TERMINATION TBCA A	B	C
RTD01	1	2	3
RTD02	4	5	6
RTD03	7	8	9
RTD04	10	11	12
RTD05	13	14	15
RTD06	16	17	18
RTD07	19	20	21
RTD08	22	23	24
RTD09	25	26	27
RTD10	28	29	30
RTD11	31	32	33
RTD12	34	35	36
RTD13	37	38	39
RTD14	40	41	42
RTD15	43	44	45
RTD16	46	47	48
RTD17	49	50	51
RTD18	52	53	54
RTD19	55	56	57
RTD20	58	59	60
RTD21	61	62	63
RTD22	64	65	66
RTD23	67	68	69
RTD24	70	71	72
RTD25	73	74	75
RTD26	76	77	78
RTD27	79	80	81
RTD28	82	83	84
RTD29	85	86	87
RTD30	88	89	90

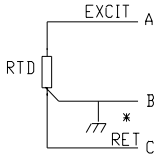
(SEE PREVIOUS PAGE FOR DIAGRAM)

\TC2000\AIO-C-7 6/2/93

Figure D-34. <R5> Core: RTD Inputs on TBCA/TCCA



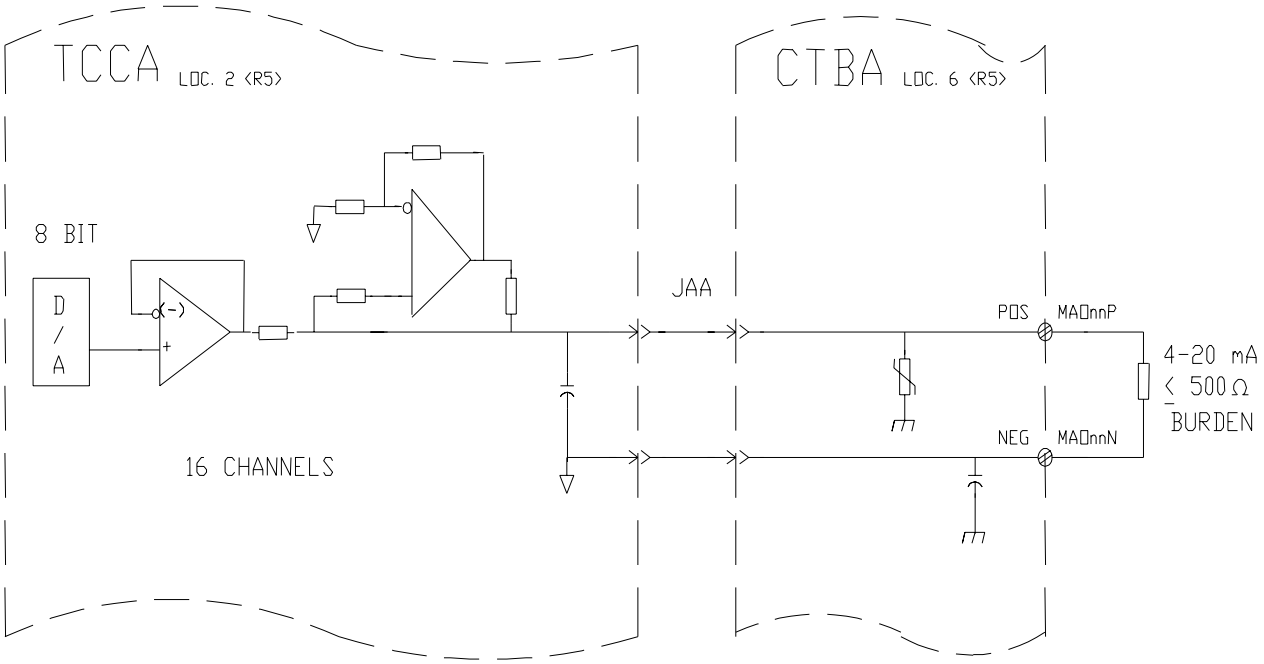
DEVICE TB DESIGNATION	TERMINATION TBCB A	B	C
RTD01	67	68	69
RTD02	70	71	72
RTD03	73	74	75
RTD04	76	77	78
RTD05	79	80	81
RTD06	82	83	84
RTD07	85	86	87
RTD08	88	89	90
RTD09	91	92	93
RTD10	94	95	96
RTD11	97	98	99
RTD12	100	101	102
RTD13	103	104	105
RTD14	106	107	108



\TC2000\AIO-C-13 9/29/95

* GROUNDING IS OPTIONAL

Figure D-35. <R5> Core: RTD Inputs on TBCB/TCCB



DEVICE TB DESIGNATION	SIGNAL TERMINATION	
	POS	NEG
MA□01	1	2
MA□02	3	4
MA□03	5	6
MA□04	7	8
MA□05	9	10
MA□06	11	12
MA□07	13	14
MA□08	15	16
MA□09	17	18
MA□10	19	20
MA□11	21	22
AM□12	23	24
MA□13	25	26
MA□14	27	28
MA□15	29	30
MA□16	31	32

\TC2000\AI□-C-2 9/29/95

Figure D-36. <R5> Core: 4–20 mA Outputs on CTBA

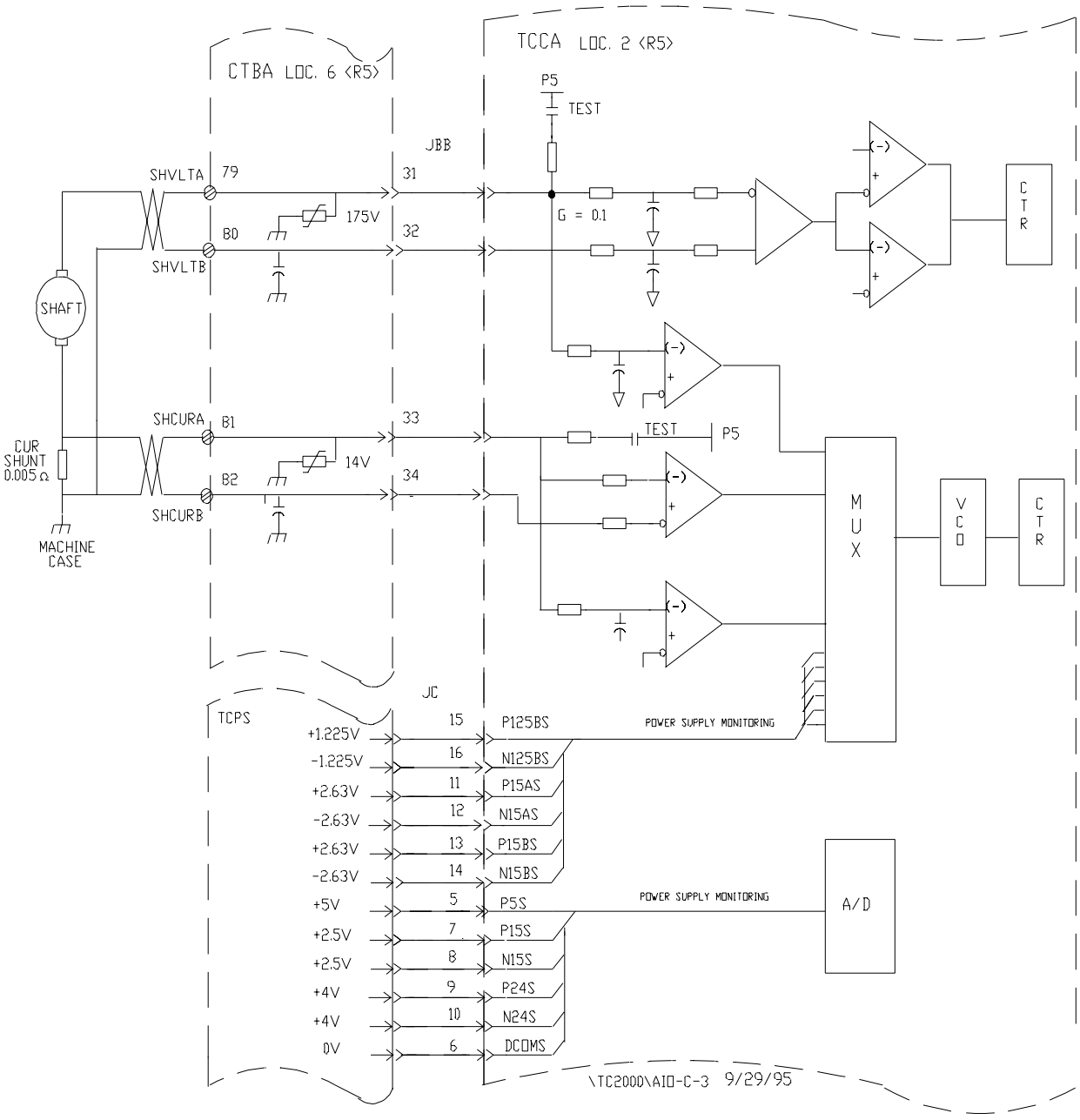


Figure D-37. <R5> Core: Shaft Voltage Monitoring on CTBA

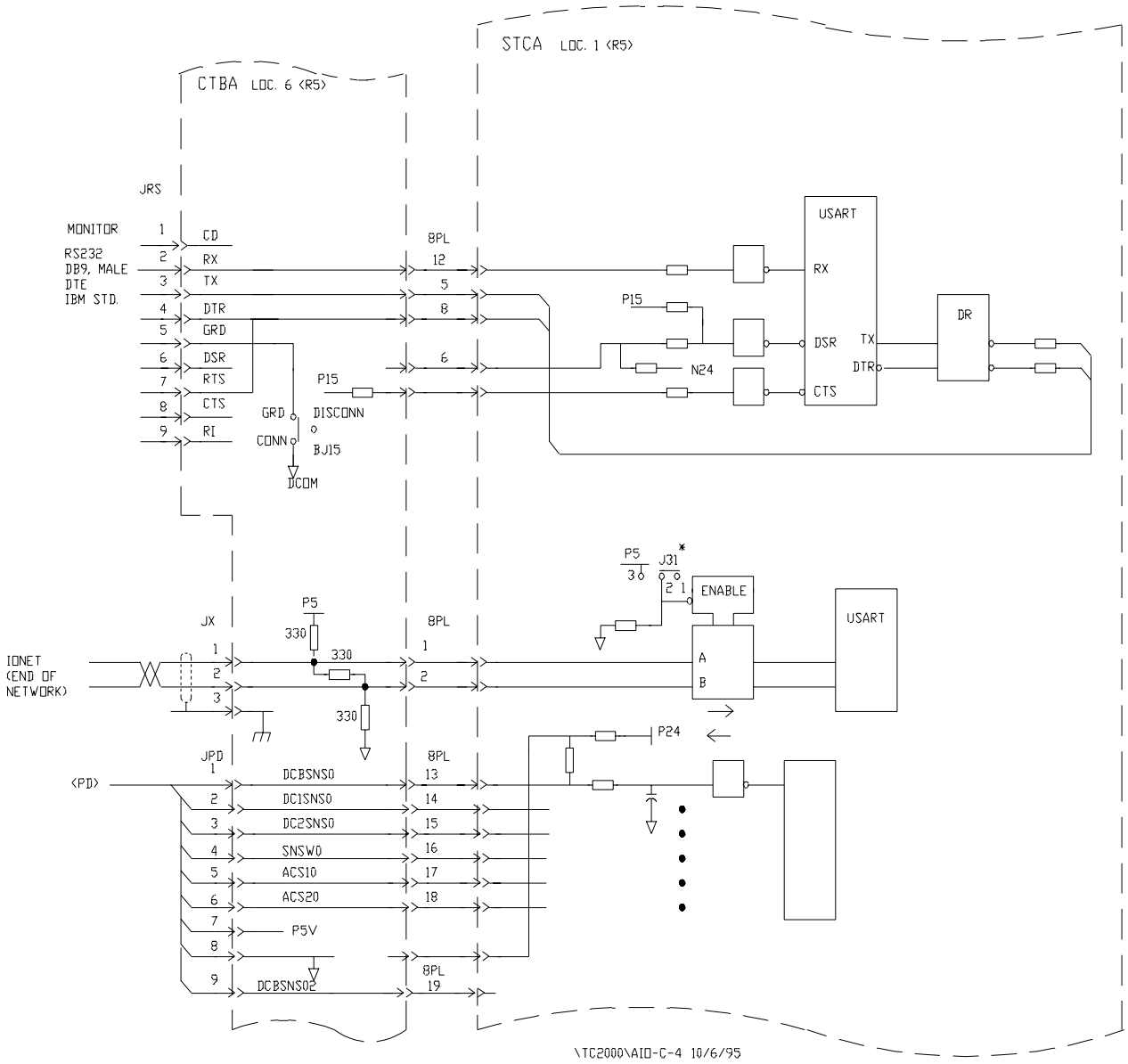


Figure D-38. <R5> Core: TIMN Monitor and IONET Connection on CTBA

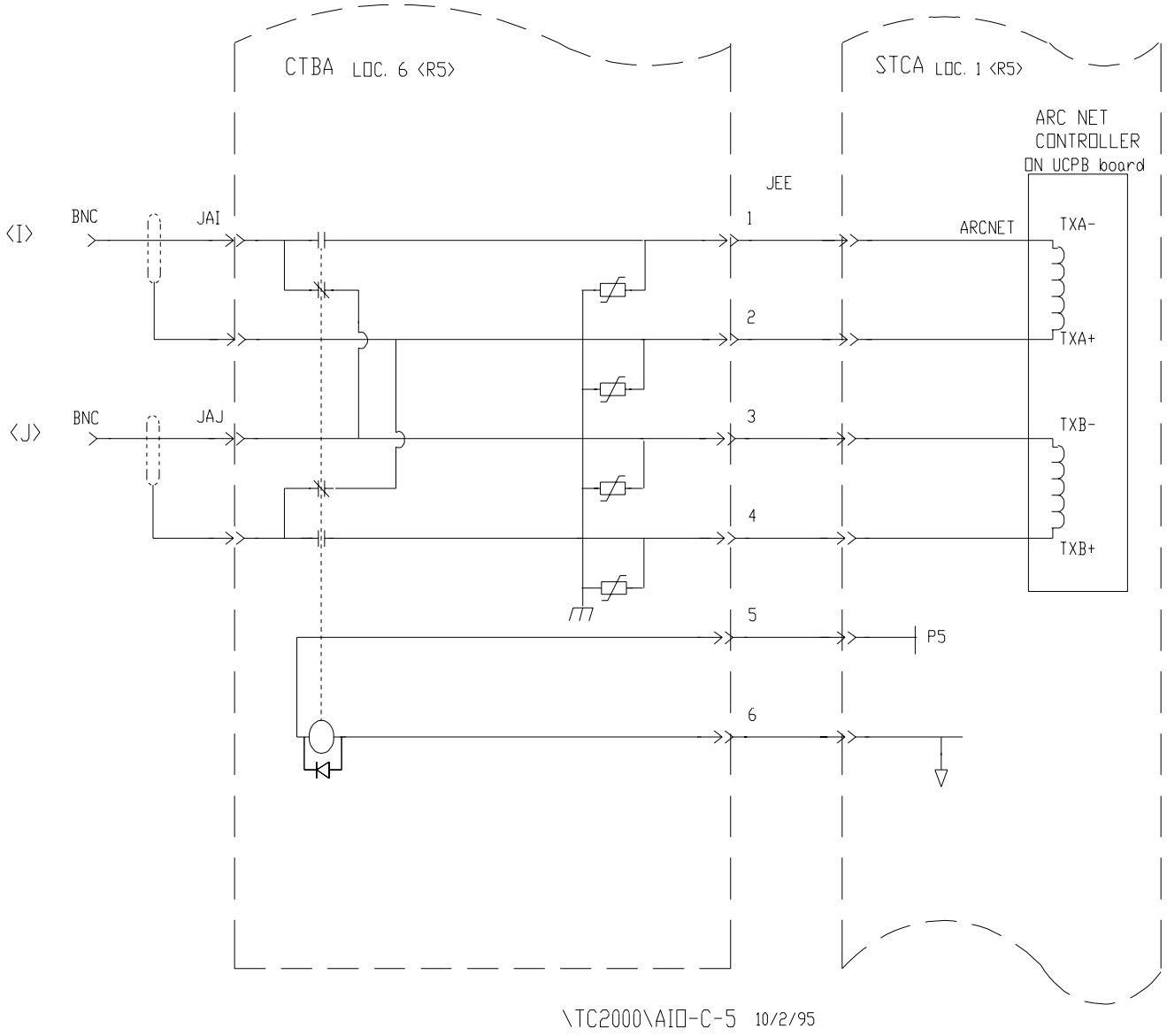


Figure D-39. <R5> Core: COREBUS Connection on CTBA

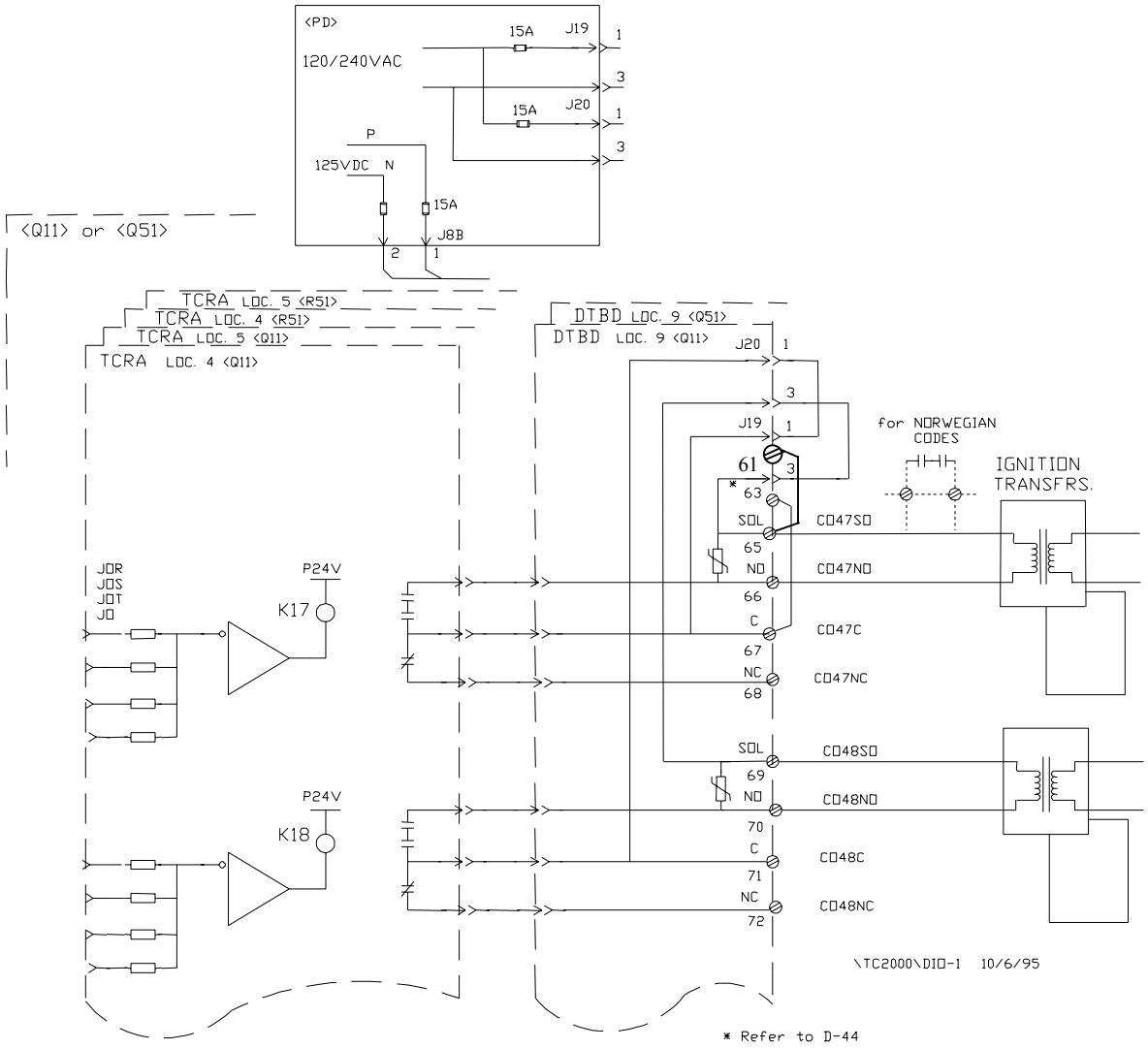
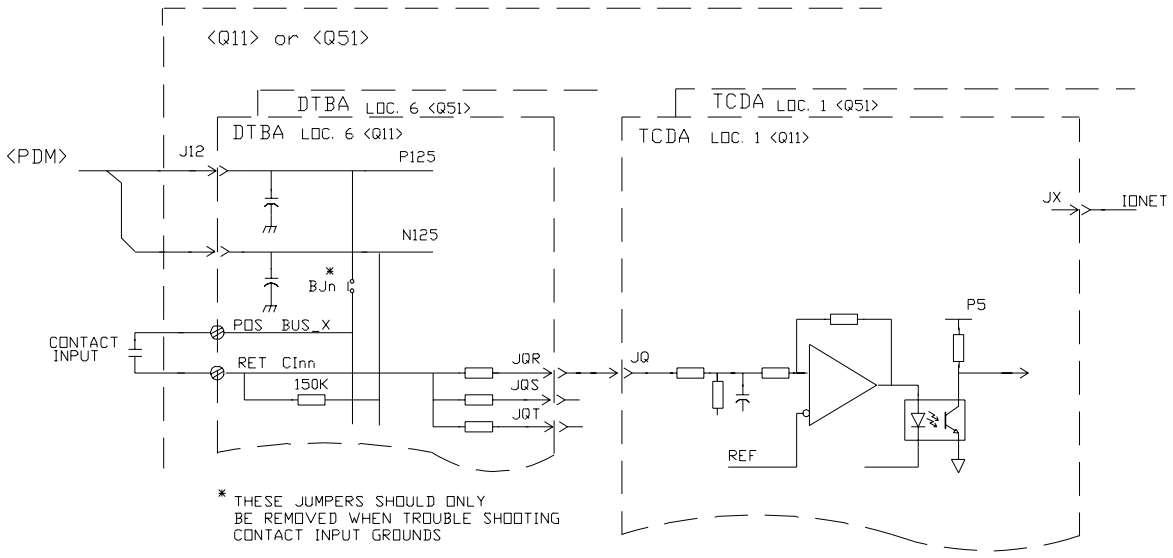


Figure D-40. <Q11> and <Q51> Cores: Solenoid Outputs/Ignition Transformers on DTBD



CONTACT #	DTBA SCREW	
	POS	RET
CI01	2	1
CI02	4	3
CI03	6	5
CI04	8	7
CI05	10	9
CI06	12	11
CI07	14	13
CI08	16	15
CI09	18	17
CI010	20	19
CI011	22	21
CI012	24	23
CI013	26	25
CI014	28	27
CI015	30	29
CI016	32	31
CI017	34	33
CI018	36	35
CI019	38	37
CI020	40	39

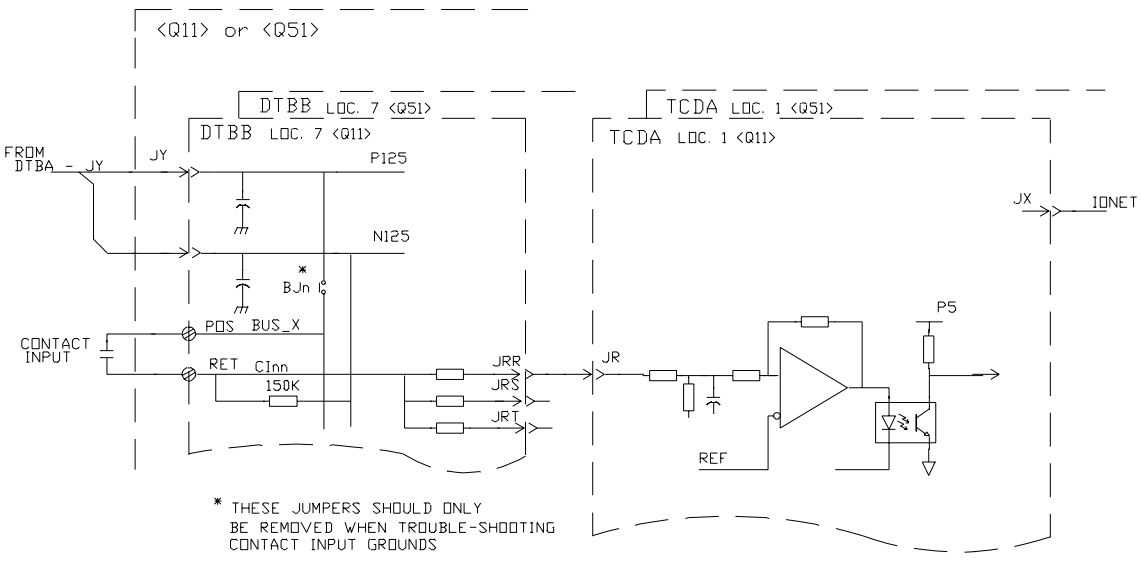
CONTACT #	DTBA SCREW	
	POS	RET
CI021	42	41
CI022	44	43
CI023	46	45
CI024	48	47
CI025	50	49
CI026	52	51
CI027	54	53
CI028	56	55
CI029	58	57
CI030	60	59
CI031	62	61
CI032	64	63
CI033	66	65
CI034	68	67
CI035	70	69
CI036	72	71
CI037	74	73
CI038	76	75
CI039	78	77
CI040	80	79

CONTACT #	DTBA SCREW	
	POS	RET
CI041	82	81
CI042	84	83
CI043	86	85
CI044	88	87
CI045	90	89
CI046	92	91

\TC2000\DIO-2 10/6/95

JUMPER ISOLATION TABLE	
JBn*	INPUTS
BJ1	#1 to #9
BJ2	#10 to #18
BJ3	#19 to #27
BJ4	#28 to #36
BJ5	#37 to #46

Figure D-41. <Q11> and <Q51> Cores: Digital Inputs on DTBA



CONTACT #	DTBB SCREW	
	POS	RET
CI047	2	1
CI048	4	3
CI049	6	5
CI050	8	7
CI051	10	9
CI052	12	11
CI053	14	13
CI054	16	15
CI055	18	17
CI056	20	19
CI057	22	21
CI058	24	23
CI059	26	25
CI060	28	27
CI061	30	29
CI062	32	31
CI063	34	33
CI064	36	35
CI065	38	37
CI066	40	39

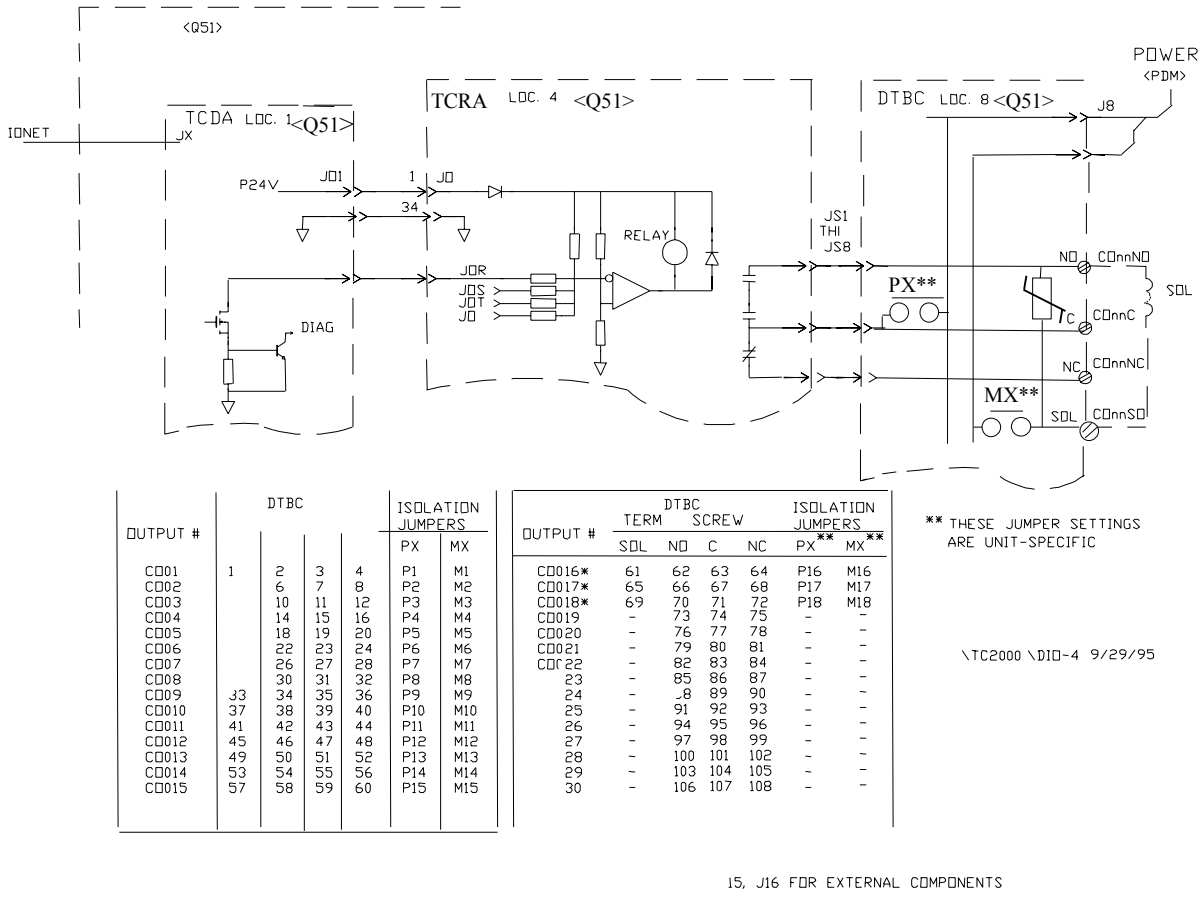
CONTACT #	DTBB SCREW	
	POS	RET
CI067	42	41
CI068	44	43
CI069	46	45
CI070	48	47
CI071	50	49
CI072	52	51
CI073	54	53
CI074	56	55
CI075	58	57
CI076	60	59
CI077	62	61
CI078	64	63
CI079	66	65
CI080	68	67
CI081	70	69
CI082	72	71
CI083	74	73
CI084	76	75
CI085	78	77
CI086	80	79

CONTACT #	DTBB SCREW	
	POS	RET
CI087	82	81
CI088	84	83
CI089	86	85
CI090	88	87
CI091	90	89
CI092	92	91
CI093	94	93
CI094	96	95
CI095	98	97
CI096	100	99

\TC2000\DIO-3 9/29/95

JUMPER ISOLATION TABLE	
JBn *	INPUTS
BJ1	#47 to #56
BJ2	#57 to #66
BJ3	#67 to #76
BJ4	#77 to #86
BJ5	#87 to #96

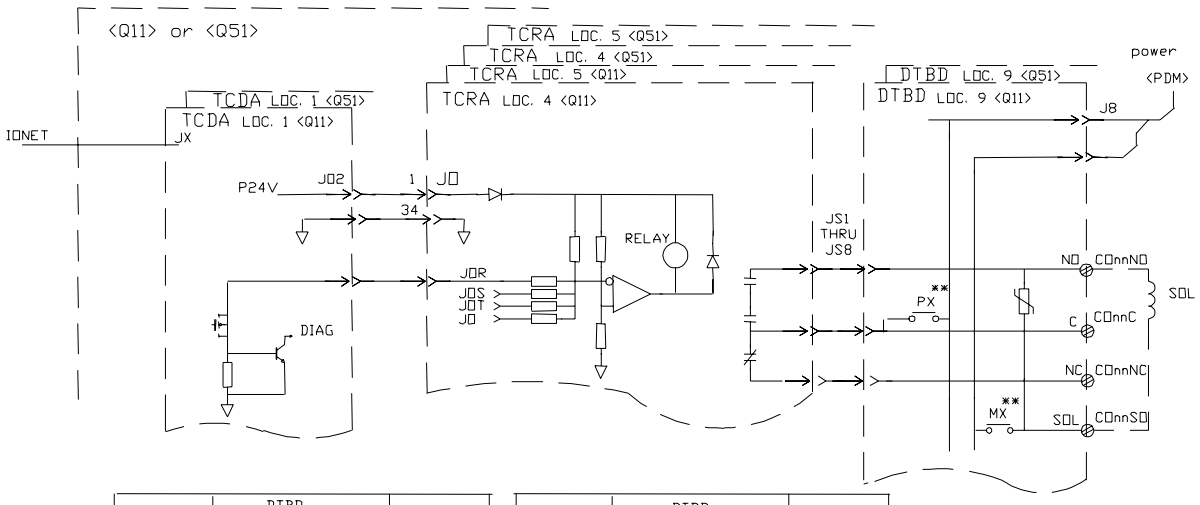
Figure D-42. <Q11> and <Q51> Cores: Digital Inputs on DTBB



OUTPUT #	DTBC				ISOLATION JUMPERS	
					PX	MX
C001	1	2	3	4	P1	M1
C002		6	7	8	P2	M2
C003		10	11	12	P3	M3
C004		14	15	16	P4	M4
C005		18	19	20	P5	M5
C006		22	23	24	P6	M6
C007		26	27	28	P7	M7
C008		30	31	32	P8	M8
C009	33	34	35	36	P9	M9
C010	37	38	39	40	P10	M10
C011	41	42	43	44	P11	M11
C012	45	46	47	48	P12	M12
C013	49	50	51	52	P13	M13
C014	53	54	55	56	P14	M14
C015	57	58	59	60	P15	M15

OUTPUT #	DTBC TERM SCREW				ISOLATION JUMPERS	
	SOL	NO	C	NC	PX**	MX**
C0016*	61	62	63	64	P16	M16
C0017*	65	66	67	68	P17	M17
C0018*	69	70	71	72	P18	M18
C0019	-	73	74	75	-	-
C0020	-	76	77	78	-	-
C0021	-	79	80	81	-	-
C0022	-	82	83	84	-	-
23	-	85	86	87	-	-
24	-	88	89	90	-	-
25	-	91	92	93	-	-
26	-	94	95	96	-	-
27	-	97	98	99	-	-
28	-	100	101	102	-	-
29	-	103	104	105	-	-
30	-	106	107	108	-	-

Figure D-43. <Q51> Core: Relay Outputs on DTBC



OUTPUT #	DTBD TERM SCREW				ISOLATION JUMPERS	
	SOL	NO	C	NC	PX	MX
CO031	1	2	3	4	P1	M1
CO032	5	6	7	8	P2	M2
CO033	9	10	11	12	P3	M3
CO034	13	14	15	16	P4	M4
CO035	17	18	19	20	P5	M5
CO036	21	22	23	24	P6	M6
CO037	25	26	27	28	P7	M7
CO038	29	30	31	32	P8	M8
CO039	33	34	35	36	P9	M9
CO040	37	38	39	40	P10	M10
CO041	41	42	43	44	P11	M11
CO042	45	46	47	48	P12	M12
CO043	49	50	51	52	P13	M13
CO044	53	54	55	56	P14	M14
CO045	57	58	59	60	P15	M15

OUTPUT #	DTBD TERM SCREW				ISOLATION JUMPERS	
	SOL	NO	C	NC	PX**	MX**
CO046	61	62	63	64	P16	M16
CO047 *	65	66	67	68	P16	M16
CO048 *	69	70	71	72	P16	M16
CO049	-	73	74	75	-	-
CO050	-	76	77	78	-	-
CO051	-	79	80	81	-	-
CO052	-	82	83	84	-	-
CO053	-	85	86	87	-	-
CO054	-	88	89	90	-	-
CO055	-	91	92	93	-	-
CO056	-	94	95	96	-	-
CO057	-	97	98	99	-	-
CO058	-	100	101	102	-	-
CO059	-	103	104	105	-	-
CO060	-	106	107	108	-	-

* THESE ARE SPECIAL CIRCUITS -- THEY ARE POWERED WITH VOLTAGE FROM CO046 (REFERENCE D-40)

Figure D-44. <Q11> and <Q51> Cores: Relay Outputs on DTBD

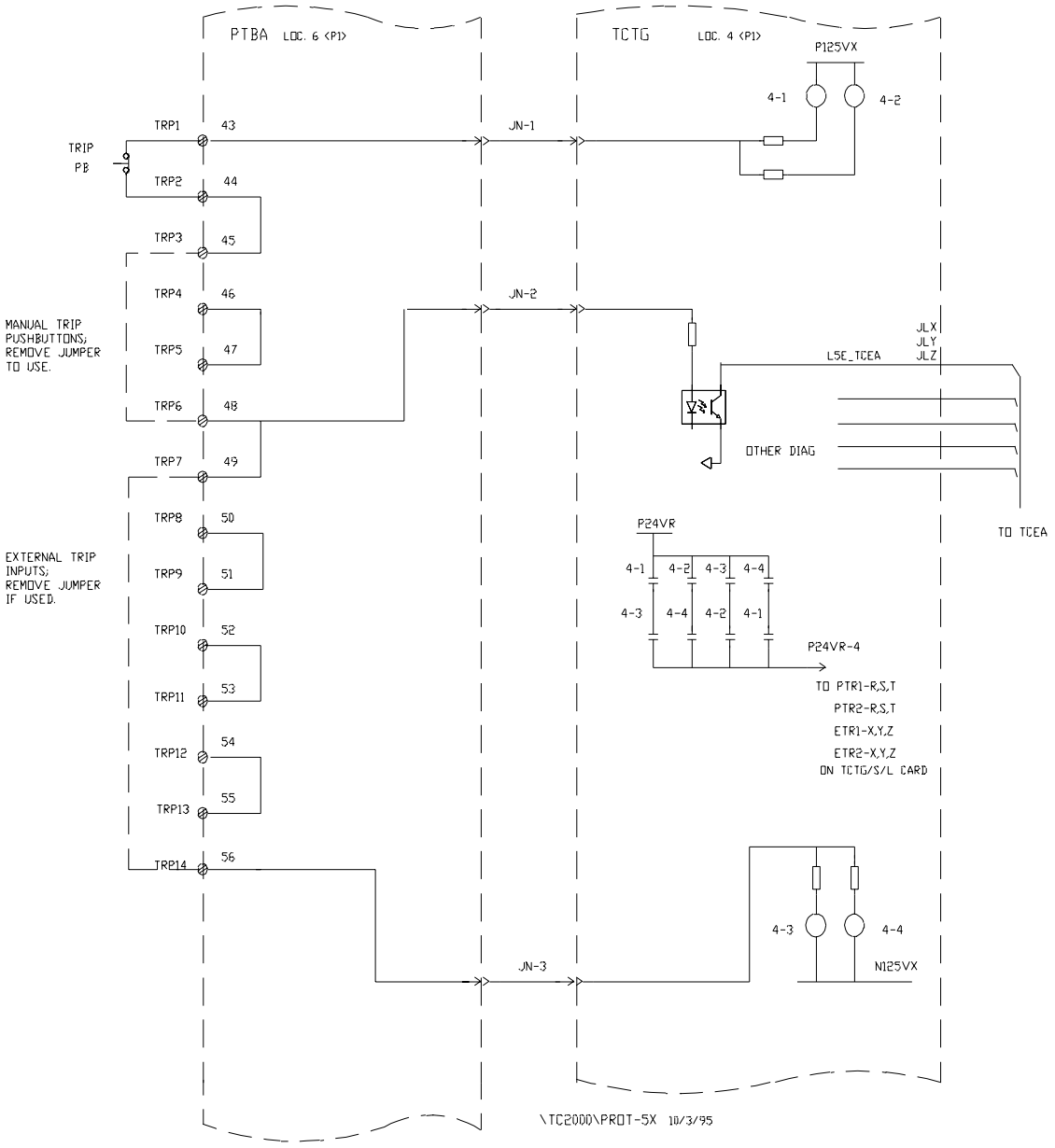


Figure D-45. <P1> Core: Emergency Trip Pushbutton Connections on PTBA

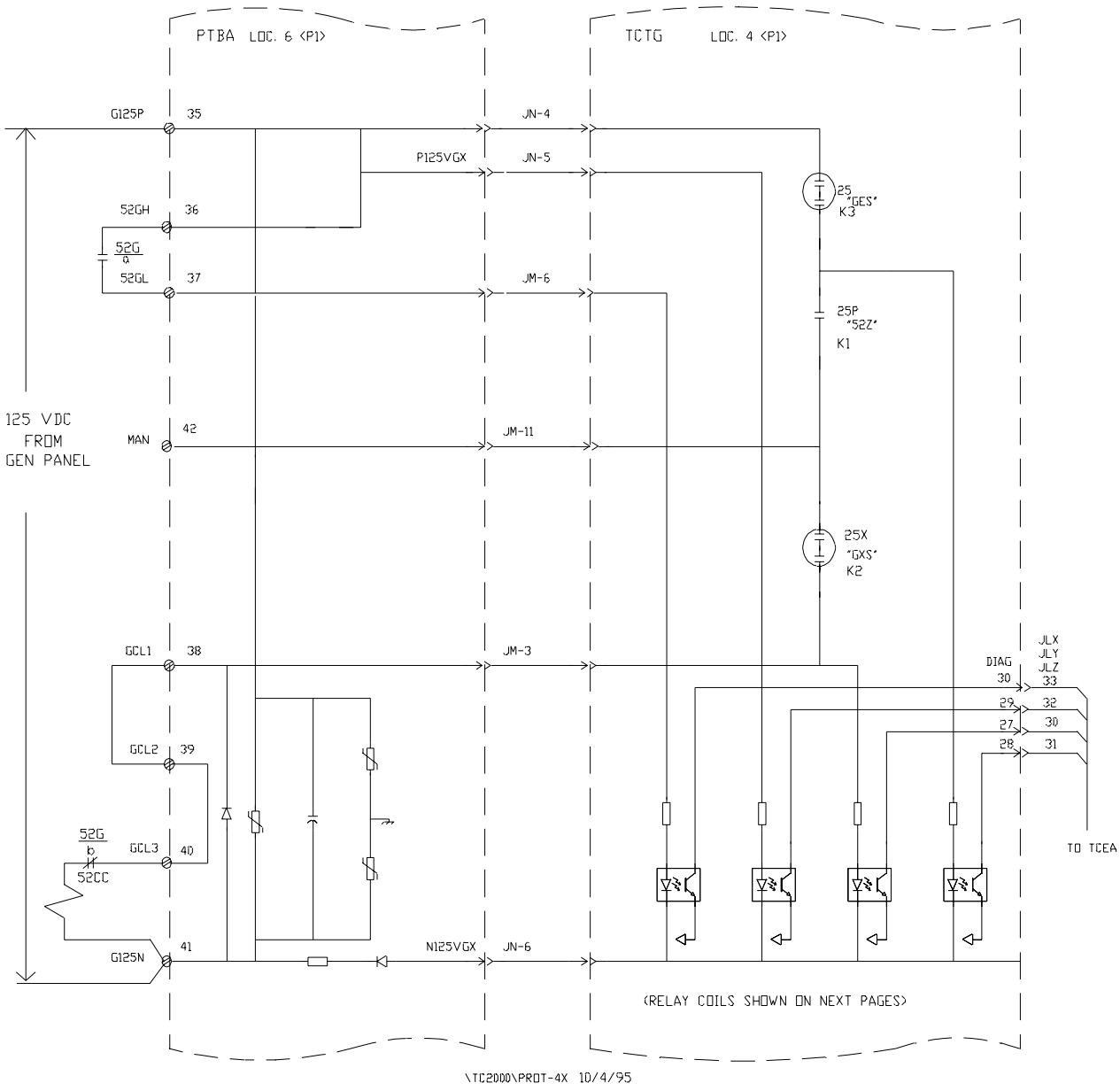
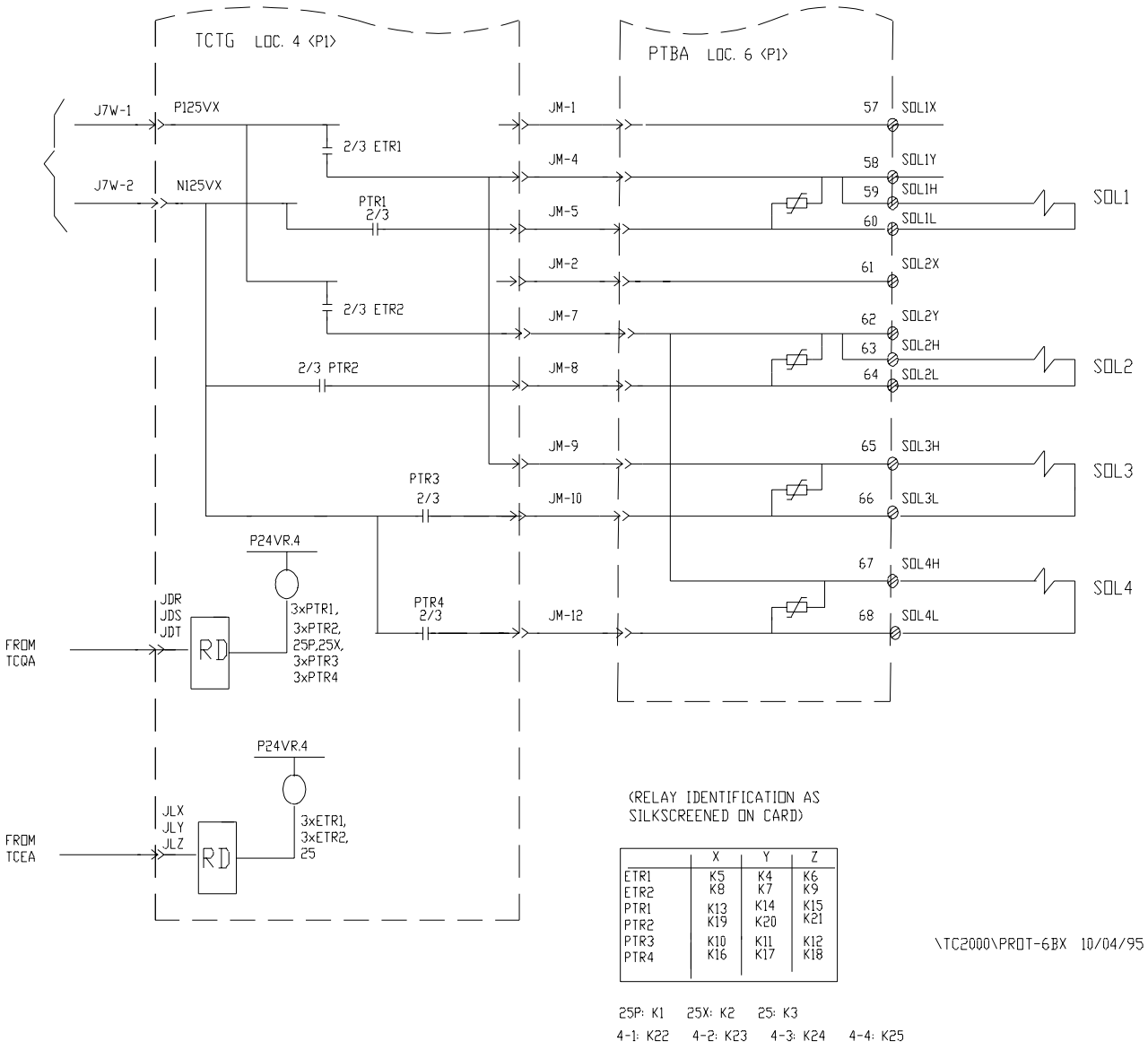


Figure D-46. <P1> Core: Circuit Breaker (52G) Close Circuit



	X	Y	Z
ETR1	K5	K4	K6
ETR2	K8	K7	K9
PTR1	K13	K14	K15
PTR2	K19	K20	K21
PTR3	K10	K11	K12
PTR4	K16	K17	K18

Figure D-47. <P1> Core: Emergency Trip Circuit

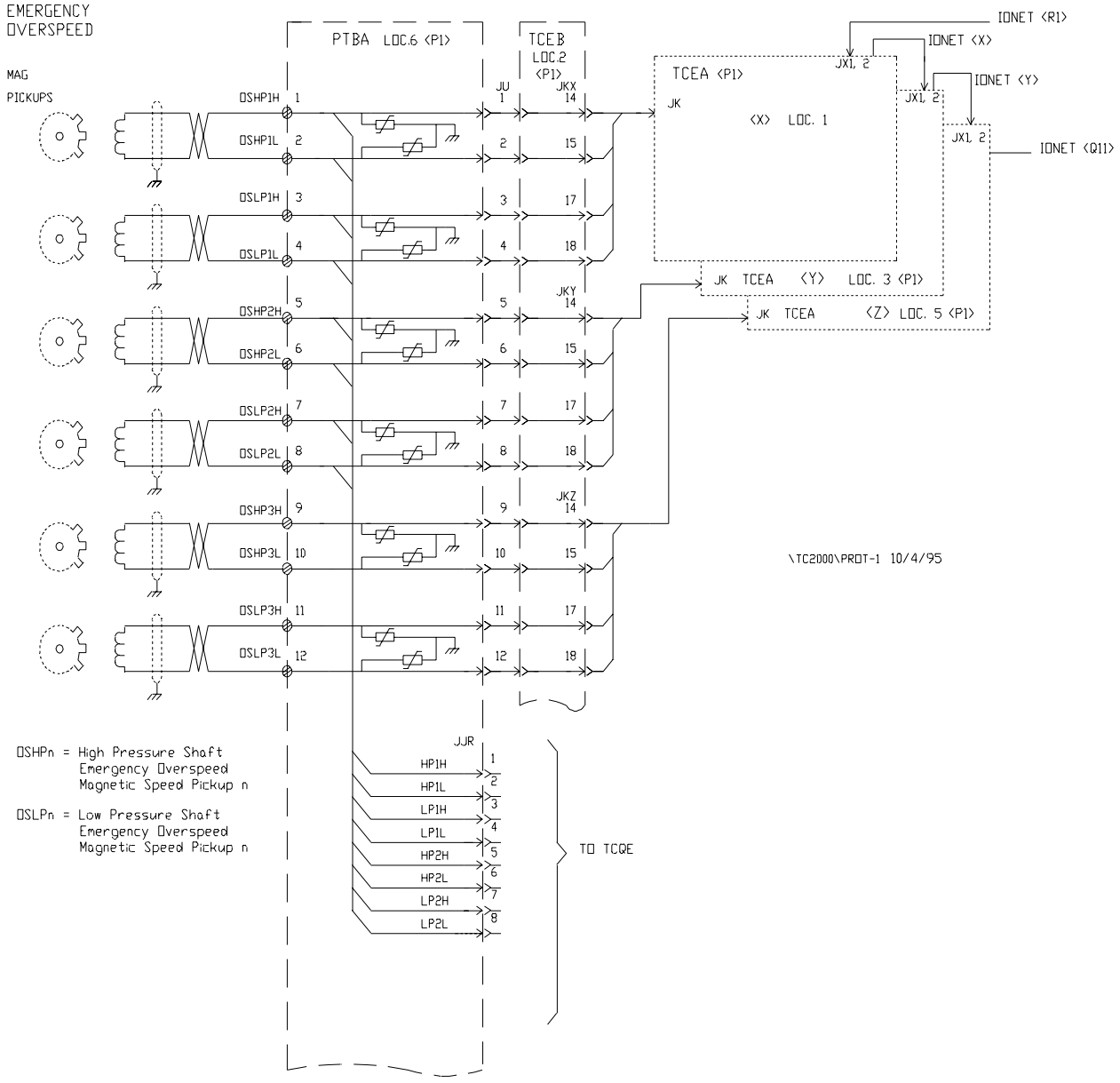
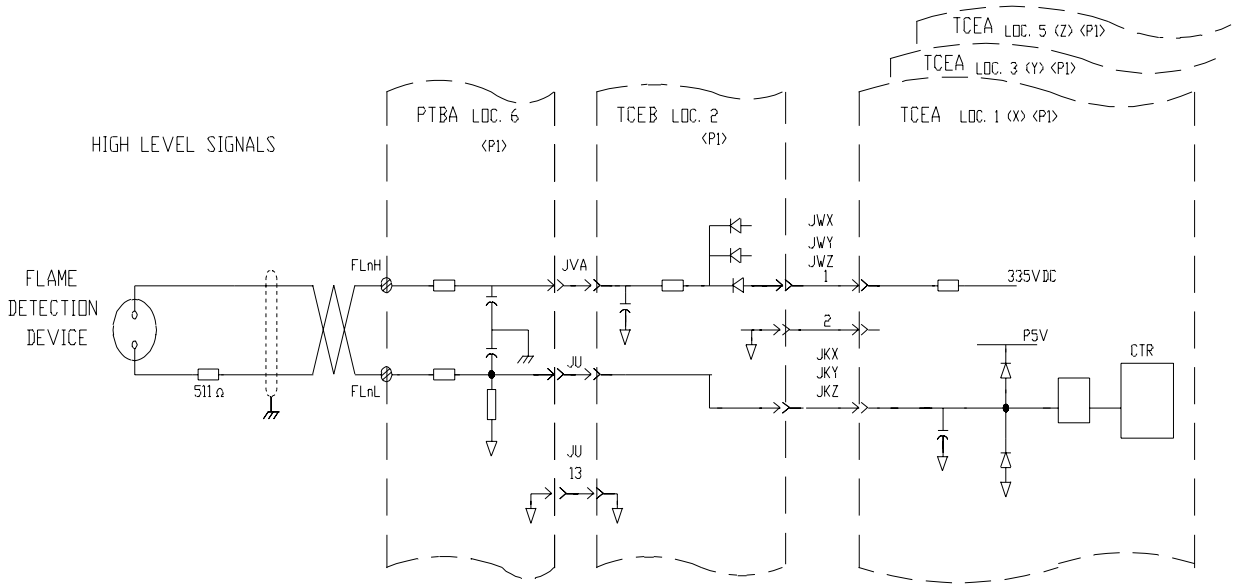


Figure D-48. <P1> Core: Overspeed Magnetic Pickups on PTBA



\TC2000\PROT-2 10/4/95

DEVICE TB DESIGNATION	TERMINATION SCREW	TCEB PIN	TCEA PIN	<I> SIGNAL NAMES: FLAME INTENSITY HZ	THRESHOLD TCE_CONFIG_L28_HI/LO: HIGH	THRESHOLD TCE_CONFIG_L28_HI/LO: LOW	FLAME LOGIC
FL1H	13	JVA-1	-				
FL1L	14	JU-19	JK-1	FD_INTENS_1	_HI[0]	_LO[0]	L28FDA
FL2H	15	JVA-2	-				
FL2L	16	JU-20	JK-2	FD_INTENS_2	_HI[1]	_LO[1]	L28FDB
FL3H	17	JVA-3	-				
FL3L	18	JU-21	JK-3	FD_INTENS_3	_HI[2]	_LO[2]	L28FDC
FL4H	19	JVA-4	-				
FL4L	20	JU-22	JK-4	FD_INTENS_4	_HI[3]	_LO[3]	L28FDD
FL5H	21	JVA-5	-				
FL5L	22	JU-23	JK-5	FD_INTENS_5	_HI[4]	_LO[4]	L28FDE
FL6H	23	JVA-6	-				
FL6L	24	JU-24	JK-6	FD_INTENS_6	_HI[5]	_LO[5]	L28FDF
FL7H	25	JVA-7	-				
FL7L	26	JU-25	JK-7	FD_INTENS_7	_HI[6]	_LO[6]	L28FDG
FL8H	27	JVA-8	-				
FL8L	28	JU-26	JK-8	FD_INTENS_8	_HI[7]	_LO[7]	L28FDH

Figure D-49. <P1> Core: Flame Intensity Inputs on PTBA

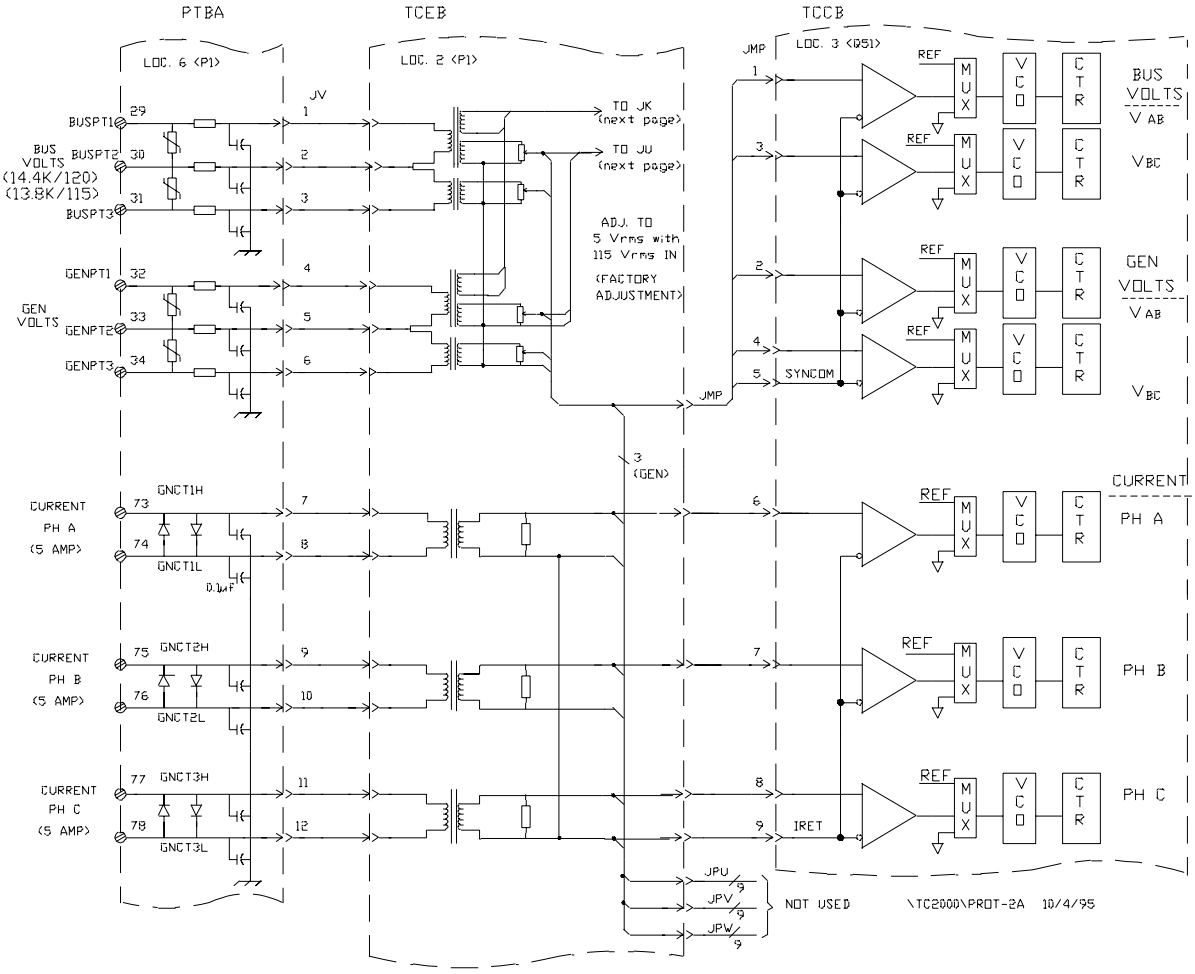


Figure D-50. <P1> Core: Bus Generator PT and CT Inputs on PTBA

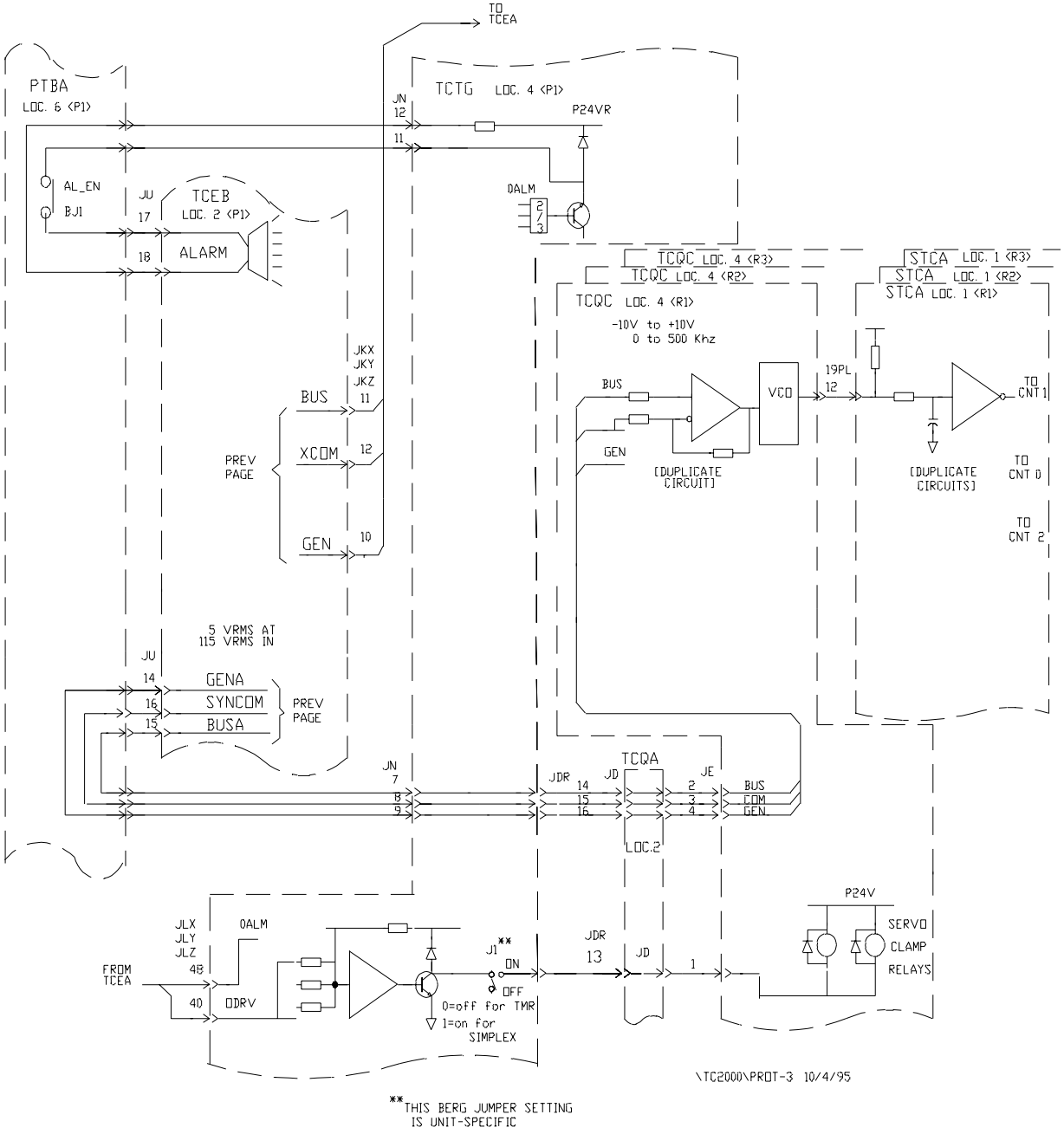


Figure D-51. <P1> Core: Alarm Horn Circuit and Bus Generator Continued

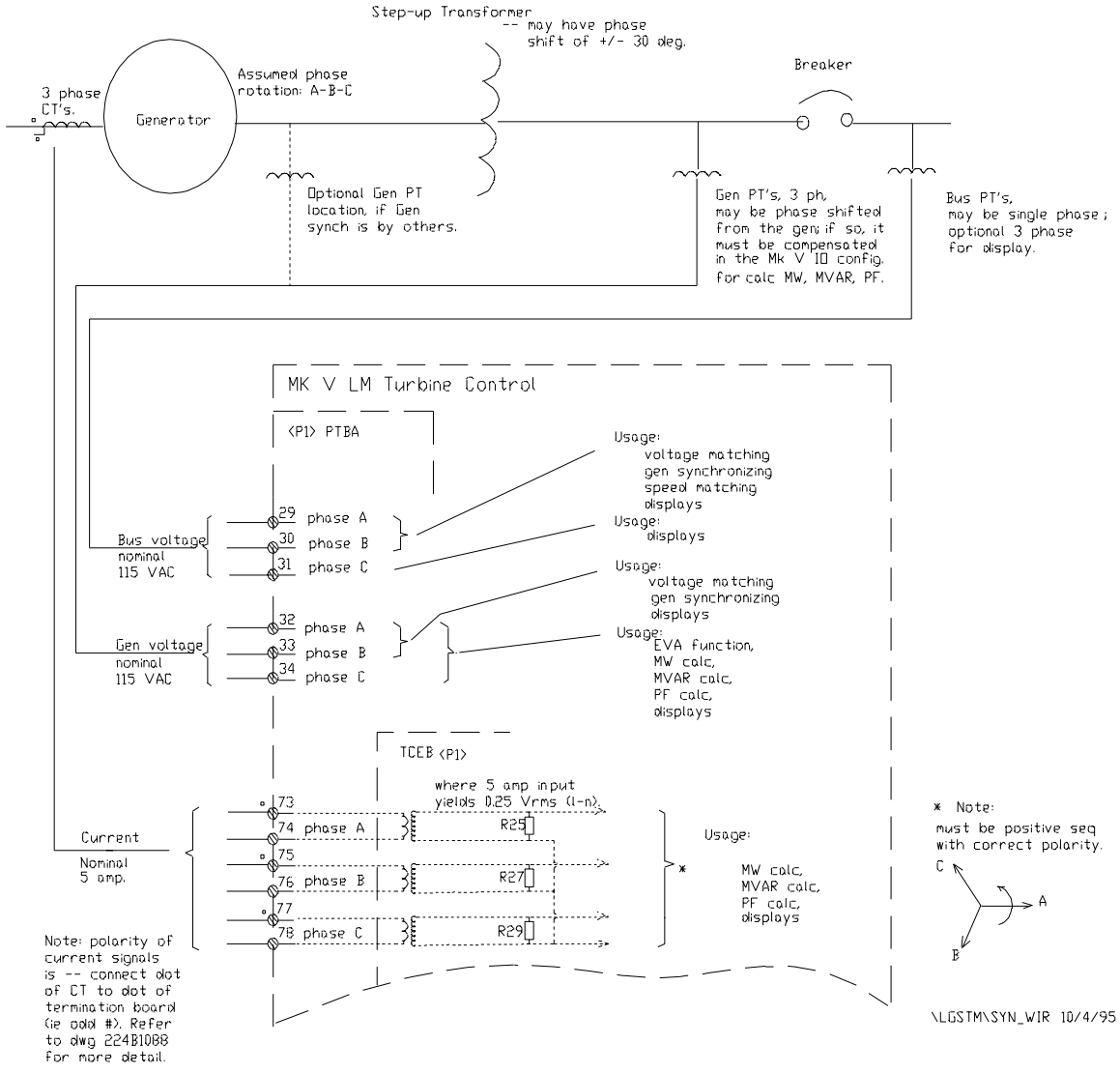


Figure D-52. <P1> Core: Generator Voltage and Current Signal Interface

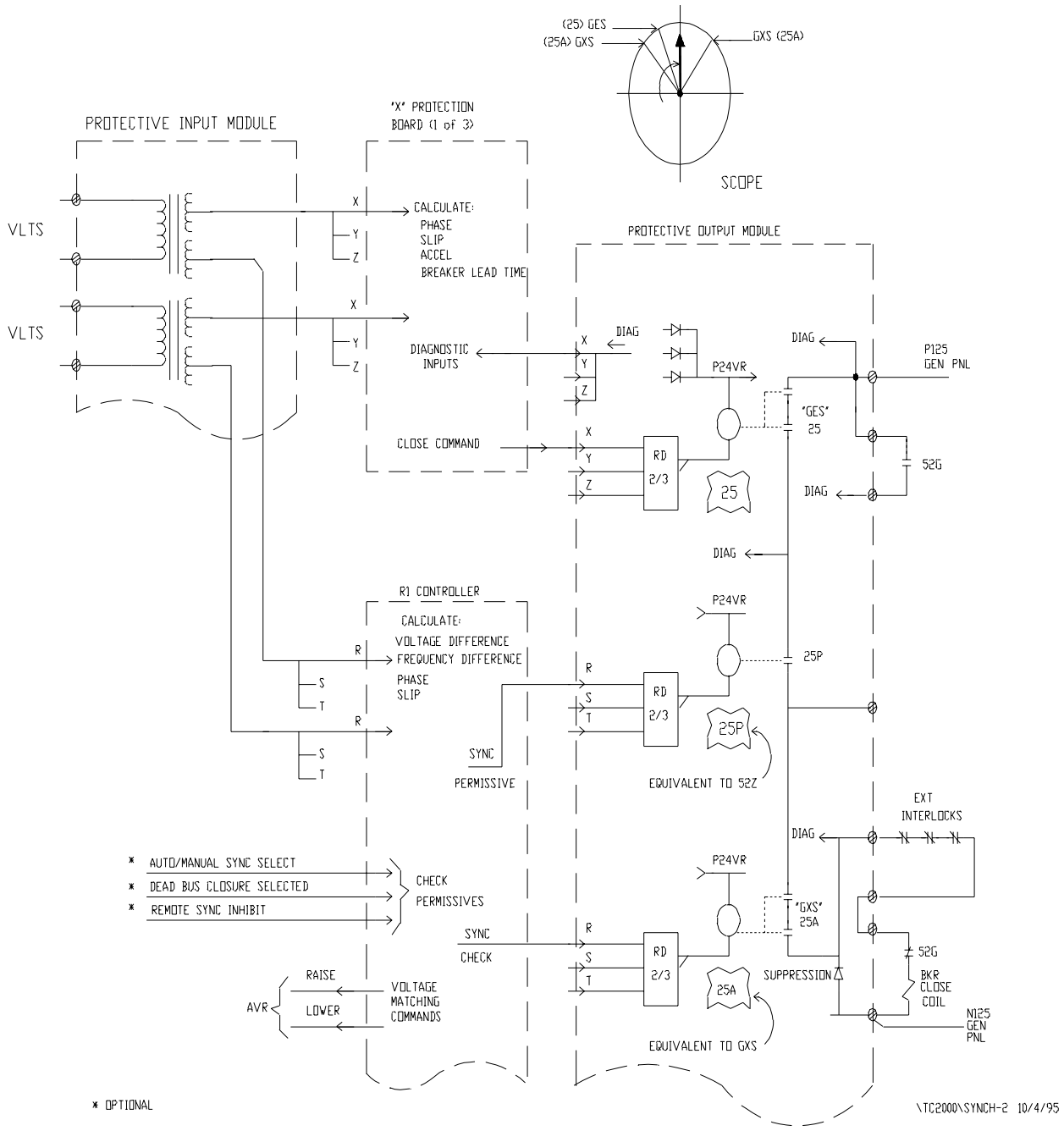


Figure D-53. Mark V LM Synchronize

Appendix E Fuse Ratings

Introduction

This appendix contains fuse ratings and vendor catalog numbers for the fuses on the TCPD, TCPS, and TCEA board. This information is presented as follows:

Power Distribution — TCPD

Fuse number	Current rating	Characteristic	Voltage rating	Vendor catalog number
FU1 – FU10	5 Amps	Fast Acting	125 Volts	Bussman GMA-5A
FU13 – FU20	15 Amps	Fast Acting	125 Volts	Bussman GMA-15A
FU21 – FU26	1.5 Amps	Time Lag	250 Volts	Bussman GMC-1.5A
FU27, FU28	3.2 Amps	Time Delay	250 Volts	Bussman MDL-3.2A
FU29	15 Amps	Fast Acting	250 Volts	Bussman ABC-15
FU30	5 Amps	Fast Acting	250 Volts	Bussman ABC-5
FU31, FU32	15 Amps	Fast Acting	250 Volts	Bussman ABC-15
FU34 – FU39	5 Amps	Fast Acting	125 Volts	Bussman GMA-5A

Power Supply — TCPS

Fuse number	Current rating	Characteristic	Voltage rating	Vendor catalog number
FU1	5 Amps	Fast Acting	125 Volts	Littlefuse 225005
FU2	1.5 Amps	Fast Acting	250 Volts	Littlefuse 22501.5
FU3	8 Amps	Fast Acting	250 Volts	Buss 3AG
FU4	1.5 Amps	Fast Acting	250 Volts	Littlefuse 22501.5

Power Supply — TCEA

Fuse number	Current rating	Characteristic	Voltage rating	Vendor catalog number
FU1	1.5 Amps	Time Lag	125 Volts	Bussman GMC-1.5A
FU2, FU3	1.5 Amps	Time Lag	250 Volts	Bussman GMC-1.5A

Appendix F Big Block Reference

Introduction

The Mark V control system's software is configured by using a "block" system. Blocks are simply standardized control functions which are divided into the following categories:

- Primitives
- Generic Big Blocks
- Application Specific Big Blocks

Primitives and generic big blocks are common to all applications and may be used for minor control modifications. Application-specific big blocks are specific to individual turbine product types, performing dedicated control and protection functions.

This Appendix covers only primitives and generic big blocks, with a separate section for each category. The primitive blocks represent relatively uncomplicated functions such as Add, Subtract, Compare A ≥ B, and Shift. They are implemented as part of a sequencing rung involving additional control operations. These blocks (once enabled) will energize a coil output when a condition has been satisfied. These operations have universal applicability and may be used in any application. Generic Big Blocks may be used in a similar fashion, but do not have the ability to accept sequencing on its (enable) input or to set a coil output.

This appendix is presented as follows:

Section ***Page***

Summary of Data Types

Data received or sent by a block is called a parameter.

To implement a block correctly, the programmer must be aware of both the functionality of the block and the type of data that must be passed to it. Parameters fall into two categories:

- *Passed parameters* can be assigned. These are depicted in the Control Sequence Editor and the control sequence program printout.
- *Automatics* are parameters embedded in the block and cannot be changed. These do not appear in the Control Sequence Editor -- only in the control sequence program printout. Blocks read from and write to the control signal database according software signal names assigned to the block. In the case of passed parameters, the Control Sequence Editor (CSE) can be used to make the assignments.

In the following sections, each block description includes a list of the passed parameters of the block. Each of the parameters has a corresponding data type.

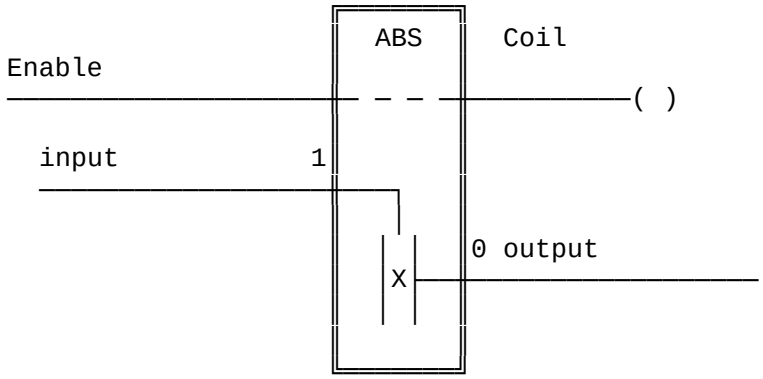
Caution

When implementing functions, an understanding of data types and their compatibility is critical. Failure to apply data types correctly may cause incorrect values to be passed to the control signal database. This may adversely affect turbine operation.

Table 1-1. Data Types Used in the Mark V LM Controller

Data Type	Description
L1	Logic state that may have a value of 1 or 0. A logic value may be forced to 0 or 1 via the logic forcing screen on the HMI. Data size is 1 byte. If the bit is forced, a "greater than" symbol (>) is displayed in front of the value. For example: `signal_name 1 LOGIC` the signal is not forced. `signal_name >1 LOGIC` the signal is forced to a logic 1. `signal_name >0 LOGIC` the signal is forced to logic 0.
A2	Numeric constant value, supplied by the user, to define a specific reference number; this is not a database point type definition.
K2	Word constant value, calculated and supplied by the sequencing editor, to define the number of data definitions used by iterative generic blocks.
S2	Enumerated state value. Enumerated states are usually presented as text, but stored and executed as a numeric value. For example, an enumerated state that represents the current status of a turbine could be: 0 stopped 1 on turning gear 2 rolling 3 at or above 70 % speed 4 at or above 95% speed 5 at 100% speed 6 decelerating 7 tripped And so on. The number values are stored and used in the execution of blocks; the text is assigned to the number in a look-up table (F:\UNITn\ENUMDATA.DAT). The text and/or value can be displayed on the screen. S2 has a range of 0 to 65535.
C4	Raw count value with a range of 0 to (2^{32} - 1) (32 bit word). Data size is 4 bytes.
F4	An integer used for dimensions, constants, and timer counters. Data size is 4 bytes.
H4	Hexadecimal value, 8 digits (0 to FFFFFFFF).
R4	An IEEE real floating point value.
V4	Any four-byte variable (that is, F4, C4, R4, or H4).

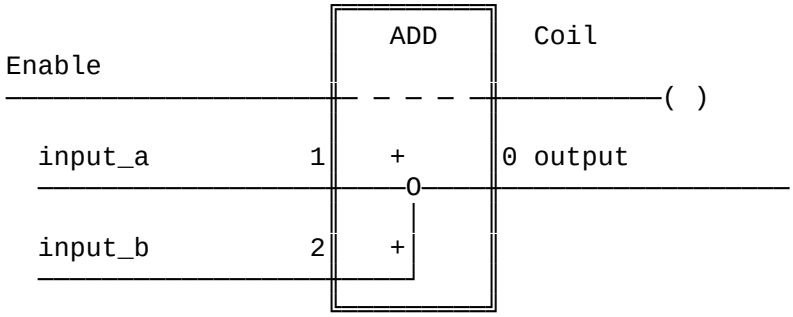
ABS -- Absolute Value



Execution of the Absolute Value (ABS) block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block performs an absolute value function on the input value and passes the result to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. A 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog quantity whose absolute value will be passed to the output.
Outputs	output	R4	Absolute value of the input figure.
	Coil	L1	Logical output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

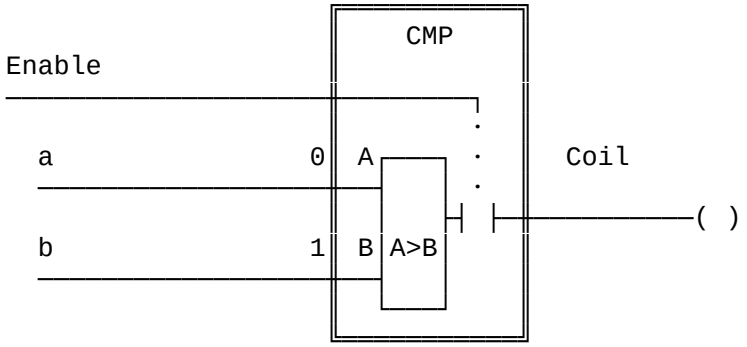
ADD



Execution of the Add block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block executes an addition operation. Analog inputs a and b are added and their sum is passed to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. A logic 1 permits function execution; a logic 0 will leave output a + b unchanged.
	Input a	R4	Analog value that is added to input b.
	Input b	R4	Analog value that is added to input a.
Outputs	output	R4	Analog sum of input values a and b.
	Coil	L1	Logic output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

CMP or CMP_A>B -- Compare A > B

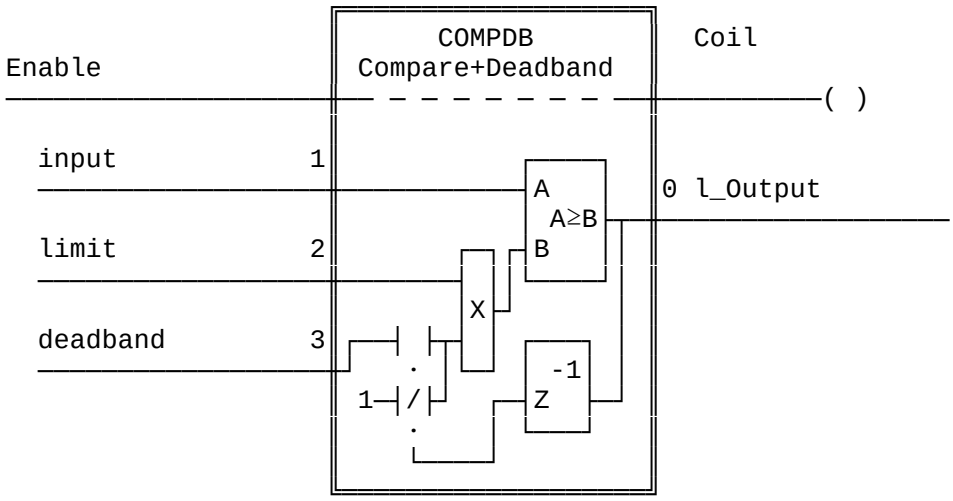


The CMP (CMP_A>B) block performs a compare operation on analog inputs a and b. Execution of the block is controlled by the Enable logical input. When the Enable input is a logic 1 and the value of analog input a is greater than input b, the Coil is set to a logic 1.

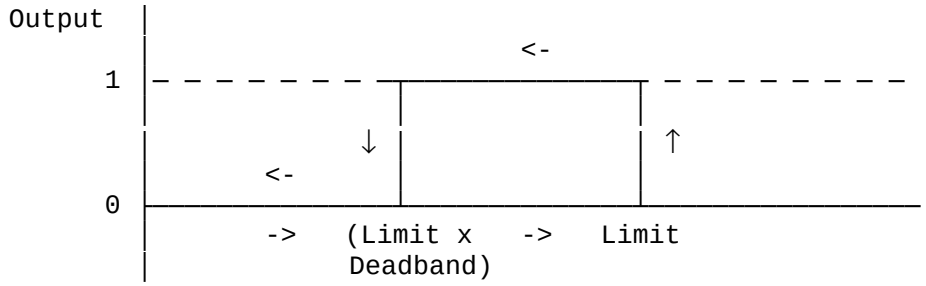
Note This block may be specified as either CMP or CMP_A>B.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines whether the function will execute. A logic 1 permits block function execution; A logic 0 will set the output to logic 0.
	a	V4	Analog value to which input b is compared.
	b	V4	AAnalog value that is compared to input a.
Outputs	Coil	L1	Output that is set to logic 1 when input a is greater than input b.

COMPDB -- Compare with Deadband

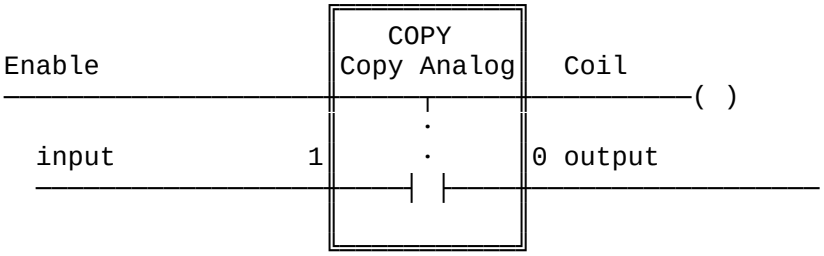


Execution of the Compare with Deadband block (COMPDB) is controlled by an Enable logical input, which is passed through to the Coil output when the block is executed. The block implements an analog compare operation with a deadband calculation after the compare limit has been exceeded. Starting with the logical output parameter l_output reset, the input value is compared with the limit. l_output remains reset while the input is less than the limit. As soon as this input exceeds the limit, the l_output is set. l_output remains set until the value of the input drops below the limit value times the deadband value. The deadband value is always between logic 0 and logic 1.



I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. A logic 1 permits function execution; a logic 0 will leave output a + b unchanged.
	input	V4	Value compared against the limit below.
	limit	V4	The input value above which l_output will initially be set.
	deadband	V4	The multiplier from which the second (return to zero) limit is calculated.
Outputs	l_output	R4	The logical result of the comparison. When enabled, transitions from logic 0 to logic 1 when the input becomes greater than the limit, then back to logic 0 when the input drops below limit deadband.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

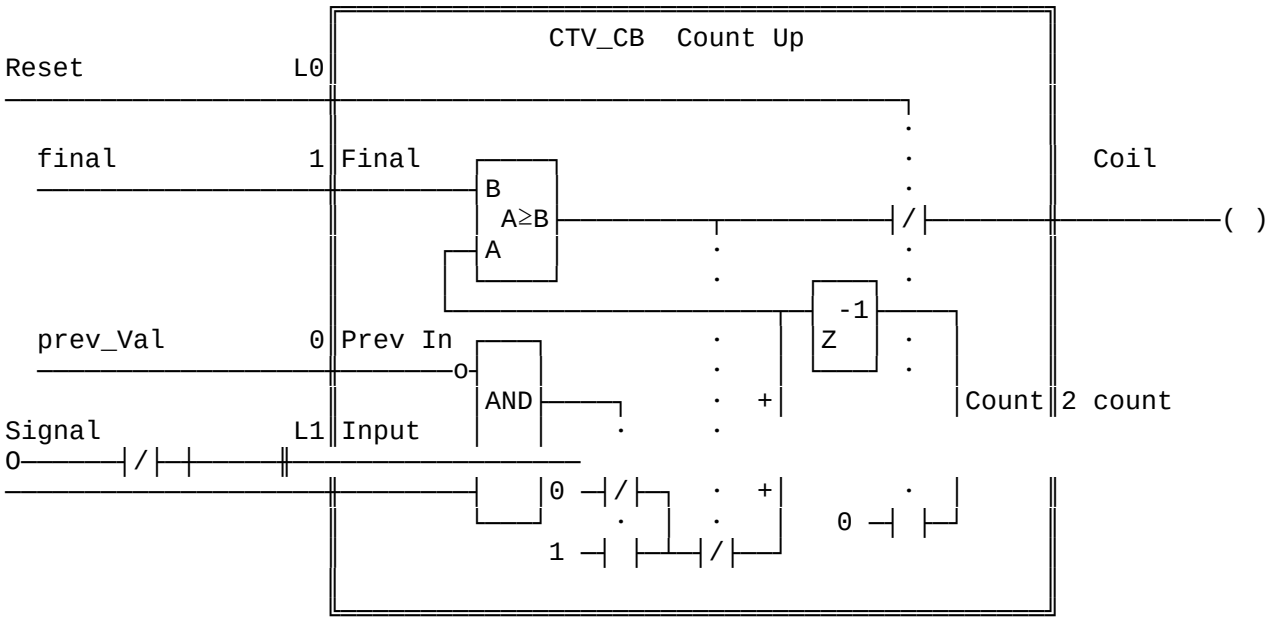
Copy



Execution of the Copy block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block passes the analog input to the output.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits block execution; a logic 0 will leave the output unchanged.
	input	V4	Analog value that is passed to the output.
Outputs	output	V4	Analog value that is passed from the input.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

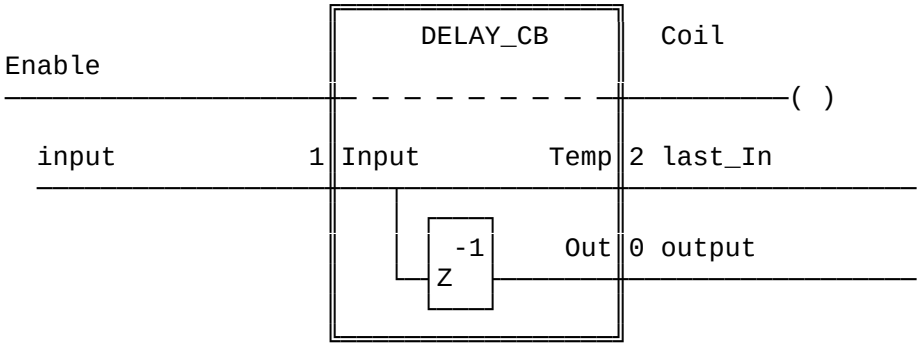
CTV -- Event Counter



The CTV block executes a count operation when the logic Signal input transitions from logic 0 to logic 1. When a transition occurs, the event count is incremented by one. To recognize the next transition in the logic signal, the new logic input is stored in the prev_val parameter. If the count reaches a point equal to the final value, the output Coil is set to logic 1. The event count and the Coil output are reset to logic 0 when a logic 1 is received from the Reset input.

I/O	Para-meter	Data Type	Description
Inputs	Reset	L1	Logic 1 input that resets the event counter and the Coil output.
	Signal	L1	The logic input whose logic 0 to logic 1 transitions are counted.
	prev_val	L1	Logic parameter use to store the previous value of the Signal input.
	final	F4	The block will set the Coil output to logic 1 when the counter reaches a value equal to this figure.
Outputs	Coil	L1	Output that is set to logic 1 if the counter figure reaches a quantity equal to the final value. It will be reset when a logic 1 is received from the Reset input, and remains reset until the count again exceeds the final value.
	count	F4	Records number of 0-to-1 transitions in logic value of the Signal input.

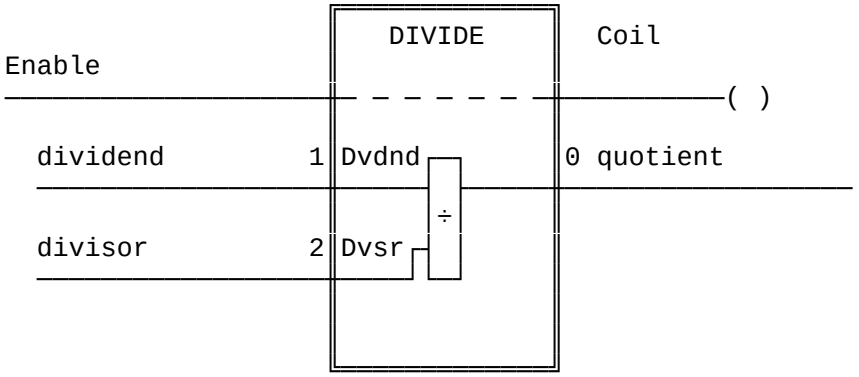
Delay



Execution of the Delay block is controlled by the Enable logical input, which is passed through to the output when the block is executed. The Delay block performs a single sweep delay function on analog input data before it is passed to the output. The previous value is held (last_in) until the next execution of the block. When the next execution occurs, the value is passed to the output.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution (enable set); a logic 0 will leave the output unchanged.
	input	R4	Analog value that is stored in the Temp storage location.
Outputs	output	R4	Analog value that has been stored for one execution of the block.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.
	Last_in	R4	Temporary storage location that holds the value of the input for one execution of the block before it is passed to the output.

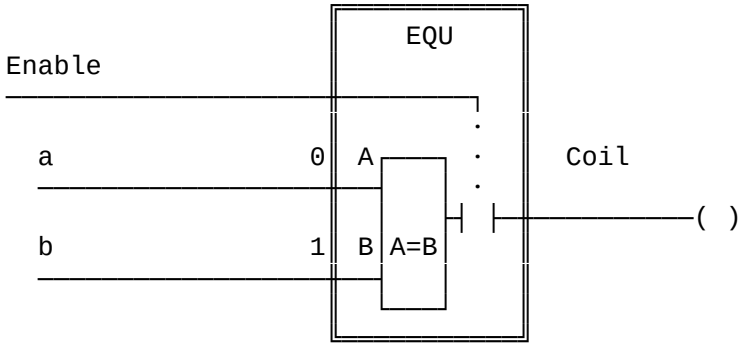
DVD -- Divide



Execution of the Divide block is controlled by the Enable logical input, which is passed through to the Coil output when the function is executed. The block executes a divide operation using analog inputs for the dividend and divisor.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. A logic 1 permits function execution; a logic 0 will leave the quotient unchanged.
	dividend	R4	Analog input that is divided by the input value of the divisor.
	divisor	R4	Analog input divisor by which the dividend is divided.
Outputs	quotient	R4	Analog value that is the result of the division of the dividend by the divisor.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

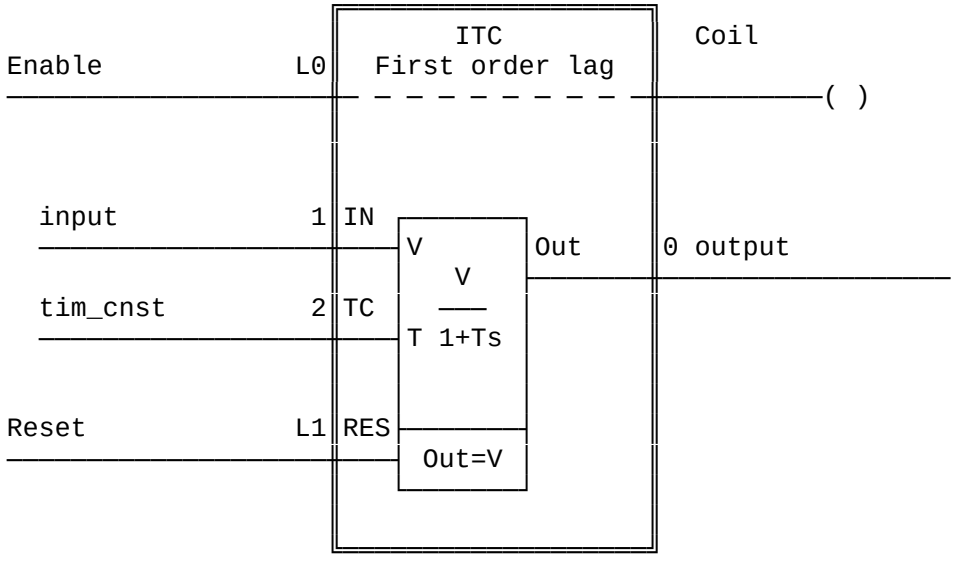
EQU -- Compare A = B



The EQU (CMP_A=B) block performs a compare operation on analog input a and b. Execution of the block is controlled by the Enable logical input. When the Enable input is a logic 1 and analog inputs a and b are equal, the Coil is set to a logic 1.

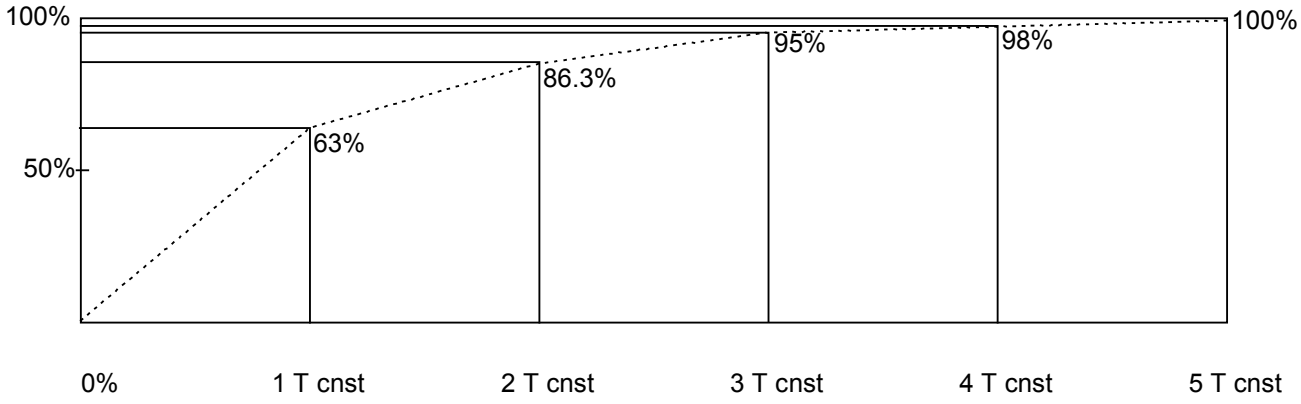
I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines whether the function will execute. A logic 1 permits function execution; a logic 0 will set the Coil to logic 0.
	a	V4	Analog value that is compared to input b.
	b	V4	Analog value that is compared to input a.
Outputs	Coil	L1	Output that is set to logic 1 when the value of input a equals the value of input b.

ITC -- Integral Time Constant



Execution of the Integral Time Constant block is controlled by the Enable logical input—which is passed through to the Coil output when the block is executed. The ITC block executes a lag function. The value of the output approaches the value of the input at a rate determined by the time constant. The difference between the input and output values represents 100% of the change of the output. The time constant represents the time needed to raise (or lower) the output 63% of the difference between the input and output. Therefore, it takes 5 time constants to change the output approx. 100% of the difference (1 sec.= 63% of 100%, 2nd sec. = 63% of 37%, 3rd sec. = 63% of 13.7%, 4th sec. 63% of 5%, 5th sec. = 63% of 2%). (See example below.)

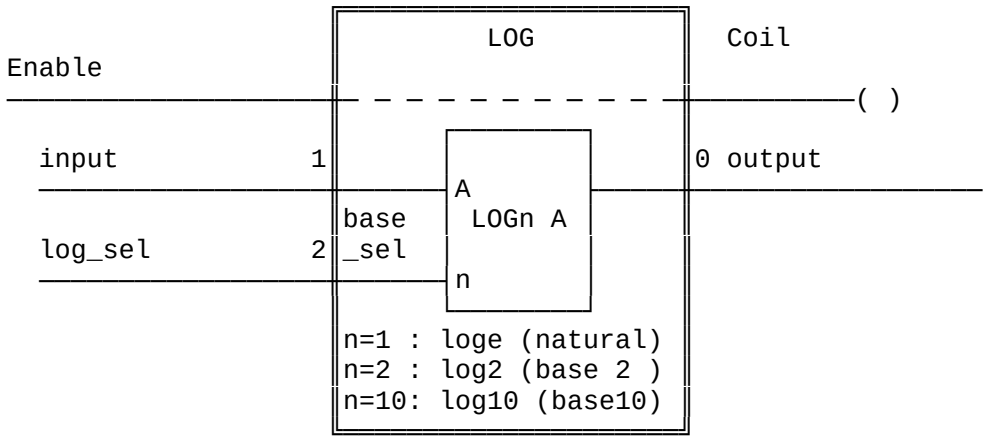
Example: Input = 100% Output = 0% Tim_Cnst = 1sec.



A logic 1 on the Reset logical sets the output to the current input value immediately. The time constant value should be at least four times the sequencing scan interval.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog value that is used to calculate the current value of the output.
	tim_cnst	R4	Analog value that represents the time needed to raise/ lower the output 63% of the current difference between the input and output.
	Reset	L1	A logic 1 on the reset logical sets the output to the current input value immediately.
Outputs	output	R4	Analog value that lags the input.
	Coil	L1	Output is set to logic 1 when the function is executed (enable set); otherwise, it will be set to logic 0.

LOG -- Logarithm



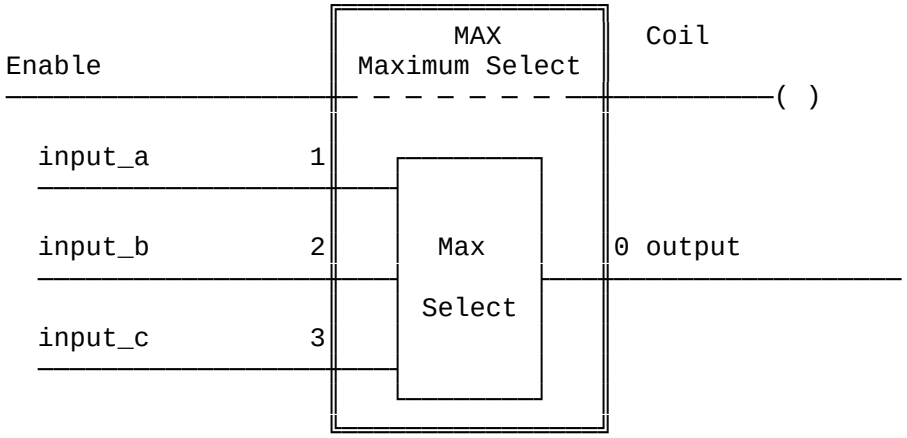
Execution of the Logarithm block is controlled by the Enable logical input—which is passed through to the Coil output when the block is executed. The LOG block executes a logarithm function. The input *log_sel* determines the type of logarithm that is executed:

log_sel	Logarithm function executed
1	Natural logarithm, $f(x) = \log_e(x) = \ln(x)$
2	base 2 logarithm, $f(x) = \log_2(x)$
10	base 10 logarithm, $f(x) = \log_{10}(x)$

The value of the output is the selected logarithm function evaluated at the input.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog value that is used to calculate the current value of the output.
	log_sel	F4	Analog value that selects the type of logarithm function to be executed.
Outputs	output	R4	Analog value that is the selected logarithm function evaluated at the input.
	Coil	L1	Output is set to logic 1 when the function is executed (enable set): otherwise, it will be set to logic 0.

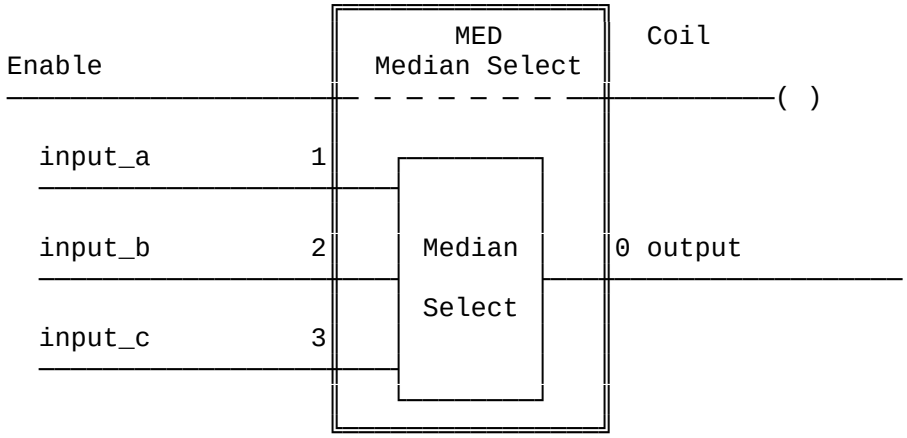
MAX -- Maximum Select



Execution of the Maximum Select block is controlled by the Enable logical input, which is passed through to the Coil output as when the block is executed. The block implements a comparison of three analog inputs. The largest of these inputs is selected and passed to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. Logic 1 permits function execution; logic 0 will leave the output unchanged.
	input_a	V4	Analog value that is compared to inputs b and c.
	input_b	V4	Analog value that is compared to inputs a and c.
	input_c	V4	Analog value that is compared to inputs a and b.
Outputs	Output	V4	Analog value that is the selected logarithm function evaluated at the input.
	Coil	L1	Output is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

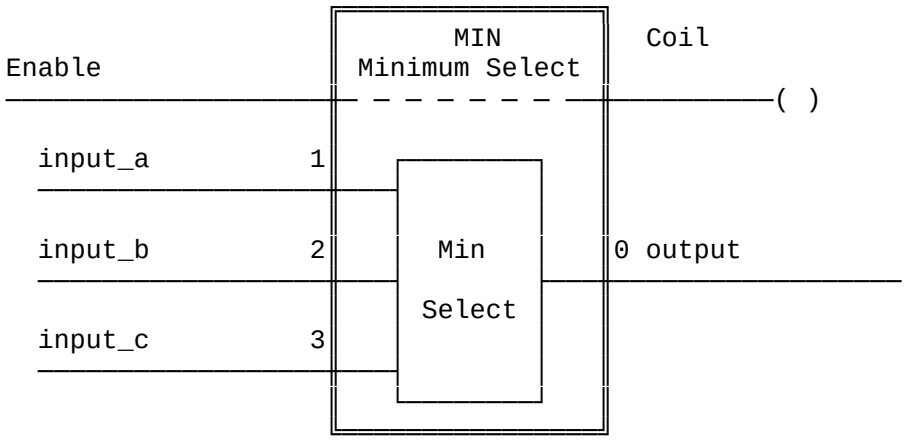
MEDIAN -- Median Select



Execution of the Median Select block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block implements a comparison of three analog inputs. The middle value of the three is selected and passed to the output.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. Logic 1 permits function execution; logic 0 will leave the output unchanged.
	input_a	V4	Analog value that is compared to inputs b and c.
	input_b	V4	Analog value that is compared to inputs a and c.
	input_c	V4	Analog value that is compared to inputs a and b.
Outputs	output	V4	Analog quantity set to the median value of inputs a, b, and c.
	Coil	L1	Output is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

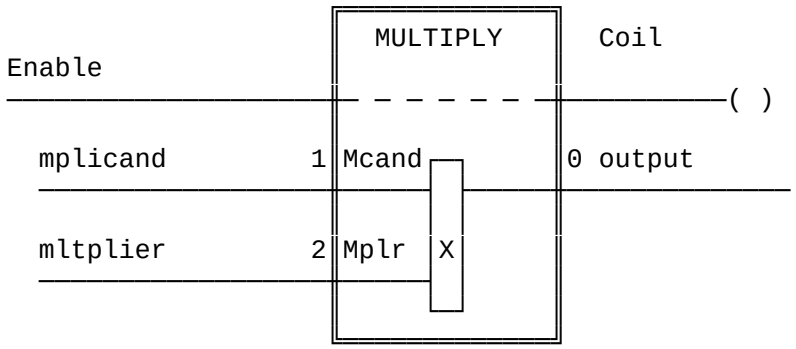
MIN -- Minimum Select



Execution of the Minimum Select block is controlled by the Enable logical input, which is passed through to the Coil when the block is executed. The block implements a comparison of three analog inputs. The smallest of these inputs is selected and passed to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines block execution mode. Logic 1 permits function execution; logic 0 will leave the output unchanged.
	input_a	V4	Analog value that is compared to inputs b and c.
	input_b	V4	Analog value that is compared to inputs a and c.
	input_c	V4	Analog value that is compared to inputs a and b.
Outputs	output	V4	Analog quantity set to the smallest value of inputs a, b, and c.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0

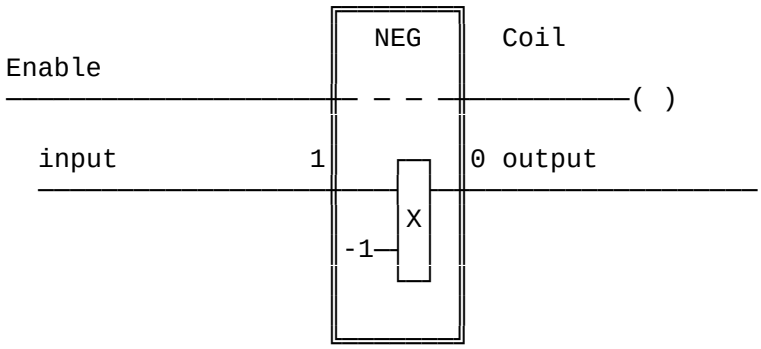
MPY -- Multiply



Execution of the Multiply block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block executes a multiplication operation on analog input values *mplicand* and *mltplier*.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	mplicand	R4	Analog value that is multiplied by input mltplier (multiplier).
	mltplier	R4	Analog value that is multiplied by input mplicand (multiplicand).
Outputs	output	R4	Analog value that is the product of the inputs.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

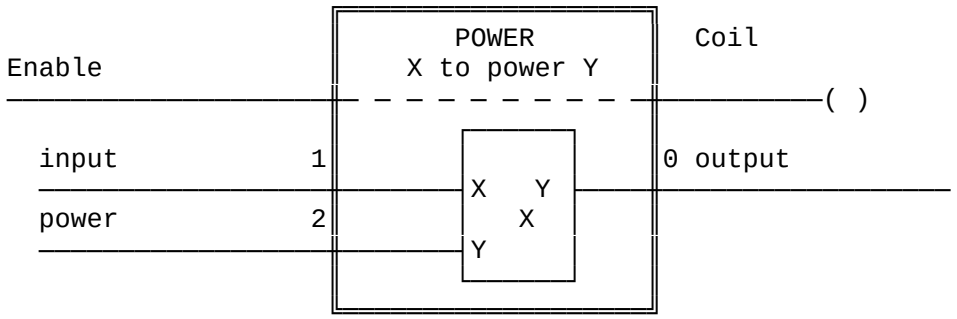
NEG -- Negative



Execution of the Negative (NEG) block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block multiplies analog input data by -1 before it is passed to the output.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog value that is multiplied by -1 before it is passed to the output.
Outputs	Coil	L1	Output that is set to logic 1 if the block is executed (enable set); otherwise, it will be set to logic 0.
	output	R4	Analog value that has been multiplied by -1.

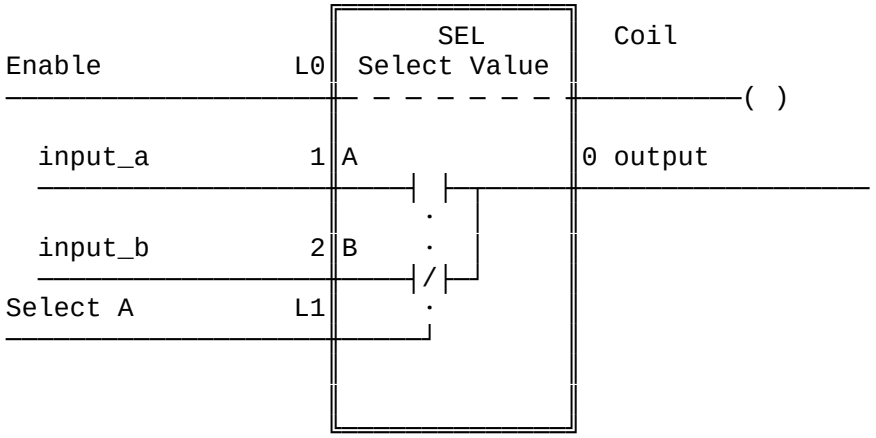
POWER -- Exponentiation



Execution of the Exponentiation block is controlled by the Enable logical input—which is passed through to the Coil output when the block is executed. The POWER block executes an exponentiation. The value of the output is simply the value of the input, raised to the given exponent.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog value that is used to calculate the current value of the output.
	power	R4	Analog value that is the exponent.
Outputs	output	R4	Analog value that is the input raised to the exponent.
	Coil	L1	Output is set to logic 1 when the function is executed (enable set): otherwise, it will be set to logic 0.

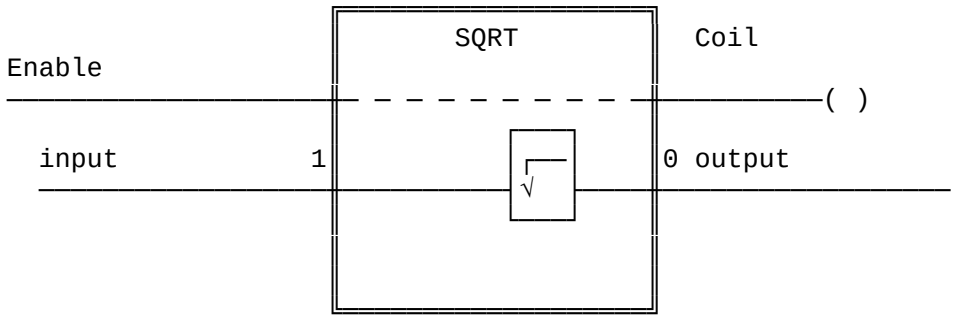
SEL -- Select



Execution of the Select block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. When Select_A is false, the block passes the analog value of input_b to the output. However, when the block receives a logic 1 input on Select_A, input_a is passed to the output.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	Select_A	L1	When false, the Select_A logical input passes the value of input_b to the output; otherwise, the value of input_a is passed to the output.
	input_a	V4	Analog value that replaces input_b as the output when the Select_A logic input reads logic 1.
	input_b	V4	Analog value which the block will pass to the output when a logic 0 signal is received on the Select_A input.
Outputs	output	V4	Analog value selected from either input_a or input_b.
	Coil	L1	Output that is set to logic 1 if the function is executed; otherwise, it will be set to logic 0.

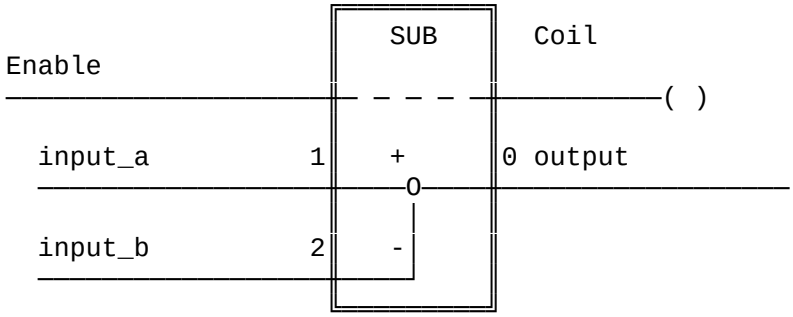
SQRT -- Square Root



Execution of the Square Root block is controlled by the Enable logical input, which is passed to the Coil output when the block is executed. The block executes a square root function.

I/O	Para-meter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input	R4	Analog value that is the input to the square root function.
	log_sel	F4	Analog value that selects the type of logarithm function to be executed.
Outputs	output	R4	The result of the Square Root operation.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

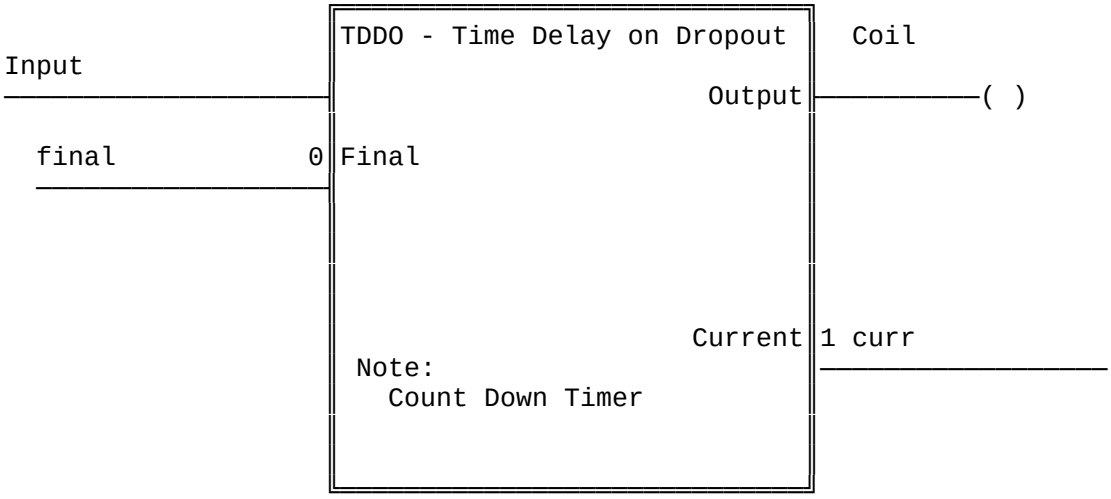
SUB -- Subtract



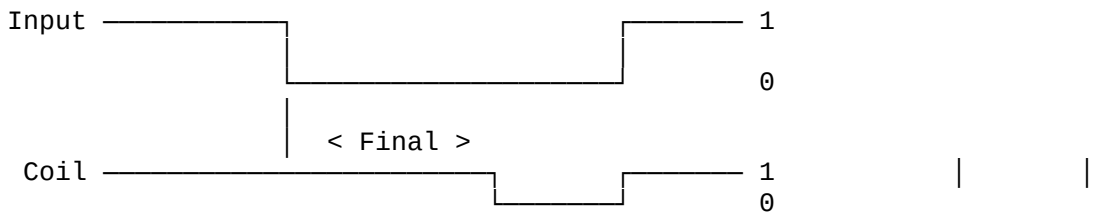
Execution of the Subtract block is controlled by the Enable logical input, which is passed through to the Coil output when the block is executed. The block executes a subtraction operation. The analog value of input_b is subtracted from input_a. The difference between the two inputs is then passed to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	The Enable logical input determines the block execution mode. A logic 1 permits function execution; a logic 0 will leave the output unchanged.
	input_a	R4	Analog value from which input_b will subtracted.
	input_b	R4	Analog value that is subtracted from input_a.
Outputs	output	R4	Analog difference between input_a and input_b.
	Coil	L1	Output that is set to logic 1 if the function is executed (enable set); otherwise, it will be set to logic 0.

TDDO -- Time Delay Drop Out

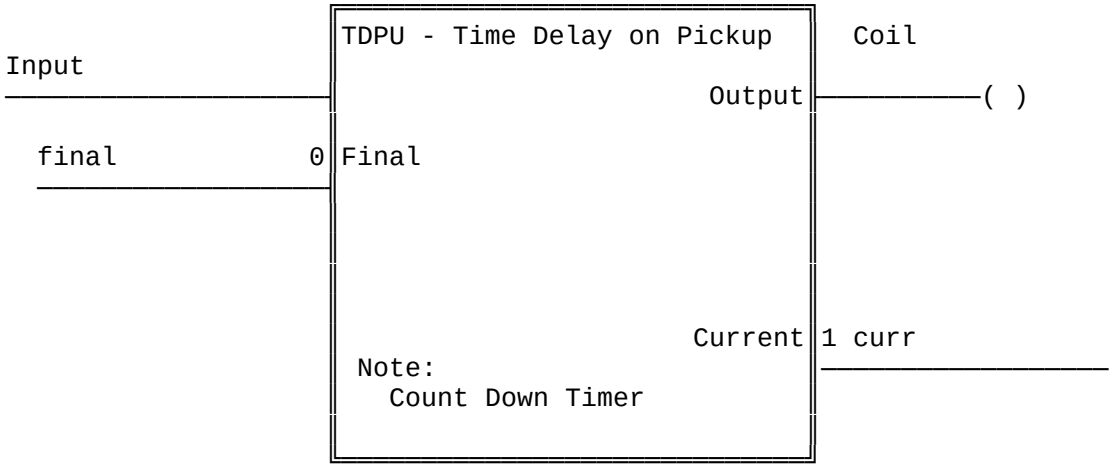


The TDDO block performs a time delay function. Execution of the block is controlled by the logical input. When a logic 0 is received, the timer function begins executing. When the input signal transitions from logic 1 to logic 0, elapsed time (sec.) is tabulated in the current counter. When the total in the counter equals the value of the final constant, the Coil output is set to logic 0. A true input signal will reset the current counter and the Coil output to logic 1 immediately.

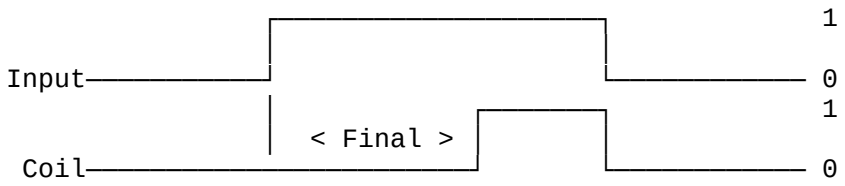


I/O	Parameter	Data Type	Description
Inputs	Input	L1	The input determines the block execution mode. A logic 0 permits function execution; a logic 1 will reset the counter and the Coil output to 1.
	final	F4	A time duration constant that when reached by the counter, permits the Coil output to be set to logic 0.
Outputs	Coil	L1	Output is set to logic 1 when the function is executed (enable set): otherwise, it will be set to logic 0.
	curr	F4	Records elapsed time (sec.) after a logic 0 is received from the Input.

TDPU -- Time Delay Pick Up

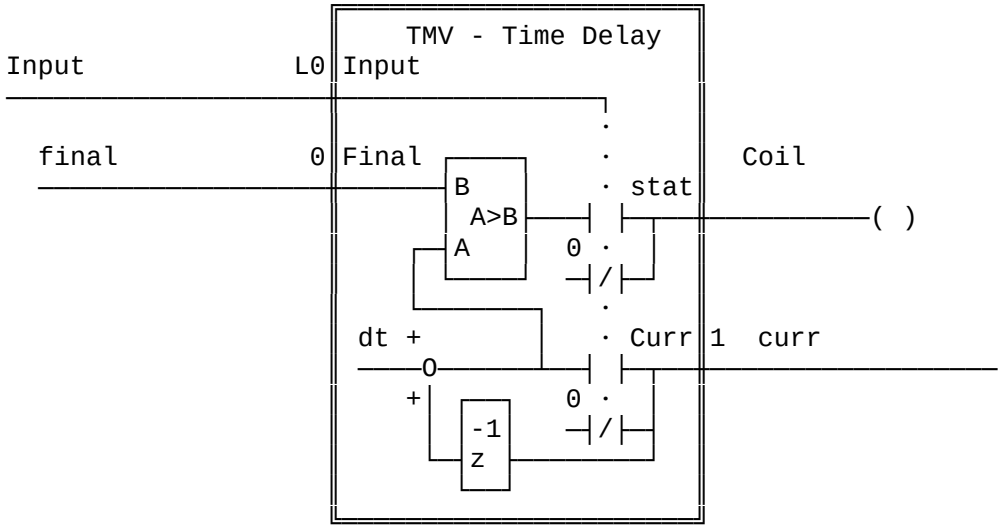


The TDPU block performs a time delay function. Execution of the block is controlled by the logical input. When a logic 1 is received, the timer function begins executing. When the input signal transitions from logic 0 to logic 1, elapsed time (sec.) is tabulated in the current counter. When the total in the counter equals the value of the final constant, the Coil output is set to logic 1. A false input signal will reset the current counter and the Coil output to logic 0 immediately.

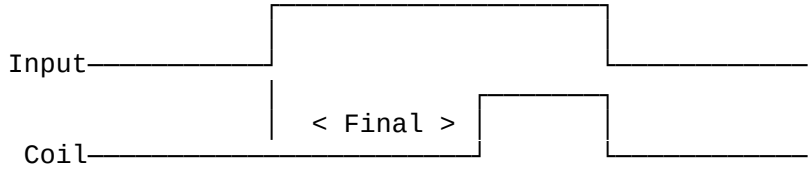


I/O	Parameter	Data Type	Description
Inputs	Input	L1	The input determines the block execution mode. A logic 1 permits function execution; a logic 0 will reset the counter and the Coil output to 0.
	final	F4	A time duration constant that when reached by the counter, permits the Coil output to be set to logic 1.
Outputs	Coil	L1	Output that is set to logic 1 when the amount in the current counter equals the Final value.
	curr	F4	Records elapsed time (sec.) after a logic 1 is received from the Input.

TMV -- Time Delay

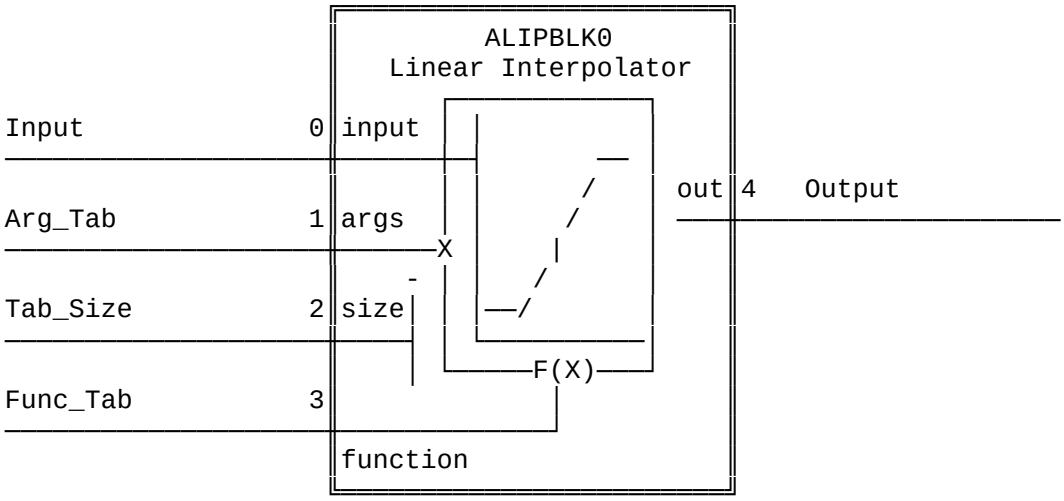


The TMV block performs a time delay function. Execution of the block is controlled by the logical input. When a logic 1 is received, the timer function begins executing. When the input signal transitions from logic 0 to logic 1, elapsed time (sec.) is tabulated in the current counter. When the total in the counter equals the value of the final constant, the Coil output is set to logic 1. A false input signal will reset the current counter and the Coil output to logic 0 immediately.



I/O	Parameter	Data Type	Description
Inputs	Input	L1	The input determines the block execution mode. A logic 1 permits function execution; a logic 0 will reset the counter and the Coil output to 0.
	final	F4	A time duration constant that when reached by the counter, permits the Coil output to be set to logic 1.
Outputs	Coil	L1	Output that is set to logic 1 when the amount in the current counter equals the Final value.
	curr	F4	Records elapsed time (sec.) after a logic 1 is received from the Input. Maximum recordable time is determined by system scaling of time in seconds.

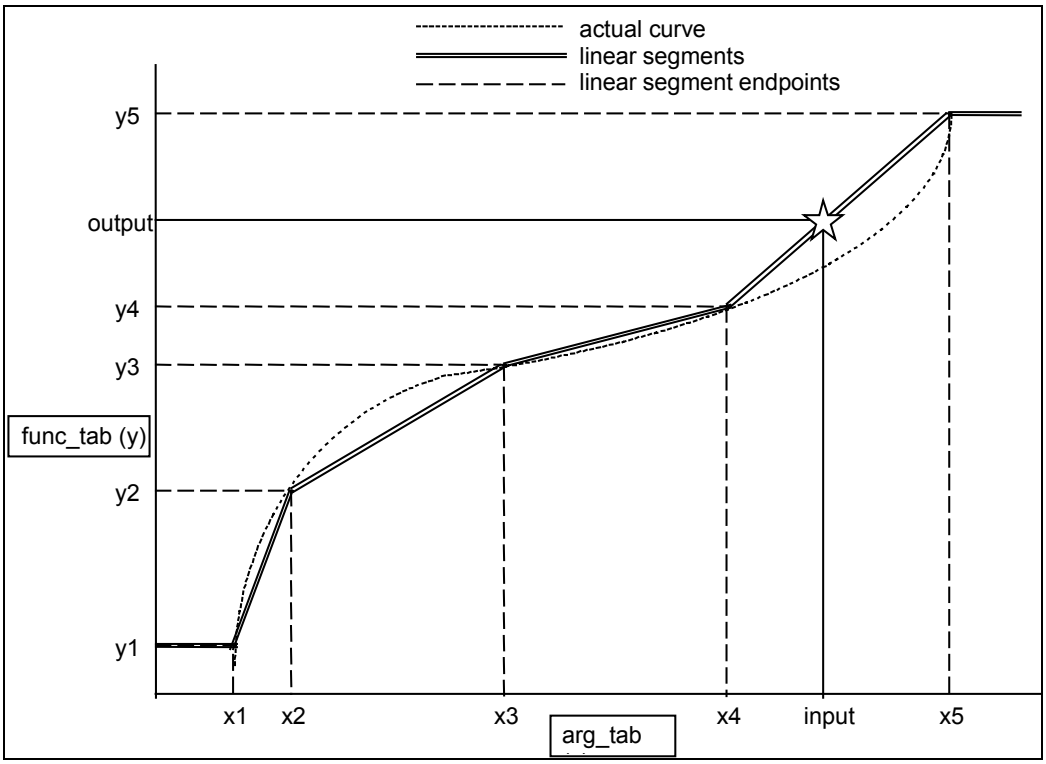
ALIPBLK0 -- Analog Linear Interpolation Block



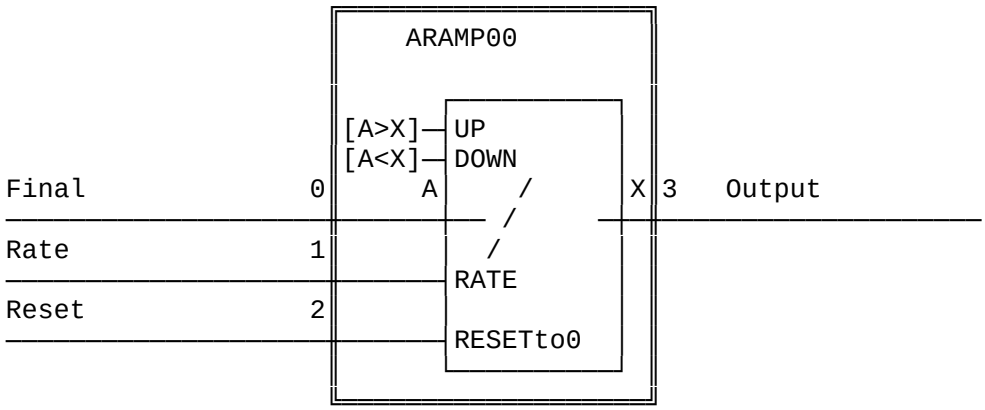
The Analog Linear Interpolation block approximates a continuous relationship between the input and the output as a series of connected linear segments. These segments are defined by the pairs of corresponding values in the argument table and the function table. The argument table values are the values of the input where a new linear segment in the approximation begins. The argument entries must be entered in a numerically increasing order.

The function table values are the desired output values at the points defined in the argument table. For input values located between argument table entries, standard linear interpolation is performed between the corresponding function table entries to calculate the output value. If the input value is outside of the range of the argument table, the output is clamped to either the first or last element of the function table. As the number of argument table locations increases, the table size should increase correspondingly (table_size must be positive). As table size increases, resolution of the linear interpolation will increase and execution speed will decrease. An illustration of this function is given in the following diagrams.

I/O	Parameter	Data Type	Description
Inputs	Input	R4	Analog value used to locate the proper linear segment in the argument table, and interpolate between its endpoints.
	Arg_Tab	R4	Index of constant values that define where a new linear segment of the approximation begins. Must be the same size as the function table.
	Func_Tab	R4	Desired output values at points defined in the argument table.
	Tab_Size	A2	Number of entries in the argument table and function table.
Outputs	Output	R4	The approximation to the output value for the function represented in the Argument and Function Tables.


actual curve
linear segments
linear segment endpoints
y5
output
y4
y3
func_tab (y)
y2
y1
x1
x2
x3
x4
input
x5
arg_tab

ARAMP00 -- Analog Ramp Block



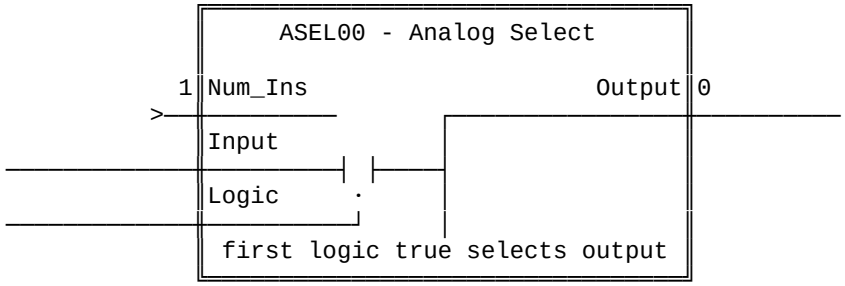
The Analog Ramp block executes a function that increments a value (X) up (A>X) or down (A<X) until the final (input) value (A) is reached. The output (X) is modified during each scan according to the value supplied to the rate input. The output is compared to the final input and the rate value is added or subtracted from the output according to the result of the compare. The output will be clamped when it reaches the final value. If the reset logical input reads 1, the output will be set to 0.

I/O	Parameter	Data Type	Description
Inputs	Final	R4	Analog value that the output will reflect when the block has executed its function.
	Rate	R4	Analog constant that represents the rate at which the output is ramped (up or down) to reflect the final input.
	Reset	R4	Logical input that sets the Output to 0 when it reads 1.
Outputs	Output	R4	Analog value that equals the Final input when the block has executed its function.

ASEL00 -- Analog Select

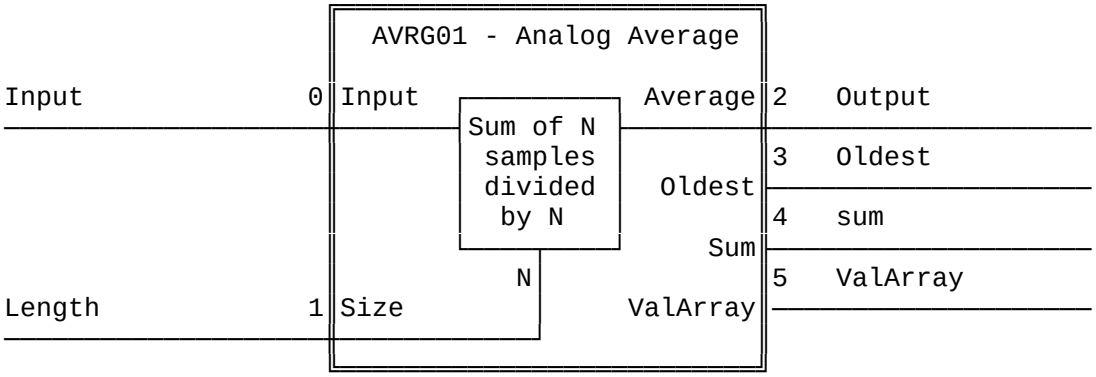
```
                              ASEL00
                                                                  output
input_1  logic_1  input_2  logic_2  input_3  logic_3  input_4
logic_4  input_5  logic_5  input_6  logic_6  input_7  logic_7
input_8  logic_8  input_9  logic_9  input_10 logic_10 input_11
logic_11 input_12 logic_12 input_13 logic_13 input_14 logic_14
input_15 logic_15 input_16 logic_16 input_17 logic_17 input_18
logic_18 input_19 logic_19 input_20 logic_20 input_21 logic_21
input_22 logic_22 input_23 logic_23 input_24 logic_24 input_25
logic_25 input_26 logic_26 input_27 logic_27 input_28 logic_28
```

The ASEL00 block reads a list of logic inputs (max. 28), determines the first true logic, and passes its corresponding analog variable to the output. The picture below is an abbreviated representation of the block functionality.



I/O	Para-meter	Data Type	Description
Inputs	Num_Ins	K2	Number of entry sets for ASEL00. This block may be used multiple times within a single Control Sequence Program (max. 28 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
	State_n	V4	Analog variables that correspond to logic inputs.
	Logic_n	L1	Logic inputs.
Outputs	Output	V4	Analog value that represents the corresponding variable of the first sequential logic input that reads true.

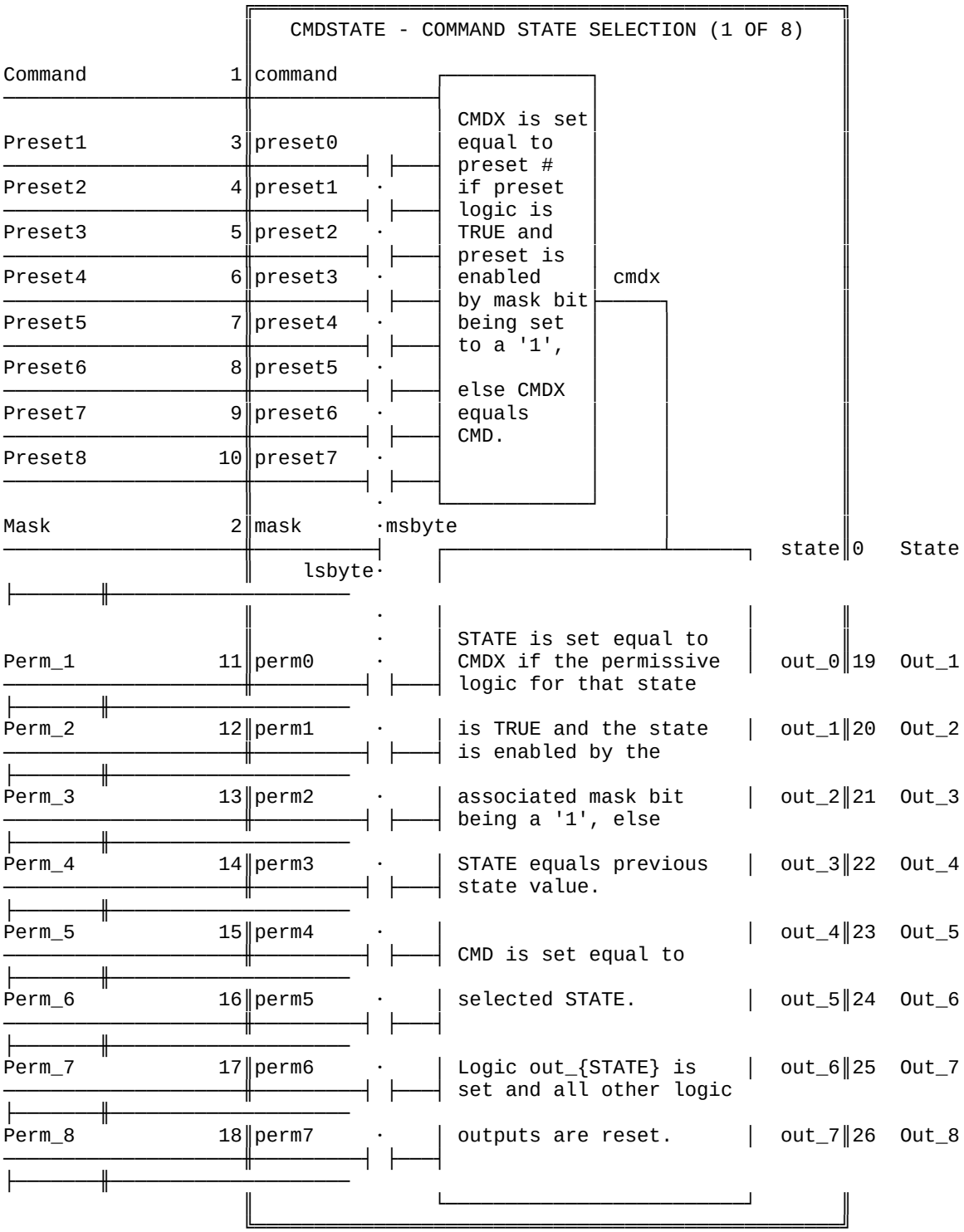
AVRG01 -- Analog Average Block



The Average block calculates the rolling average of a sequence of input values. A list of previous values is stored in a value array (ValArray []). Once the average is calculated, the value is passed to the output. The first execution of the block initializes the array to the very first input value. Subsequent analog values stored in this location are entered and exited on a first in - first out basis. That is, new values entering the array successively displace the oldest value of the list. To accelerate the computation of the array's rolling average, the oldest value is temporarily stored in oldest. This value is recalled and utilized to calculate the new average. Subsequent calculations will use different oldest values as they are replaced with each update of the array. The value assigned as the length must equal the array's actual number of storage cells to generate accurate results from this operation.

I/O	Parameter	Data Type	Description
	Input	R4	Analog value that is used to generate the rolling average.
	Length	A2	The storage capacity of the value array.
Outputs	Output	R4	Analog value equal to the rolling average of the input values over the number of samples given in Length.
	Oldest	F4	Temporary storage location that records the oldest value in the value array while the block is running.
	Sum	R4	Summation of values in value array.
	ValArray	R4	Array of previous values.

CMDSTATE -- Command State



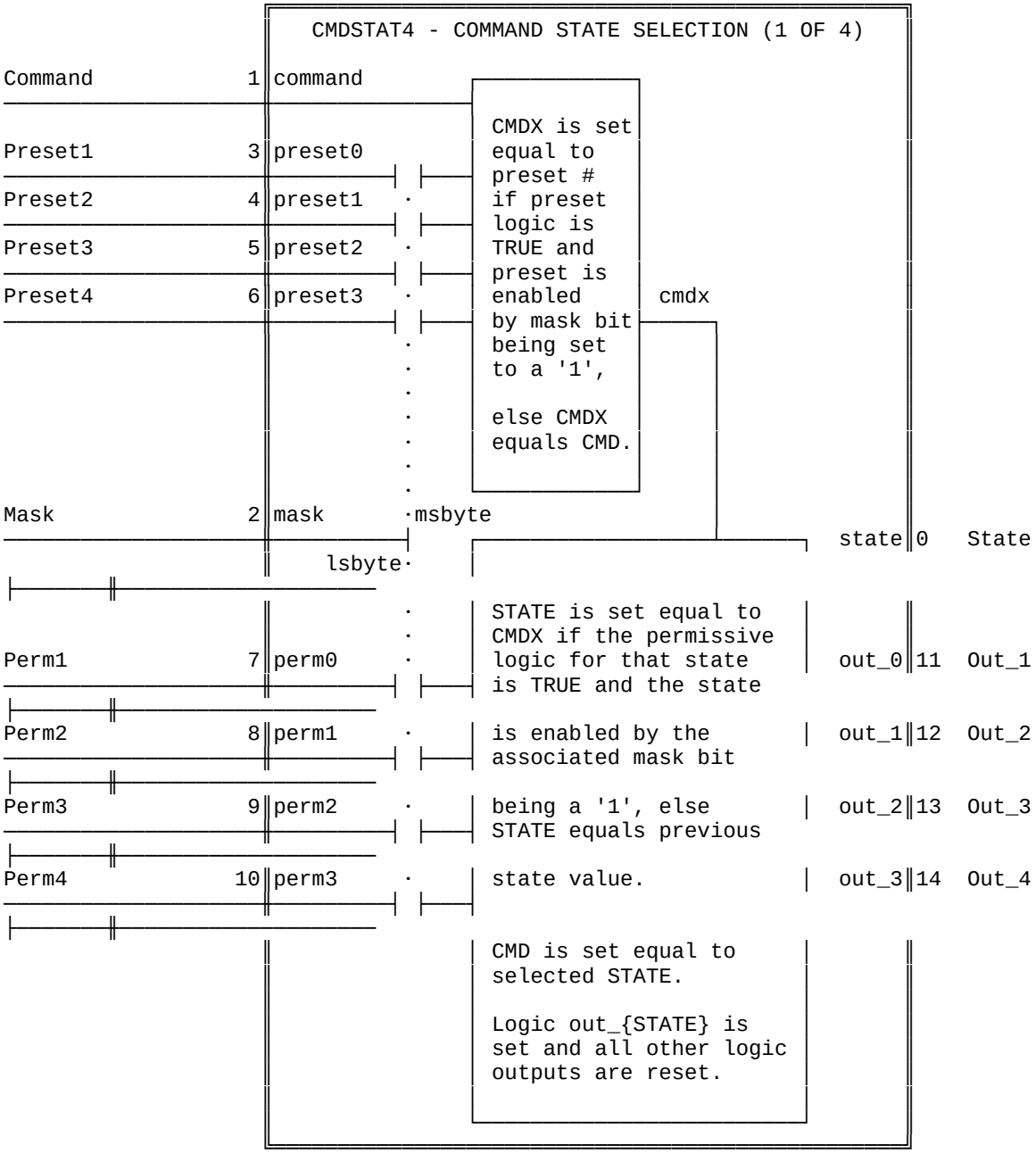
The Command State block selects one of eight mutually exclusive operational states and generates data reflecting the selected state. The (0-7) command variable received as an analog setpoint must pass the conditions set by a 16 bit mask before it is passed to the State output. The mask value is a control constant that contains the bit values of the mask. The upper or most significant byte of the mask contains enabling data for a consecutive series of 8 preset states (0-7).

If a 1 logic input to a preset state is true, and the corresponding bit of the mask value is set, the command variable is changed to that state. The command variable will be changed to the first preset state that meets these criteria. When the preset condition evaluation is completed, the command variable is processed against the second part (least significant byte) of the mask (This comparison will occur whether the command variable value is changed or not).

The LSB of the mask contains enabling data for a consecutive series (0-7) of permissive states. If the command variable corresponds to a Permissive state that has a logic true input and an LSB mask bit set, the variable is passed to the state output. This output regulates the 8 logic state outputs of the block. If the State output is set to 0, the first logic output is set to 1 and the other outputs are reset: similarly, higher numbered states will set the associated output and reset the rest of the array.

I/O	Parameter	Data Type	Description
Inputs	Command	S2	Input variable that is compared to mask requirements before it is passed to the output.
	Mask	H4	Set of conditions stored in a two-byte configuration (preset, permissive) that the command variable must pass before it is passed to the State output.
	Preset1 – Preset8	L1	A logic 1 input for one of these variables requests that the command variable be changed to a value of 0 to 7, respectively.
	Perm1 – Perm8	L1	A logic 1 input for one of these variables, and a corresponding LSB mask bit that is set will allow the command variable to be passed to the State output if the command variable value is 0 to 7, respectively.
Outputs	State	S2	Output that regulates the 8 logic outputs of the block.
	Out_1 – Out_8	L1	Logic outputs that correspond to the 8 permissive states the block will allow.

CMDSTAT4 -- Command State Four



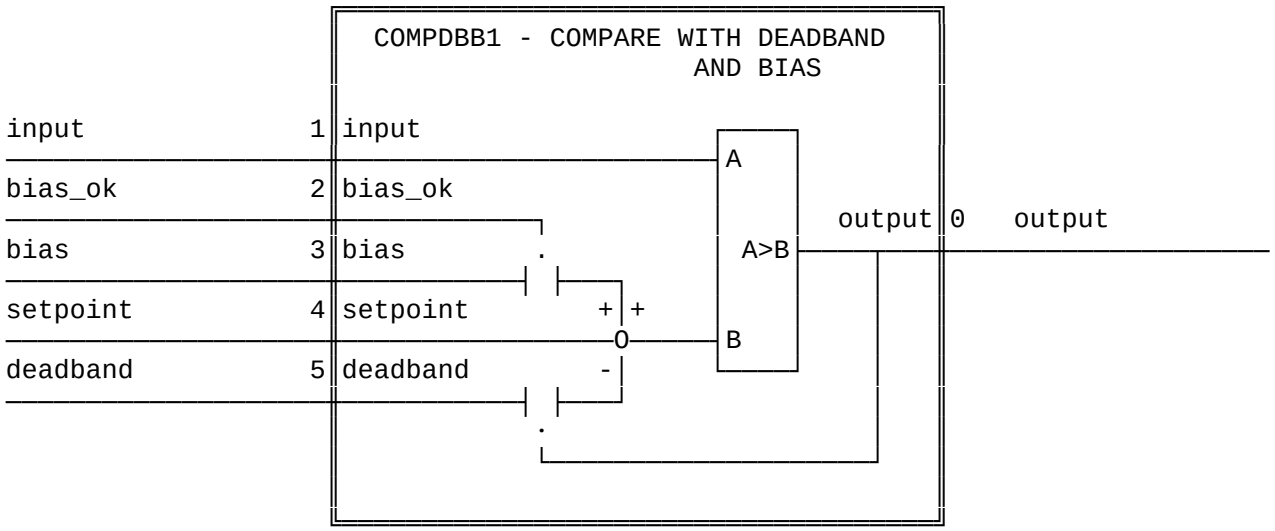
The Command State block selects one of four mutually exclusive operational states and generates data reflecting the selected state. The (0-3) command variable received as an analog setpoint must pass the conditions set by a 16 bit mask before it is passed to the State output. The mask value is a control constant that contains the bit values of the mask. The upper or most significant byte of the mask contains enabling data for a consecutive series of 4 preset states (0-3).

If a 1 logic input to a preset state is true, and the corresponding bit of the mask value is set, the command variable is changed to that state. The command variable will be changed to the first preset state that meets these criteria. When the preset condition evaluation is completed, the command variable is processed against the second part (least significant byte) of the mask (This comparison will occur whether the command variable value is changed or not).

The LSB of the mask contains enabling data for a consecutive series (0-3) of permissive states. If the command variable corresponds to a Permissive state that has a logic true input and an LSB mask bit set, the variable is passed to the state output. This output regulates the 4 logic state outputs of the block. If the State output is set to 0, the first logic output is set to 1 and the other outputs are reset: similarly, higher numbered states will set the associated output and reset the rest of the array.

I/O	Parameter	Data Type	Description
Inputs	Command	S2	Input variable that is compared to mask requirements before it is passed to the output.
	Mask	H4	Set of conditions stored in a two-byte configuration (preset, permissive) that the command variable must pass before it is passed to the State output.
	Preset1 – Preset4	L1	A logic 1 input for one of these variables requests that the command variable be changed to a value of 0 to 3, respectively.
	Perm1 – Perm4	L1	A logic 1 input for one of these variables, and a corresponding LSB mask bit that is set will allow the command variable to be passed to the State output if the command variable value is 0 to 3, respectively.
Outputs	State	S2	Output that regulates the 4 logic outputs of the block.
	Out_1 – Out_4	L1	Logic outputs that correspond to the 4 permissive states the block will allow.

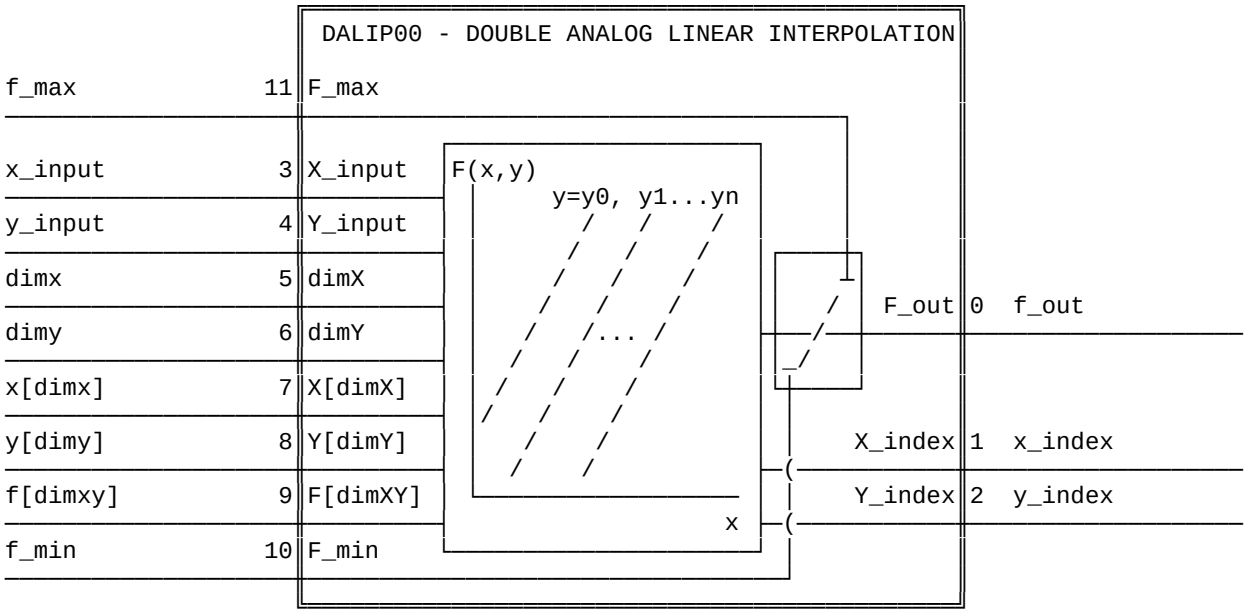
COMPDBB1 -- Compare with Deadband and Bias



The Compare with Deadband and Bias block executes a function that compares an analog variable (input) with a setpoint value; if the input exceeds the setpoint value, the output will be set. A True bias_ok logic input will cause a bias value to be added to the setpoint constant before it is compared against the input variable. When the output is set, a deadband calculation is initiated. The output is reset when the input drops below the difference of the setpoint and deadband values.

I/O	Para-meter	Data Type	Description
Inputs	input	R4	Analog variable that is compared to the setpoint value. If the input exceeds the setpoint value, the output is set to logic 1.
	bias_ok	L1	Logic input that when True, causes a bias value to be added to the setpoint before it is compared to the input.
	bias	R4	Value that is added to the setpoint input when bias_ok is True.
	setpoint	R4	Analog constant that is compared to the input.
	deadband	L1	Analog constant that is subtracted from the setpoint when the output is set.
Outputs	output	L1	Logic that reads True when the input value exceeds the setpoint value.

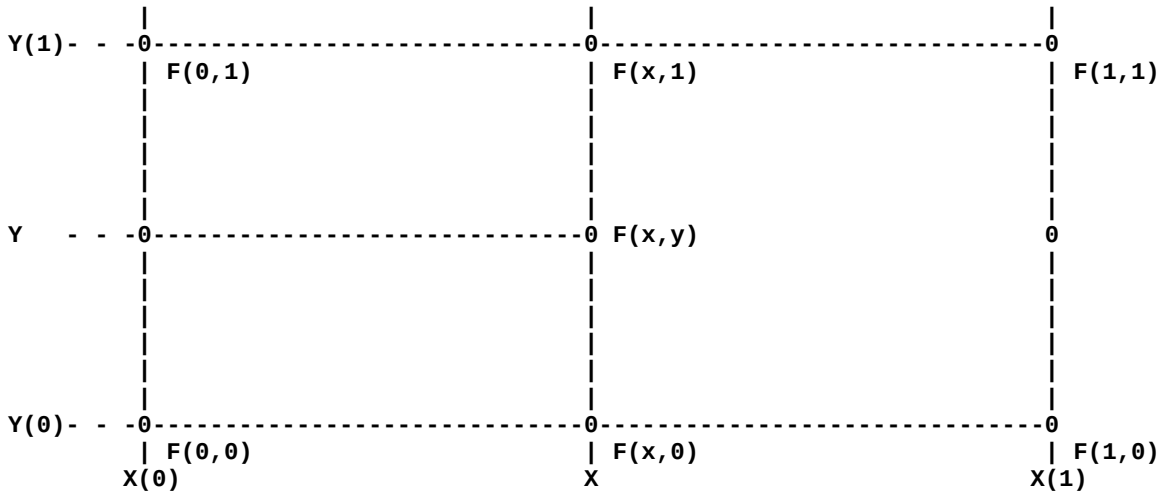
DALIP00 -- Double Analog Linear Interpolation



The Double Analog Linear Interpolation block solves for an output as a function of two input variables (i.e., f(x, y)) by performing a dual linear interpolation calculation based on the analog input variables x_input and y_input. The algorithm interpolates linear segments along two axes (x, y) which are in turn defined by x and y table arrays (x[dimx], y[dimy] of size dimx, dimy. [Size inputs must be positive; as well, table value inputs must be entered in ascending order). These interpolation calculations locate and define a third value that is passed to the output (f_out).

In this manner, the DALIP00 block approximates a continuous (three dimensional) relationship between the x_input and y_input inputs, and the output reference. To perform the interpolation, the block requires at least four known points to be defined; these points are supplied by the f[dimxy] array input. If the x_input and y_input signals exceed the range of the dimx and/or dimy arrays, the output will be clamped to either the first or last value of f[dimxy]. The output reference will be clamped according to f_min or f_max. inputs.

The example below provides a functional example of the double interpolation performed by the DALIP00 block. The module estimates a missing value (F(x,y)) from four (4) known values at neighboring points {F(0,0), F(0,1), F(1,0), F(1,1)}.



First, F(x, 0) is linearly interpolated between F(1, 0) and F(0, 0).

$$F(x,0)=F(0,0)+[\frac{x-X(0)}{X(1)-X(0)}]*[F(1,0)-F(0,0)]$$

Second, F(x, 1) is linearly interpolated between F(1, 1) and F(0, 1).

$$F(x,1) = F(0,1) + [\frac{x - X(0)}{X(1) - X(0)}] * [F(1,1) - F(0,1)]$$

Finally, the linear interpolation between F(x, 0) and F(x, 1) gives F(x, y).

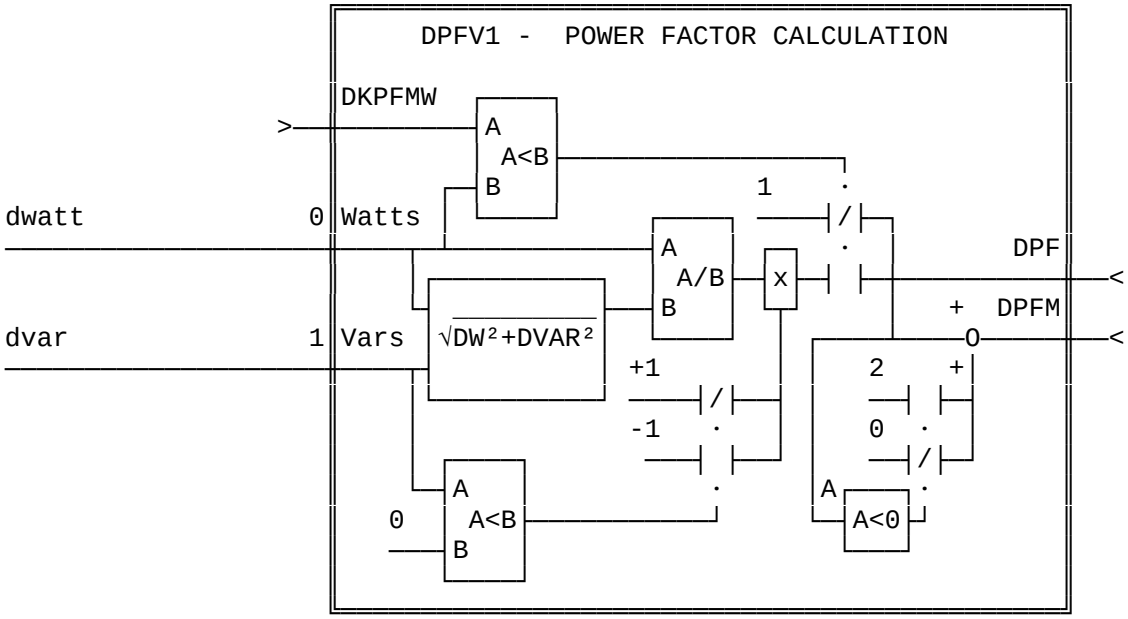
$$F[x,y] = F(x,0) + [\frac{y - Y(0)}{Y(1) - Y(0)}] * [F(x,1) - F(x,0)] =$$

$$F(0,0) + [\frac{x - X(0)}{X(1) - X(0)} * [F(1,0) - F(0,0)]] + [\frac{y - Y(0)}{Y(1) - Y(0)} * [F(0,1) - F(0,0)]]$$

$$[\frac{y - Y(0)}{Y(1) - Y(0)} * \frac{x - X(0)}{X(1) - X(0)} * [F(1,1) - F(0,1) - F(1,0) - F(0,0)]]$$

I/O	Para-meter	Data Type	Description
Inputs	f_max	R4	Analog constant that clamps the maximum value of the output.
	x_input	R4	X input.
	y_input	R4	Y input.
	dimx	F4	X array size.
	dimy	F4	Y array size
	x[dimx]	R4	First signal name (pointer) of the X array.
	y[dimy]	R4	First signal name (pointer) of the Y array.
	f[dimxy]	R4	First signal name (pointer) of the F array defining the output corresponding to the fixed points of x and y arrays. The F array is a one dimensional array ordered as: F(0,0), F(0,1), F(0,2),...F(1,0), F(1,1), F(1,2),….
	f_min	R4	Analog constant that clamps the minimum value of the output.
Outputs	f_out	R4	Result of double linear interpolation calculation.
	x_index	F4	x array index.
	y_index	F4	y array index.

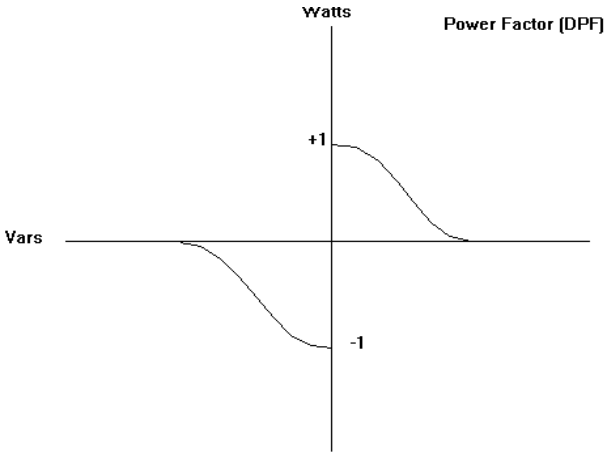
DPFV1 -- Power Factor Calculation

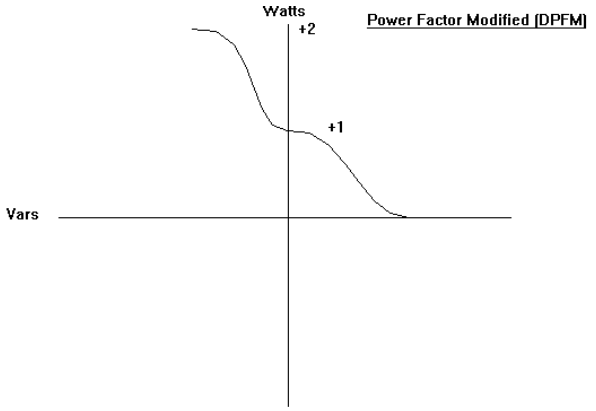


The Power Factor Calculation block executes a function that reads watts, and reactive volt-amperes (vars) calculated from analog inputs and computes the power factor at the point connection. The DPF analog output of the block will remain at 1 until the watt input exceeds the DKPFMW (constant power factor - megawatt) input value. The sign of the output is determined by the dvar input and designates the direction of reactive power flow. This value is positive for the generator supplying vars to the system. Note: when the power factor calculation is negative (A<0), the DPFM (driven power factor modified) output will pass the value in terms of positive numbers; this is accomplished by adding a positive value of two to the power factor number.

$$Powerfactor = \cos\theta = \frac{Watts}{\sqrt{Watts^2 + VARS^2}}$$

I/O	Parameter	Data Type	Description
Inputs	DKPFMW	R4	Power Factor constant that is compared to the watts input. If the watts input is less than this value, the block will pass a value of logic 1 to the output(s).
	dwatt	R4	Analog input that represents the amount of watts being measured.
	dvar	R4	Analog input that represents the amount of vars (volt-ampere reactive) being measured.
Outputs	DPF	R4	Analog value that represents the power factor as calculated from the Watts and Vars analog inputs. The sign of the dpf output is determined by Vars input; an input value greater than 0 will generate a positive output while one that is less than 0 will produce a negative output.
	DPFM	R4	Power Factor Modified: Analog value that represents the power factor in terms of positive numbers.


Watts
Power Factor (DPF)
+1
Vars
-1

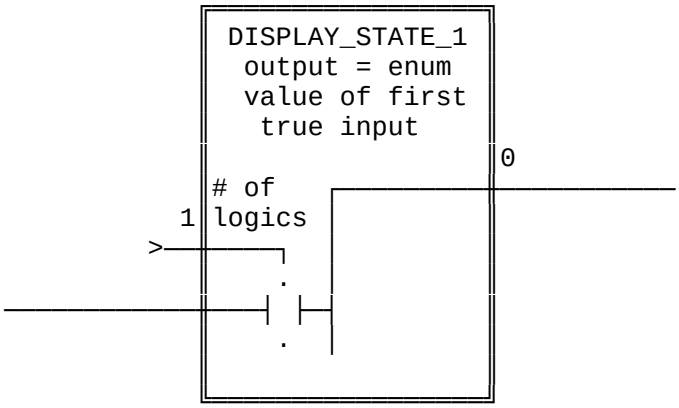

Watts
+2
Power Factor Modified (DPFM)
+1
Vars

DPYSTAT1 -- Display State 1

```
                                DPYSTAT1


input_1   input_2   input_3   input_4   input_5   input_6
input_8   input_9   input_10  input_11  Input_12  input_13
input_15  input_16  input_17  input_18  input_19  input_20
input_22  input_23  input_24  input_25  input_26  input_27
input_29  input_30  input_31  input_32  input_33  input_34
input_36  input_37  input_38  input_39  input_40  input_41
input_43  input_44  input_45  input_46  input_47  input_48
input_50  input_51  input_52  input_53  input_54  input_55
```

The Display State 1 block generates a value for an Enumerated State Variable. This is accomplished by interrogating a list of logic variable inputs (1-56). The first consecutive logic input that reads True will have its corresponding Enumerated State value passed to the output. If none of the logic inputs are True, the enumerated state will read 0. For efficient block operation, only those (consecutive) input logic variables that will be utilized for function definition should be filled in.



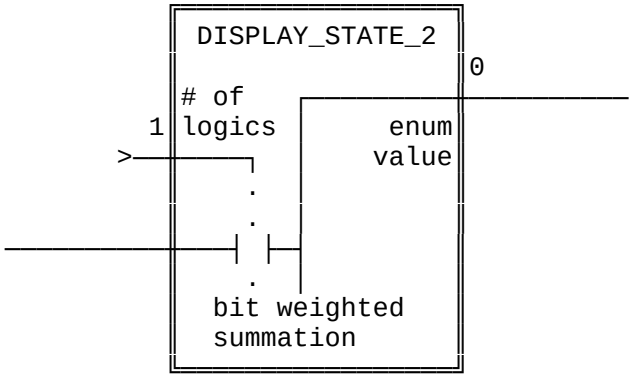
I/O	Parameter	Data Type	Description
Inputs	# of logics	K2	Number of entry sets for DPYSTAT1 This block may be used multiple times within a single Control Sequence Program (max. 56 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry inputs.
	input_n	L1	The DPYSTAT1 block has 56 possible logic inputs that correspond to 56 Enumerated State Variables. The first consecutive logic True input will determine which ESV. is passed to the output.
Outputs	output	S2	Enumerated State Variable whose value is set corresponding to the sequential order number of the first logic True input.

DPYSTAT2 -- Display State 2

DPYSTAT2

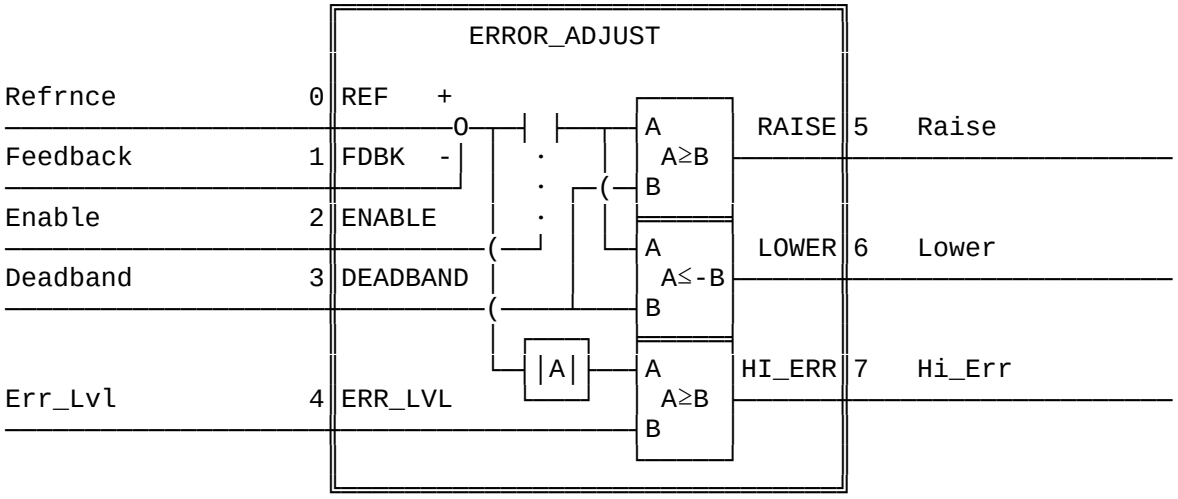
input_1	input_2	input_3	input_4	
input_5	input_6	input_7	input_8	output
input_9	input_10	input_11	input_12	
input_13	input_14	input_15	input_16	

The Display State 2 block generates an Enumerated State Variable and passes that value to the output. This is accomplished by interrogating a list of logic variables (1-16) and setting the enumerated state value equal to the bit weighted summation of the true logic entries (that is, the block is able to generate an enumerated state value that can range from 0 to (2^{15})-1). When the logic True inputs are tallied, the equivalent enumerated state value is passed to the output.



I/O	Parameter	Data Type	Description
Inputs	input_n	L1	Logic inputs. There are 16 possible logic inputs for the Display State block.
	# of logics	K2	Number of entry inputs for DPYSTAT2. This block may be used multiple times within a single Control Sequence Program (max. 16 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry inputs.
Outputs	output	S2	Enumerated State Variable whose value is equal to the weighted bit summation of the logic True inputs.

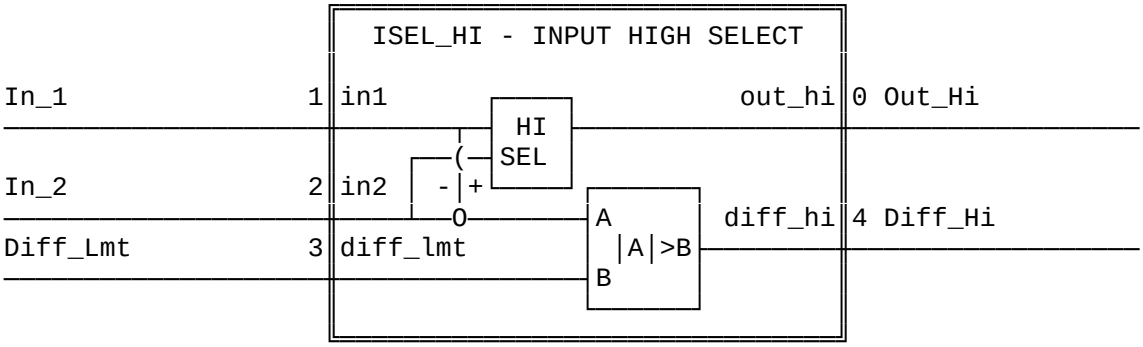
Error Adjust



The Error Adjust block is controlled by an enable logical input; a logic 1 signal on this input permits block execution. The block executes a comparison between a reference value and a feedback value and generates raise and lower logic signals. The value assigned to deadband determines how far the feedback value may deviate from the reference value before a raise or lower signal is generated. When the difference between reference and feedback exceeds the deadband value an output signal is produced. The error level constant defines when a high error signal will be generated. If the absolute difference between reference and feedback exceeds the error level, a logic 1 is passed to the high error output (The value assigned to error level should be greater than the deadband value).

I/O	Parameter	Data Type	Description
Inputs	Refrnce	R4	Analog quantity that represents the desired parameter the block is to maintain with the raise and lower outputs.
	Feedback	R4	The actual value being controlled with the raise and lower outputs.
	Enable	L1	The enable logical input determines whether the block will execute. A 1 permits block execution; a 0 will bypass the block.
	Deadband	R4	Analog constant that determines how far the feedback value may deviate from the Reference value before a Raise or Lower signal is generated.
	Err_Lvl	R4	Analog constant that determines how far the feedback value may deviate from the reference value before an alarm is generated.
Outputs	Raise	L1	Logic signal that is generated when the feedback value drops below the reference minus the deadband.
	Lower	L1	Logic signal that is generated when the Feedback value exceeds the reference plus the deadband.
	Hi_Err	L1	Logic signal that is generated when the absolute difference between reference and feedback exceeds the error Level.

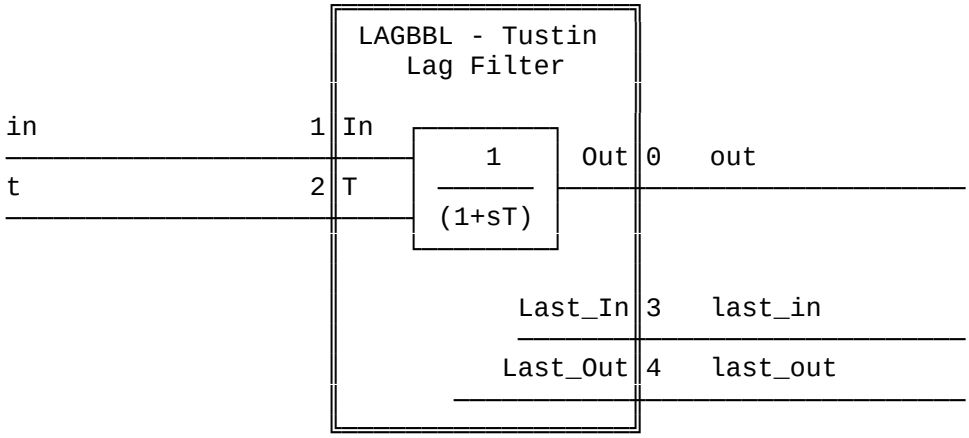
ISEL_HI -- Input High Select



The ISEL_HI High Select block executes a function that reads two inputs (in1, in2), selects the higher of the two, and passes that value as the output. If the difference between these values exceeds the limit specified by the diff_lmt input constant, a diff_hi logic output is generated.

I/O	Para-meter	Data Type	Description
Inputs	In_1	R4	Analog value compared to In_2
	In_2	R4	Analog value compared to In_1.
	Diff_Lmt	R4	Analog limit constant that defines the range of variance that may occur between In_1 and In_2 before a Diff_Hi logic output is generated.
Outputs	Out_Hi	R4	Analog value that represents the higher value between In_1 and In_2.
	Diff_Hi	L1	Logical output that reads 1 when the difference between In_1 and In_2 exceeds the Diff_Lmt constant.

LAGBBL -- Lag

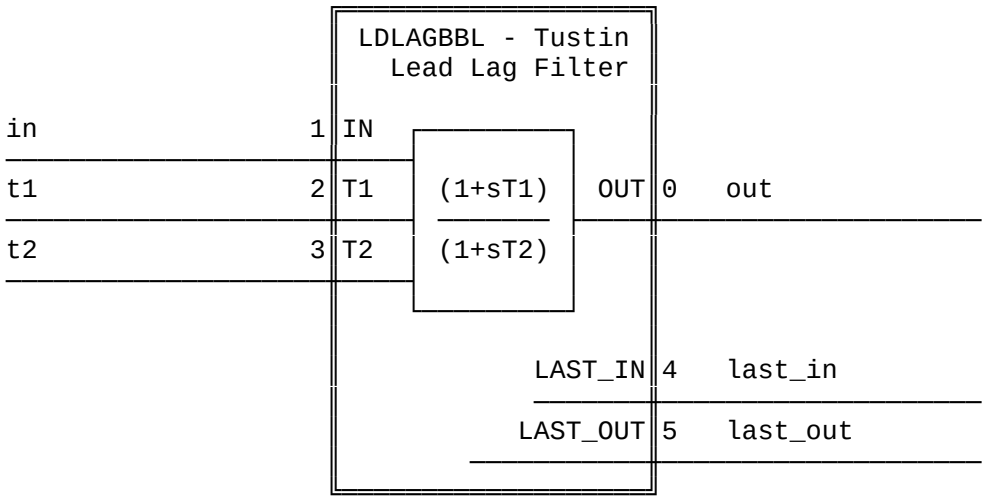


The LAGBBL block executes a (discrete) filter function that approximates a first order lag. The value of the output approaches the value of the input at a rate determined by the Time Constant. The difference between the input and output values represents 100% of the change of the output. The time constant represents the time needed to raise (or lower) the output 63% of the difference between the input and output. Therefore, it takes 5 time constants to change the output approx. 100% of the difference (1 sec.= 63% of 100%, 2nd sec. = 63% of 37%, 3rd sec. = 63% of 13.7%, 4th sec. 63% of 5%, 5th sec. = 63% of 2%). (See example below.)

Damping characteristics of the block will improve for varying analog inputs (in) as the time constant value is increased. The time constant value should be at least four times the sequencing scan interval.

I/O	Parameter	Data Type	Description
Inputs	in	R4	Analog variable is used to calculate the current value of the output.
	t	R4	Analog variable that represents the time needed to raise/lower the outut 63% of the current difference between the input and output.
Outputs	out	R4	Analog variable that is incremented toward the input (in) at a rate determined by the block's time constant (t).
	last_in	R4	Variable that stores the most recent input (in).
	last_in	R4	Variable that stores the last output value.

LDLAGBBL -- Lead Lag



The LDLAGBBL block executes a (discrete) filter function that combines both Lead and Lag compensator characteristics. The properties of the Lead compensator are typified by an output that, with an appropriate time constant (T1), is proportional to the sum of the input signal (in) and its derivative (slope). As the derivative action tends to uncover that part of a signal which is not constant (i.e., time varying.), the Lead compensator, with the appropriate time constant, tends to act similar to a high pass filter (magnitude response) except low frequencies are passed with unity gain, while high frequency components of the input signal are amplified. The resultant phase shift for this type of compensator is typically positive—where the output leads the input.

The Lag portion of the algorithm acts as integrator, ramping the output toward the input at a rate defined by the time constant, T2. Phase response for this compensator is typically characterized by a lagging phase shift, where the output lags the input. The manner in which the LDLAGBBL filter compensates the input signal's phase and magnitude response is contingent on the values supplied for the two time constants (T1, T2).

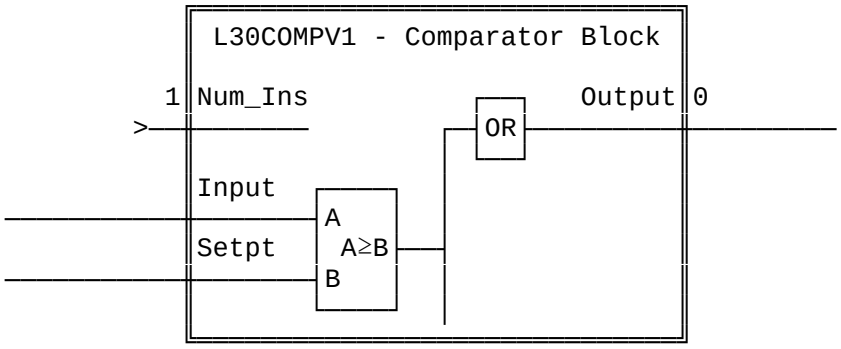
Proper block operation requires a T1 value that is two (minimum) to eight (maximum) times the T2 value; as such, the algorithm will function predominantly as a lead compensator, passing lower frequency components of the input with variable gain, and higher frequency components with amplification equal to the ratio T1/T2. In addition, the T2 constant should be assigned a value that is at least four (4) times the sequencing scan interval.

I/O	Parameter	Data Type	Description
Inputs	in	R4	Analog input variable.
	t1	R4	Analog variable that defines the block's lead compensator characteristics.
	t2	R4	Analog variable that defines the block's lag compensator characteristics.
Outputs	out	R4	Analog variable that is the compensated version of the input.
	last_in	R4	Analog variable that stores the most recent input (in).
	last_out	R4	Analog variable that stores the last output value.

L30COMPV1 -- Comparator Block Signal Level Comparison

```
                                L30COMPV1
                                                                  output
input_1  input_2  input_3  input_4  input_5  input_6  input_7
setpt_1  setpt_2  setpt_3  setpt_4  setpt_5  setpt_6  setpt_7
input_8  input_9  input_10 input_11 input_12 input_13 input_14
setpt_8  setpt_9  setpt_10 setpt_11 setpt_12 setpt_13 setpt_14
input_15 input_16 input_17 input_18 Input_19 input_20 input_21
setpt_15 setpt_16 Setpt_17 setpt_18 setpt_19 setpt_20 setpt_21
input_22 input_23 input_24 input_25 input_26 input_27 input_28
setpt_22 setpt_23 setpt_24 setpt_25 setpt_26 setpt_27 setpt_28
```

The Comparator (1) block executes a comparison function that compares an analog input signal to a corresponding analog setpoint value (Max. 28 pairs). If any of the analog input signals become equal to or exceed a corresponding setpoint value, the logic output is set to 1. Otherwise, the output is set to 0.

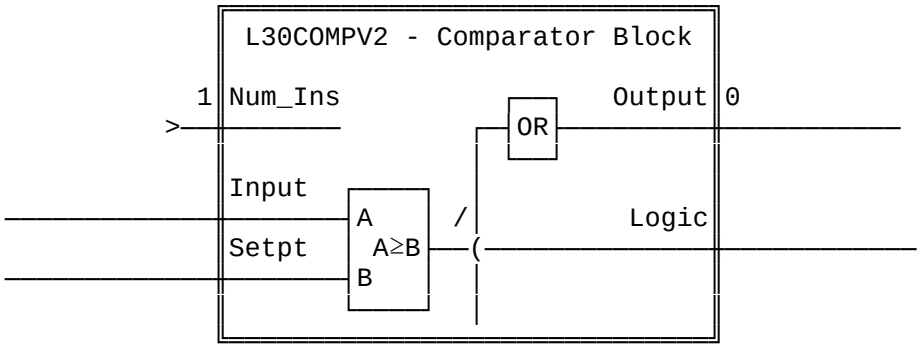


I/O	Para-meter	Data Type	Description
Inputs	input_n	V4	Analog input that is compared to a corresponding setpoint value.
	setpt_n	V4	Analog constant to which a corresponding input is compared.
	Num_Ins	K2	Number of entry sets for L30COMPV1 algorithm. This block may be implemented multiple times within a single Control Sequence Program (max. 28 sets of entries per call of the block.) This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
Outputs	output	L1	Logic output that is set to 1 when any of the analog inputs become equal to or exceed a corresponding setpoint value.

L30COMPV2 -- Comparator Block Signal Level Comparison

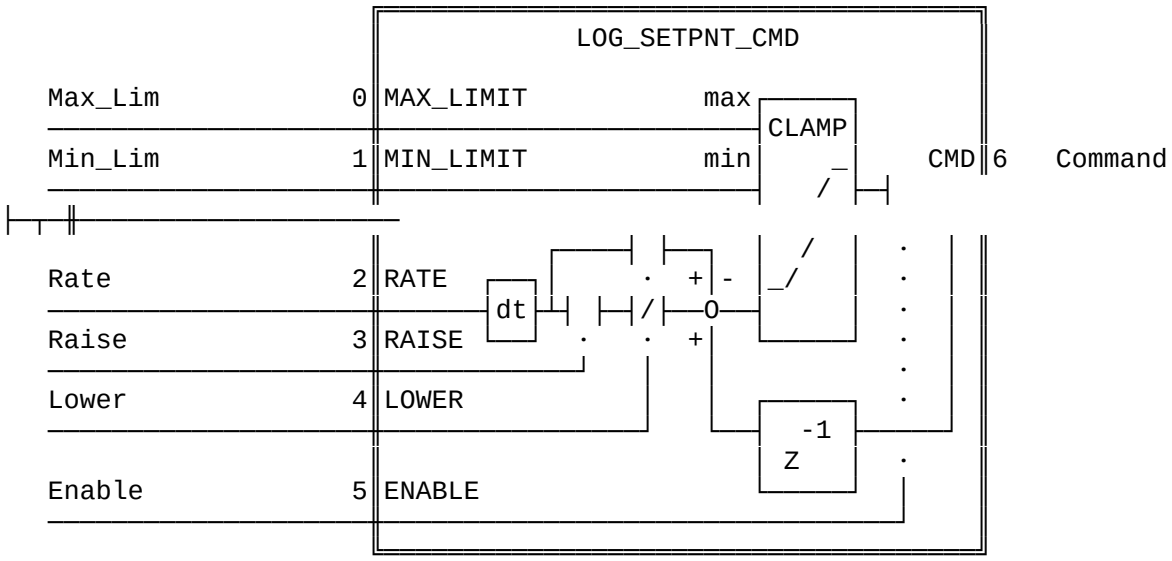
```
                              L30COMPV2
                                                                    Output
input_1  input_2  input_3  input_4  input_5  input_6  input_7
setpt_1  setpt_2  setpt_3  setpt_4  setpt_5  setpt_6  setpt_7
logic_1  logic_2  logic_3  logic_4  logic_5  logic_6  logic_7
input_8  input_9  input_10 input_11 input_12 input_13 input_14
setpt_8  setpt_9  setpt_10 setpt_11 setpt_12 setpt_13 setpt_14
logic_8  logic_9  logic_10 logic_11 logic_12 logic_13 logic_14
input_15 logic_15 input_16 input_17 logic_17 input_18
setpt_15 logic_16 setpt_16 setpt_17 logic_18 setpt_18
```

The Comparator (2) block executes a comparison function that compares an analog input to a corresponding setpoint value (Max. 18 pairs). When an analog input equals or exceeds a corresponding setpoint value, a logic output relating uniquely to that comparison is set to 1. If any comparison generates a discriminate logic 1 signal, the block's logic Output is also set to 1. Otherwise, the logic output is set to 0.



I/O	Parameter	Data Type	Description
Inputs	input_n	V4	Analog input that is compared to a corresponding setpoint value.
	setpt_n	V4	Analog value to which a corresponding analog input is compared.
	Num_Ins	K2	Number of entry sets for L30COMPV2 algorithm. This block may be used multiple times within a single Control Sequence Program (max. 18 sets of entries per call of the block.) This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
Outputs	logic_n	L1	Logic output that specifically corresponds to an analog comparison: will be set to 1 when an analog input equals or exceeds a corresponding setpoint value.
	output	L1	Logic output that is set to 1 when any of the inputs become equal to or exceed a corresponding setpoint value.

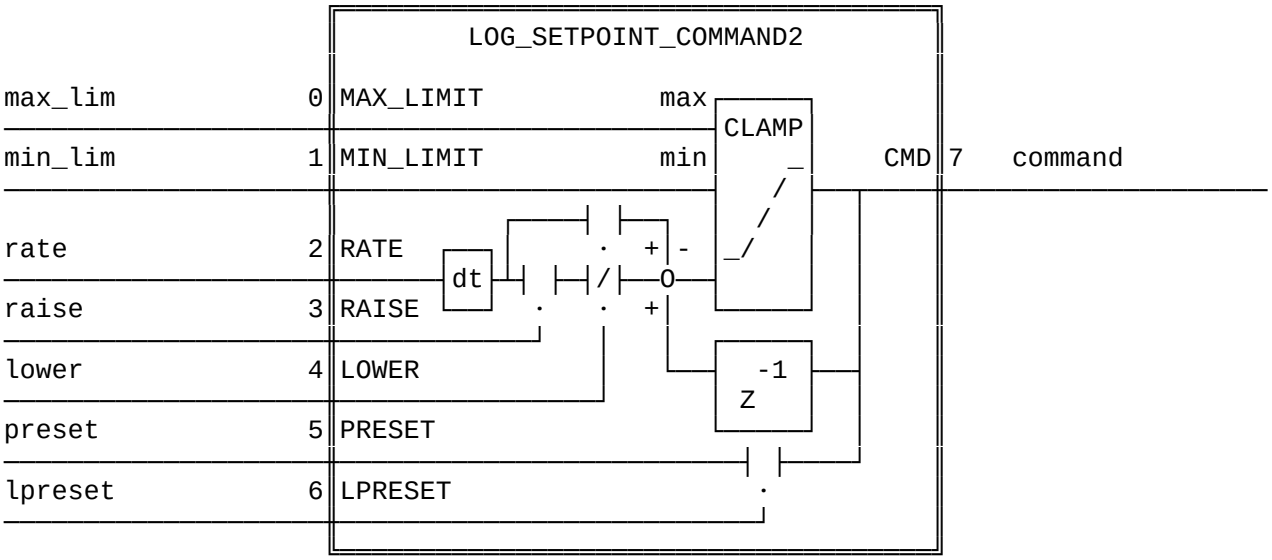
LOG_SETPNT_CMD -- Logic Setpoint Command



Execution of the Logic Setpoint Command block is controlled by the enable input; a logic 1 signal on this input permits block execution. Using logic signals, the Logic Setpoint Command block ramps setpoint commands up and down. The analog inputs Max_Lim and Min_Lim define the range of the command value output. The analog rate input regulates how rapidly the command value is altered within that range. The raise and lower logic inputs determine the positive or negative direction of change. The command output value will continue to increase or decrease until a limit is reached or the raise/lower logic input reading 1 transitions to 0.

I/O	Para-meter	Data Type	Description
Inputs	Max_Lim	R4	Analog input that determines the highest value that can be passed to command output.
	Min_Lim	R4	Analog input that determines the lowest value that can be passed to the command output..
	Rate	R4	Analog input that determines how quickly the command output transitions to a new value.
	Raise	L1	The command output value will increase at the rate value as long as this input reads logic 1, or, until the maximum limit is reached.
	Lower	L1	The command output value will decrease at the rate value as long as this input reads logic 1, or, until the minimum limit is reached.
	Enable	L1	The enable logical input determines whether the block will execute. A 1 permits block execution; a 0 will bypass the block.
Outputs	Com-mand	R4	Analog output value that is modified according to the raise, lower, rate, Min_Lim, and Max_Lim inputs.

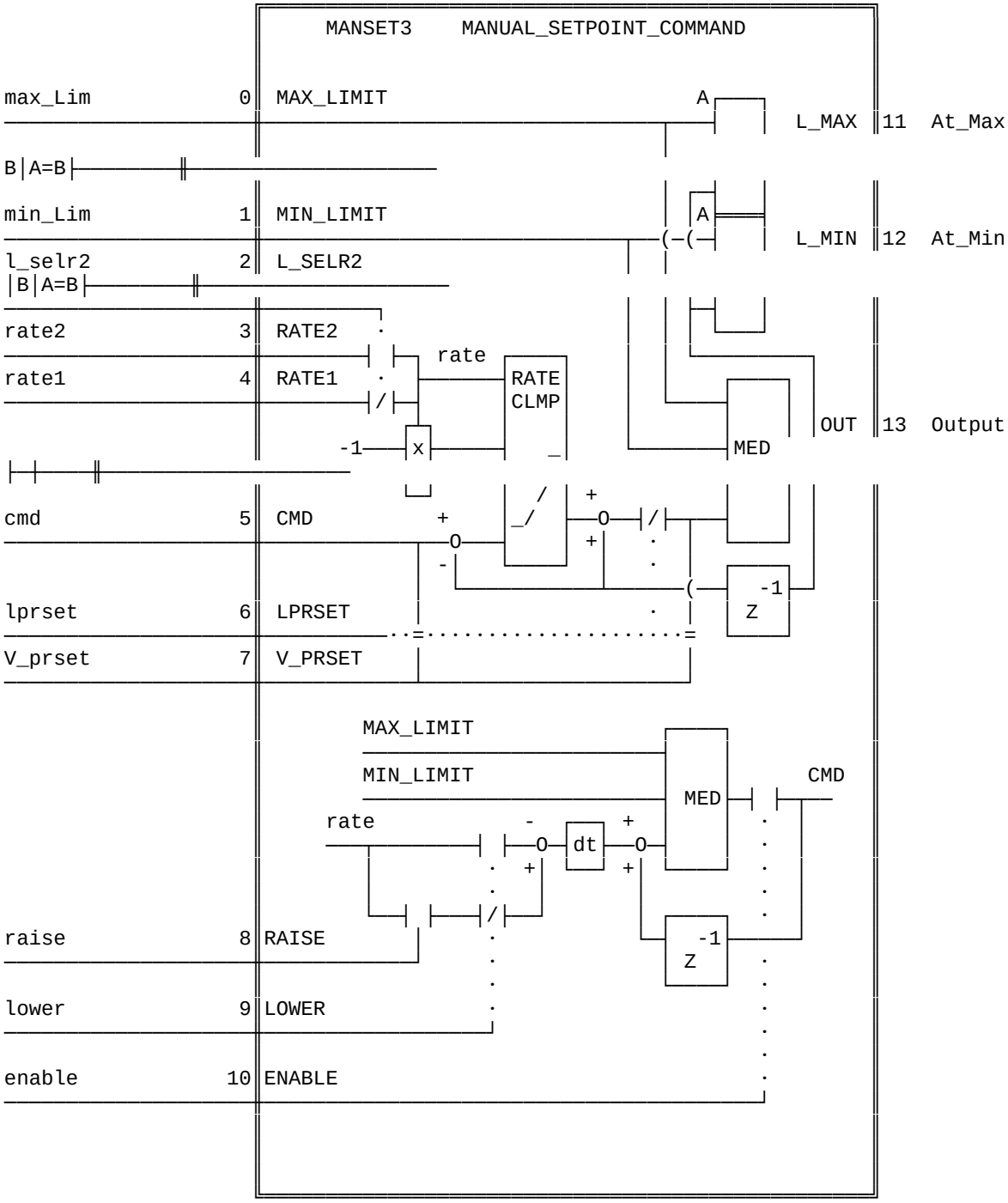
LOG_SETPNT_CMD2 -- Logic Setpoint Command 2



Using logic signals, the Logical Setpoint Command (2) block ramps setpoint commands up and down. The analog inputs max_lim and min_lim define the range of the command value output. The analog rate input regulates how rapidly the command value is altered within that range. The raise and lower logic inputs determine the positive or negative direction of change. The command output value will continue to increase or decrease until a limit is reached or the raise/lower logic input reading 1 transitions to 0. If the lpreset input reads logic 1, the block will not execute the ramping function, but will pass the Preset value to the output.

I/O	Parameter	Data Type	Description
Inputs	max_lim	R4	Analog input that determines the highest value that can be passed to command output.
	min_lim	R4	Analog input that determines the lowest value that can be passed to the command output.
	rate	R4	Analog input that determines how quickly the command output transitions to a new value.
	raise	L1	The command output value will increase at the rate value as long as this input reads logic 1, or, until the maximum limit is reached.
	lower	L1	The command output value will decrease at the rate value as long as this input reads logic 1, or, until the minimum limit is reached.
	preset	R4	Analog value that is passed to the output when the lpreset input reads logic 1.
	lpreset	L1	A logic 1 from the lpreset input will cause the the preset value to be passed to the output.
Outputs	command	R4	Analog output value that is modified according to the raise, lower, rate, min_lim, and max_lim inputs.

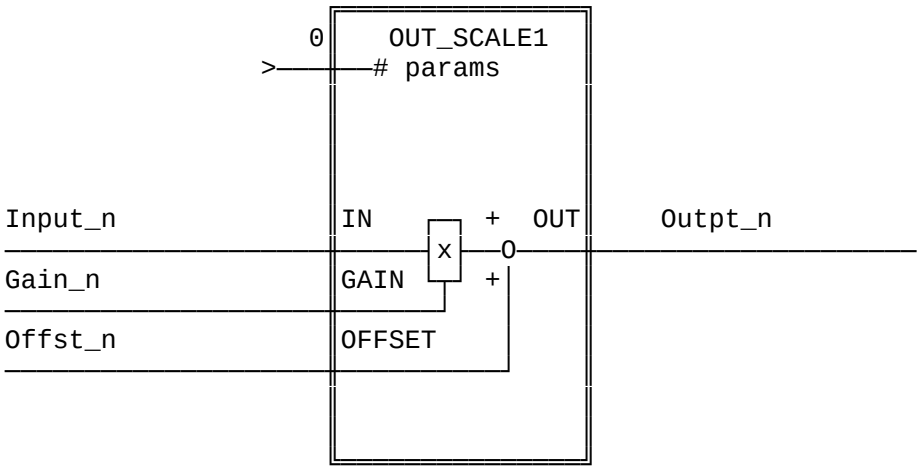
MANSET3 -- Manual Setpoint Command



The Manual Setpoint block ramps the analog output up or down until it equals the analog command input value. The analog inputs max_Lim and min_Lim define the range of adjustment for the output. The rate at which the adjustment is implemented is determined by the analog inputs rate1 and rate2. The block will alter the output value according to the analog rate1 input until the 1_selr2 logic input reads true. At this point, the value is adjusted according to the rate2 schedule. When the output reaches a value equal to the maximum or minimum range limits, the logic outputs At_Max or At_Min are set to 1 respectively. These outputs will remain set to logic 0 until a limit is reached. If the block receives a logic 1 lprset signal, the command input and the output are immediately adjusted to the V_prset analog value (subject to limits max_Lim and min_Lim).

I/O	Parameter	Data Type	Description
Inputs	max_Lim	R4	Analog input that determines the highest value the output can be adjusted to.
	min_Lim	R4	Analog input that determines the lowest value the output can be adjusted to.
	rate1	R4	Analog input that determines how quickly the output is raised or lowered to command input value.
	l_selr2	L1	A logic 1 on this input will instruct the block to adjust the output according to rate2 schedule.
	rate2	R4	Analog input that determines how quickly the output is raised or lowered to the command input value when the l_selr2 rate input reads 1.
	cmd	R4	Analog input that the output will be adjusted to. If this value exceeds the maximum or minimum range limits of the block, the output will be set to the limit that is applicable.
	l_prset	L1	Logic input that enables the v_prset value to be passed immediately to the output subject to the block's min. and max. limits.
	V_prset	R4	Analog value that is passed directly to the output when the l_prset logic input is a 1. (This value is subject to the algorithm's min. and max. limits.
Outputs	At_Max	L1	Logical output that is set to 1 when the output value equals the maximum limit value.
	At_Min	L1	Logical output that is set to 1 when the output value equals the minimum limit value.
	Output	F2	Analog value that is adjusted to reflect the current command input value.

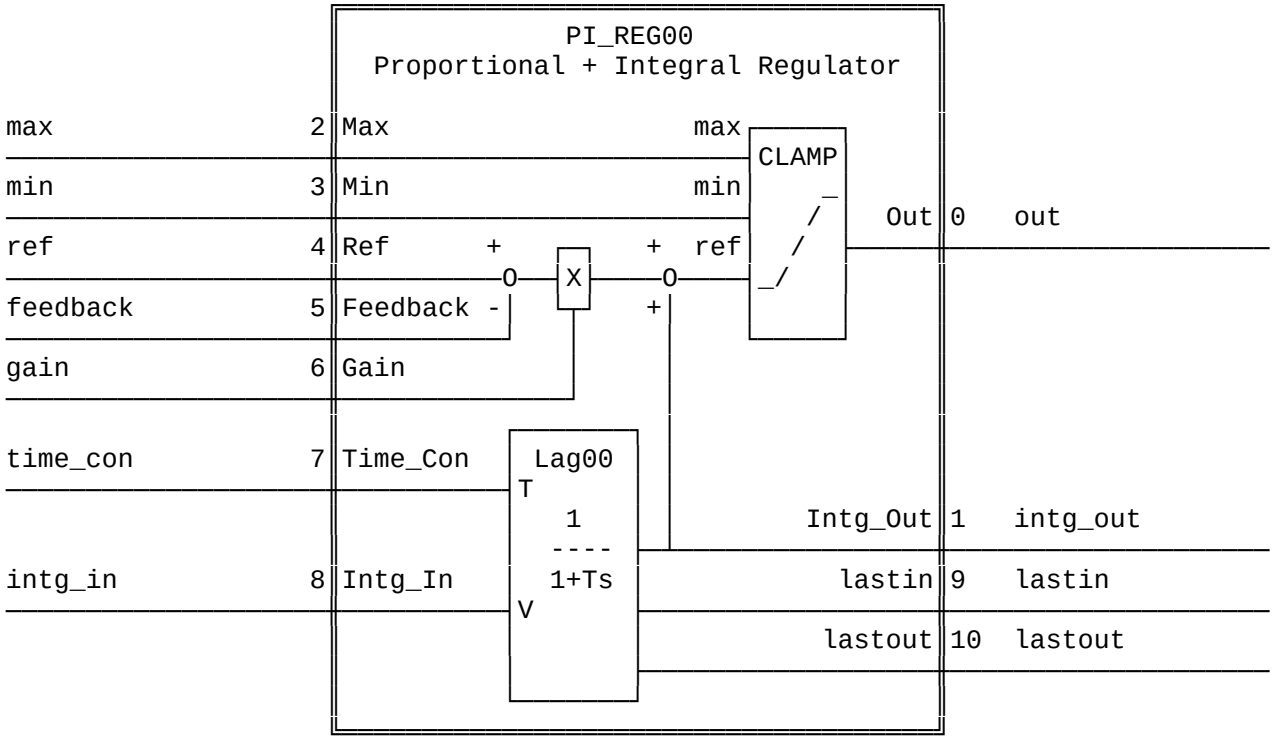
OUT_SCALE1 -- Scaling Module for Outputs



The Scaling Module for Outputs (Out_Scale1) block applies gains and offsets to a variable number of signals. The input value is first multiplied by the gain and then the offset is applied to produce the output.

I/O	Para-meter	Data Type	Description
Inputs	# params	K2	Number of entry sets for OUT_SCALE1 algorithm. This block may be used multiple times within a single Control Sequence Program (max. 12 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
	Input_n	R4	Analog input value.
	Gain_n	R4	Analog gain value.
	Offst_nl	R4	Analog gain value.
Outputs	output_n	R4	Analog output value.

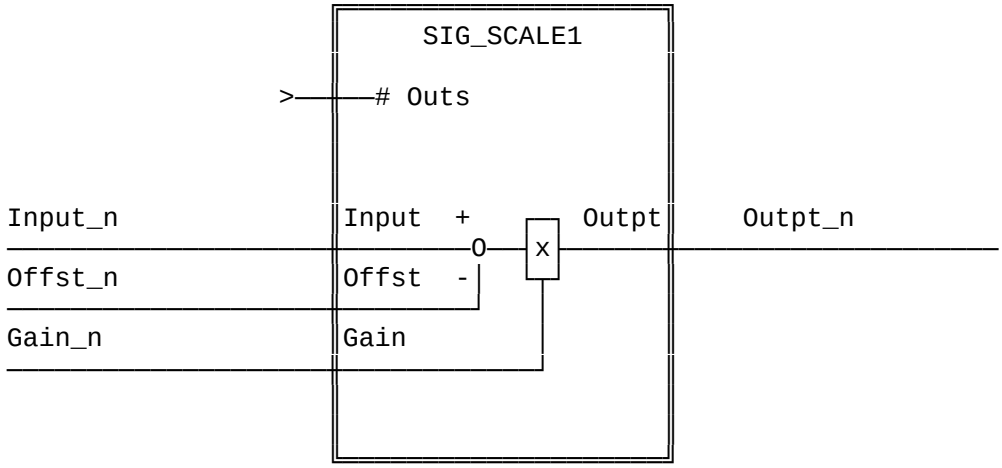
PI_REG00 -- Proportional + Integral Regulator



The PI_REG00 block executes a function that increments the output (out) toward a reference (ref) at a rate determined by proportional and integral calculations. Initially, the proportional action is performed by subtracting a feedback value from the reference. The difference (error) is then multiplied by a gain. The block's integral action is defined by the integral time constant (time_con); this value is expressed in seconds. (Note: the time constant value should be at least four times the sequencing scan interval). The output of the integrator is added to the result of the proportional calculation. This value is clamped according to the min and max inputs before being passed to the output (out).

I/O	Parameter	Data Type	Description
Inputs	max	R4	Analog value that defines the maximum value that can be passed to the output (out).
	min	R4	Analog value that defines the minimum value that can be passed to the output (out).
	ref	R4	Input value from which the feedback signal is subtracted.
	feedback	R4	Analog input that provides the device's current position.
	gain	R4	Constant input that is multiplied by the difference between the reference (ref) and the feedback values.
	time_con	R4	Constant that defines the integral time constant.
	intg_in	R4	Analog input upon which the integral action is performed.
Outputs	out	R4	Logical output that is set to 1 when the output value equals the maximum limit value.
	intg_out	R4	Logical output that is set to 1 when the output value equals the minimum limit value.

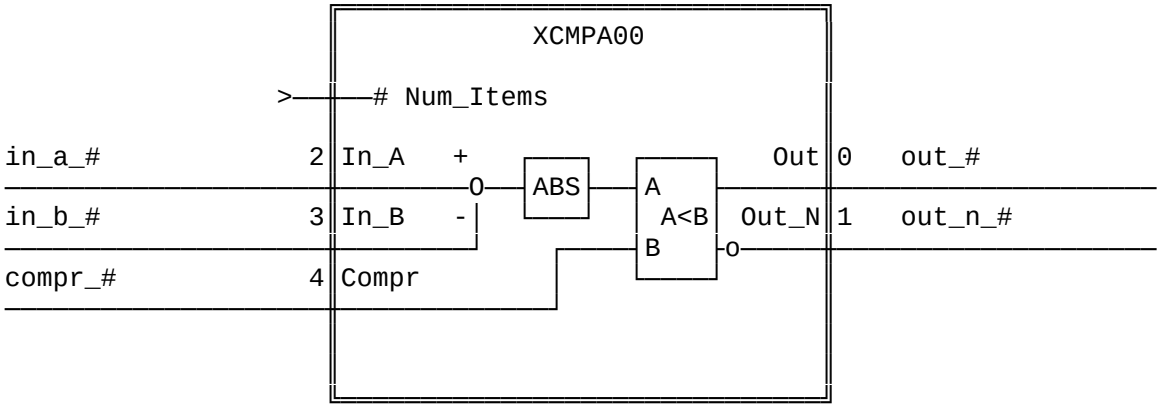
SIG_SCALE1 -- Signal Scaling



The Signal Scaling (Sig_Scale1) block applies offsets and gains to a variable number of signals. The offset value is first subtracted from the input value, and then the result is multiplied by the gain to produce the output.

I/O	Parameter	Data Type	Description
Inputs	Input_n	R4	Analog input value.
	Gain_n	R4	Analog gain value.
	Offst_n	R4	Analog offset value.
	# outs	K2	Number of entry sets for SIG_SCALE1 algorithm. This block may be used multiple times within a single Control Sequence Program (max. 12 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
Outputs	Outpt_n	R4	Analog output value.

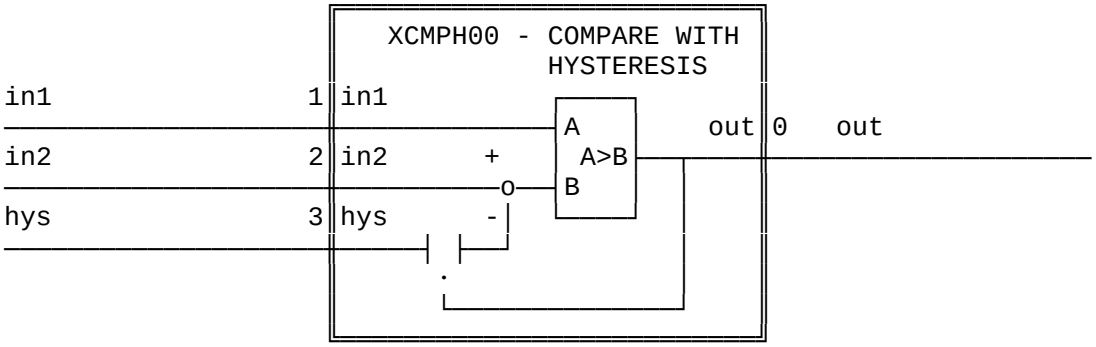
XCMPA00 -- Compare Absolute Value



The XCMPA00 block executes a function that writes to two logic outputs (out, out_N) based upon a comparison between an input signal (compr) and the absolute value (ABS) of the difference between two analog values (in_a, in_b). If the (absolute) differential value is less than the input value, the out and out_N outputs will be set to true and false respectively; and a differential value that is greater than the cmpr input will cause the logic states of the two outputs to be reversed.

I/O	Parameter	Data Type	Description
Inputs	# Num_ items	R4	Number of entry sets for XCMP00 algorithm. This block may be used multiple times within a single Control Sequence Program (max. 12 sets of entries per call of the block). This value does not require a value to be assigned. The value will be assigned by the sequencing compiler based on the number of entry sets.
	in_a_#	R4	Analog variable from which the analog variable in_b_# is subtracted.
	in_b_#	R4	Analog variable that is subtracted from the in_a_# analog variable.
	compr_#	R4	Analog value that is compared to the absolute difference between inputs in_a_# and in_b_#.
Outputs	out_#	L1	Logic output that is set true when the absolute difference between in_a_# and in_b_# is less than the compr_# input constant.
	out_n_#	L1	Logic output that is set true when the absolute difference between in_a_# and in_b_# inputs is greater than the compr_# input constant.

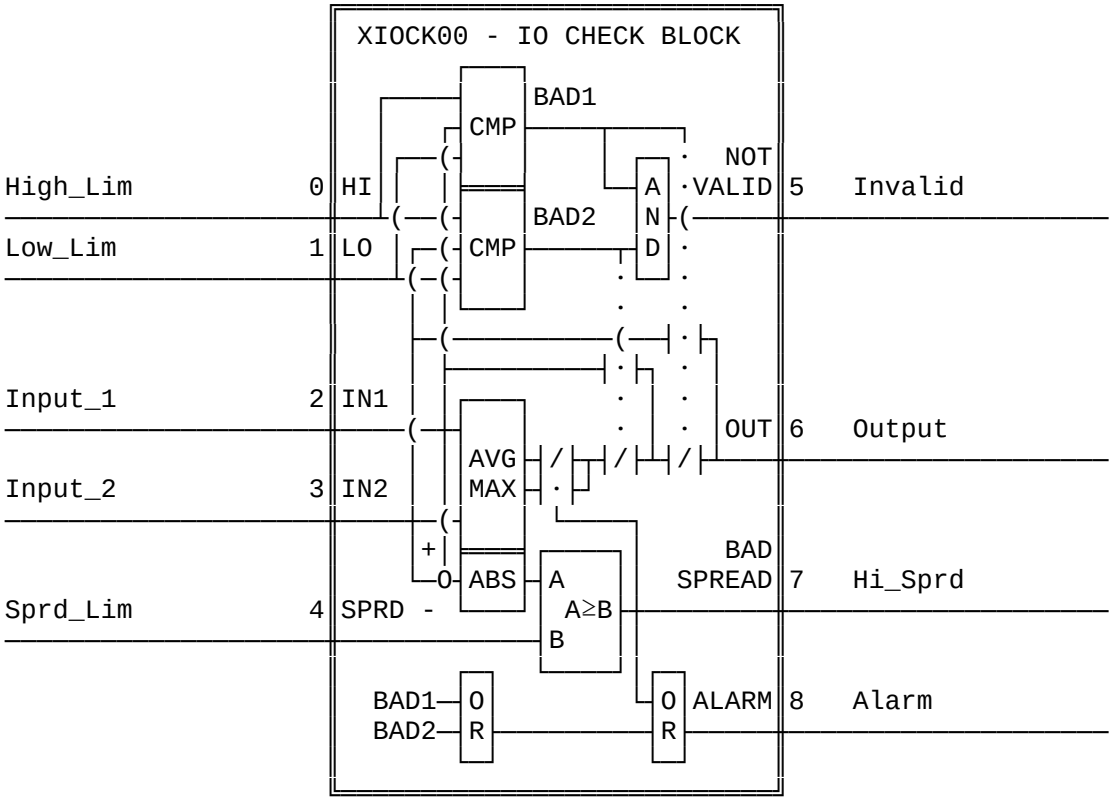
XCMPH00 -- Compare with Hysteresis



The XCMPH00 block executes a function that writes a logic signal output when input A (in1) exceeds input B (in2). When this occurs, the hysteresis is enabled and the hys value is subtracted from the in2 input. This operation effetively lowers the set-point value the input must drop below before the output will reset to logic 0.

I/O	Parameter	Data Type	Description
Inputs	in1	R4	Analog variable that is compared to in2. If in1 exceeds in2, the ouput will be set.
	in2	R4	Analog variable that is subtracted from the in_a.
	hys	R4	Analog variable that is subtracted from the in_a.
Outputs	out	L1	Logic output that is set true when in1 exceeds in2.

XIOCK00 -- Dual-Input Check Block

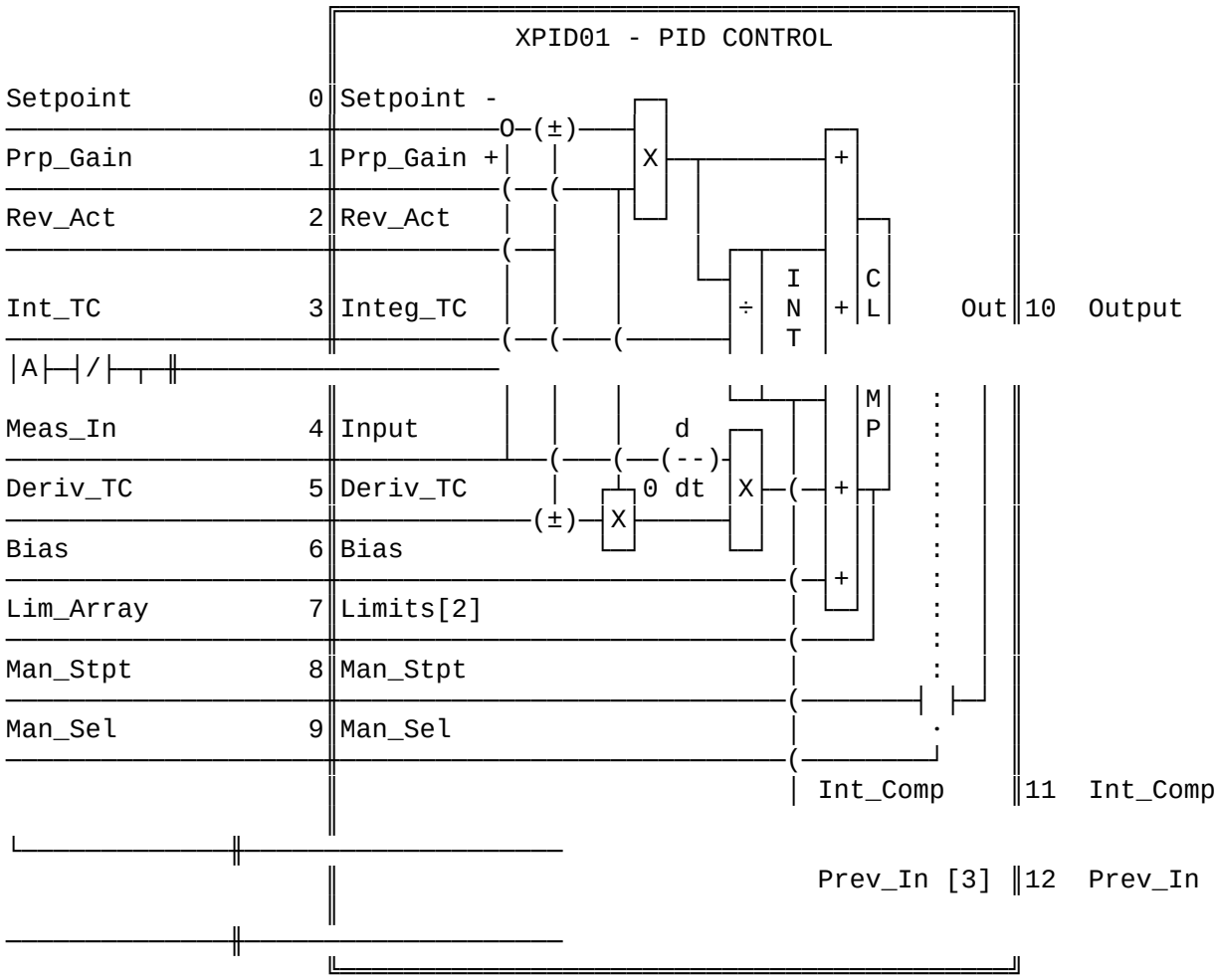


The Dual Input Check block (XIOXCK00) executes a function that compares a pair of analog (typically thermocouple) inputs against each other and high and low analog limit constants. The spread limit analog constant determines the amount of variance that can occur between the two input values before a logic 1 is passed to the high spread output (typically this value will be less than high and low limit inputs). If the inputs are within the spread limit and do not exceed either high or low limits, the block will pass the **average** of the input values as the output.

When the input values exceed the spread limit but remain within the high and low limits, the higher of the two values is passed to the output: should a single input value exceed a limit, the concurring value is passed. A condition where both inputs exceed the limit values will cause a logic 1 invalid output to be passed. If an input value exceeds any of the limits expressed above, an alarm output signal is generated.

I/O	Para-meter	Data Type	Description
Inputs	High_Lim	R4	Analog constant that determines the maximum value an input can reach before an alarm output is generated.
	Low_Lim	R4	Analog constant that determines the minimum value an input can reach before an alarm output is generated.
	Input_1	R4	The first of a pair of analog input values that are compared against each other and the high and low limit constants.
	Input_2	R4	The second of a pair of analog input values that are compared against each other and the high and low limit constants.
	Sprd_Lim	R4	Analog constant value that determines the degree to which the two input values can vary before a hi_sprd logic output is generated.
Outputs	Invalid	L1	Logical output that reads 1 when both inputs exceed a high or low limit.
	Output	R4	Analog value that expresses one of three conditions: an average of the two inputs, a single input if a corresponding input exceeds a high or low limit, or, the greater of the two input values if the spread limit has been exceeded but the high or low limits have not.
	Hi_Sprd	L1	Logical output that reads 1 when the variance between the inputs exceeds the sprd_lim value.
	Alarm	L1	Logical output that reads 1 when any of the block limits are exceeded by an input value.

XPID01 -- Proportional Integral Derivative Block



The Proportional Integral Derivative (PID) control block (XPID01) executes a function that reads analog feedback information (Meas_In), and according to the mode selected (manual, auto), produces an output that controls the process being monitored. When the Man_Sel logic input reads one, the block transitions to a manual procedure that causes the manual setpoint (Man_Stpt) value to be passed directly to the output (this value is passed regardless of the limits stipulated in the limit array (Lim_Array). If the Man_Sel reads 0, the block will perform a PID operation that sets the output according to a summation of Proportional, Integral, and Derivative compensations, and a bias value. Unlike the manual select mode, the auto mode output is clamped between the minimum and maximum limits stored in the limit array (Lim_Array).

The Proportional action of the block is defined by the gain (Prp_Gain). This action is equal to error (measured value - setpoint) * Prp_Gain. A logic FALSE Rev_Act input will cause an increasing output for a positive or negative error; a logic TRUE Rev_Act input will cause a decreasing output for a positive or negative error.

The amount of integral action is defined by the integral time constant (Int_TC). This value and the derivative time constant are both expressed in seconds; the value of each time constant should be at least four (4) times the sequencing scan interval at which the block is executed. The integrator is clamped so as to remain within the limits -- it will not wind up (continue to max. value) when the output is saturated. If the output is saturated high or low, the integrator will not increase or decrease respectively. When a saturation occurs, an inverse value (+ -) increment is added to the

integrator. When the output is saturated low, the integrator will not decrease; an increment will be added to the integrator only if it is negative. If the integral time constant is set to 0 the integrator will also be 0 and the integral action will be disabled.

The value of the integrator is saved for use in the next sample. If the block is in manual mode, and the Int_TC is not set to 0, the integrator will be modified to cause the automatic control to track the manual setpoint (i.e. Int_Comp = Man_Stpt - (P+D+B). The automatic control will track Man_Stpt only to the minimum and maximum. Under these conditions, transfer from manual to automatic mode is bumpless if the manual setpoint remains within the automatic mode limits.

The amount of Derivative action is defined by the derivative time constant and is expressed in seconds. It has been designed to operate on the measured input value rather then the error so that there will not be a spike in the output if there is a step function in the setpoint. The previous three measured input values are stored in the 3 element array Prev_In. The block takes the derivative of the proportional section using techniques that minimize noise. If Deriv_TC is set to 0 the derivative action is also logic 0. The storage of the previous measured inputs continues so that a valid change in measured value will be obtained immediately if Deriv_TC is changed from 0 to non-0. The bias is added directly to the proportional + integral + derivative actions before the output clipping takes place.

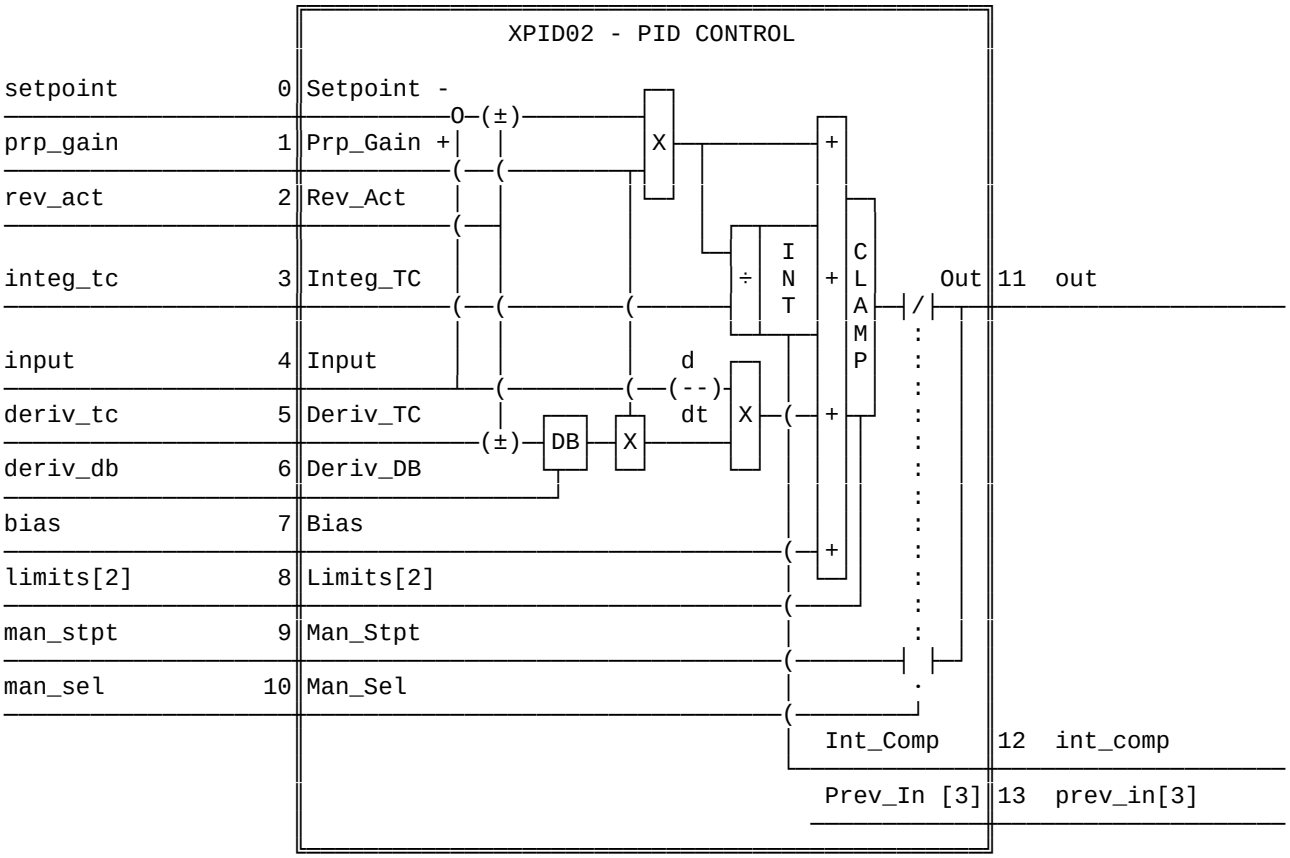
PID loop transfer function uses the following equation:

$$Output(s) = (-Setpoint + Meas\_in)(s) * [Prp\_Gain\ (1 + \frac{1}{Int\_TC(s)} + Deriv\_TC(s))]$$

Where (s) is the LaPlace transform function. Further information can be obtained from the factory, if necessary.

I/O	Parameter	Data Type	Description
Inputs	Setpoint	R4	Analog value that represents the nominal value the block maintains when in Auto mode.
	Prp_Gain	R4	Analog value that defines proportional action.
	Rev_Act	L1	A logic 1 on this input causes a decrease in the output value while a 0 produces an increase.
	Int_TC	R4	Integral time constant; defines the integral action of the block. Expressed in seconds.
	Meas_In	R4	Analog input that represents the feedback value.
	Deriv_TC	R4	Analog constant that defines derivative action of the block. Expressed in seconds.
	Bias	R4	Analog constant that is added to the sum of proportional, integral, and derivative values.
	Lim_Array	R4	Two element array that contains minimum and maximum output limits. The first element is the minimum limit, and the second element is the maximum limit.
	Man_Stpt	R4	Analog value that is passed directly to the output when the Man_Sel input reads 1.
	Man_Sel	L1	Logic input that determines if the Man_Stpt value is passed to the output. If this input reads 0, the output will equal the sum of the proportional, integral, and derivative actions, and the bias value.
Outputs	Output	R4	Analog value that represents either the Man_Stpt value (Man_Sel 1), or, the sum of the proportional, integral, and derivative actions, and the bias value (Man_Sel 0).
	Int_Comp	R4	Analog variable that stores the incremental change and accumulative total of integral action.
	Prev_In	R4	3 element array containing the three previous measured values.

XPID02 -- Proportional Integral Derivative Block (Ver. 02)



The Proportional Integral Derivative (PID) control block (XPID02) executes a function that reads analog feedback information (input), and according to the mode selected (manual, auto), produces an output that controls the process being monitored. When the manual selection logic input reads one, the block transitions to a manual procedure that causes the manual setpoint value to be passed directly to the output (this value is passed regardless of the min. and max. limits stipulated in the input limit array. If the manual selection logic reads 0, the block will perform a PID operation that sets the output according to a summation of proportional, integral, and derivative compensations, and a bias value. Unlike the manual select mode, the auto mode output is clamped between the minimum and maximum limits stored in the limit array.

The proportional action of the block is defined by the input gain. This action is equal to error (measured value - setpoint) * gain. A logic FALSE reverse acting input will cause an increasing output for a positive or negative error; a logic true reverse acting input will cause a decreasing output for a positive or negative error.

The amount of integral action is defined by the integral time constant. This value and the derivative time constant are both expressed in seconds; the value of the time constant should be at least four (4) times the sequencing scan interval at which the block is executed. The integrator is clamped so as to remain within the minimum and maximum limits stipulated by the limits input-- it will not wind up (continue to maximum value) when the output is saturated. If the output is saturated high or low, the integrator will not increase or decrease respectively. When a saturation occurs, an inverse value (+ -) increment is added to the integrator. When the output is saturated

low, the integrator will not decrease; an increment will be added to the integrator only if it is negative. If the integral time constant is set to 0 the integrator will also be 0 and the integral action will be disabled.

The value of the integrator is saved for use in the next sample. If the block is in manual mode, and the integral time constant is not set to 0, the integrator will be modified to cause the automatic control to track the manual setpoint (i.e. I = manual setpoint - (P+D+B). The automatic control will track the manual setpoint only to the min and max limits. Under these conditions, transfer from manual to automatic mode is bumpless if the manual setpoint remains within the automatic mode limits.

The amount of Derivative action is defined by the derivative time constant and is expressed in seconds. It has been designed to operate on the input rather then the error so that there will not be a spike in the output if there is a step function in the setpoint. In addition, the block permits a deadband to be introduced to the derivative operation to minimize noise. Three previous three input values are stored in the 3 element array. The block takes the derivative of the proportional section using techniques that minimize noise. If the derivative time constant is set to 0 the derivative action is also 0. The storage of the previous measured input continues so that a valid change in measured value will be obtained immediately if the derivative time constant is changed from 0 to non-0. The bias is added directly to the proportional + integral + derivative actions before the output clipping takes place.

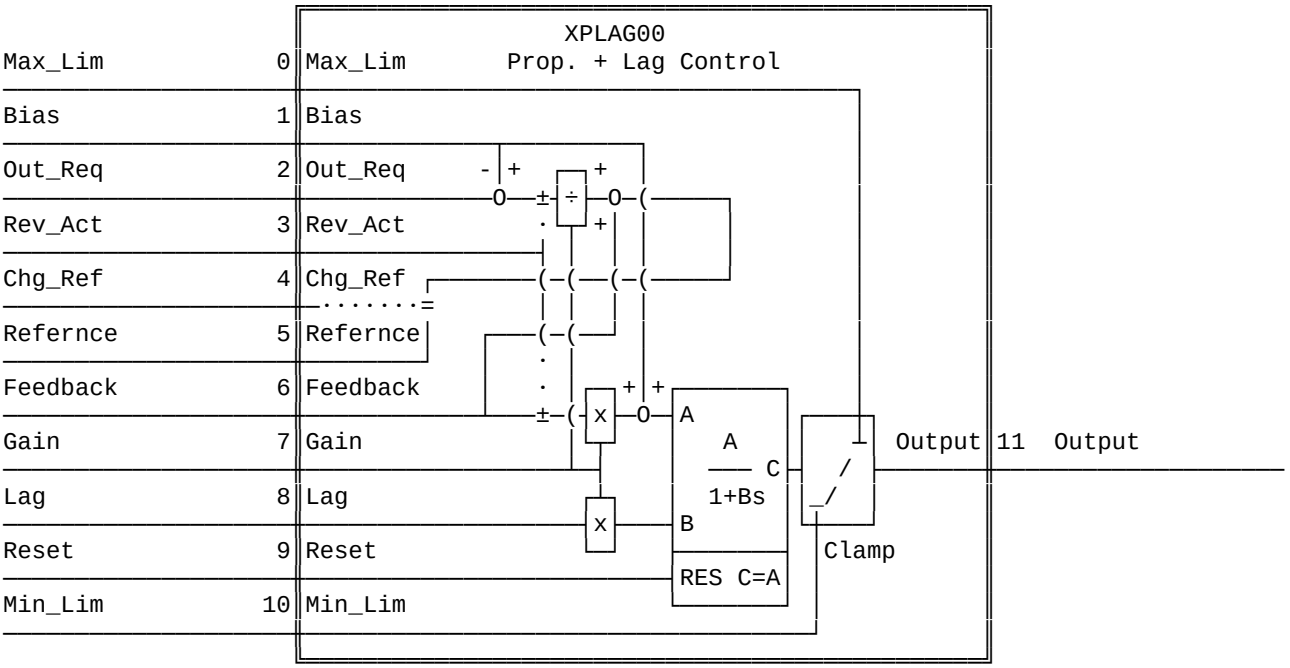
PID loop transfer function uses the following equation:

$$Output(s) = (-Setpoint + Meas\_in)(s) * [Prp\_Gain\ (1 + \frac{1}{Int\_TC(s)} + Deriv\_TC(s))]$$

Where (s) is the LaPlace transform function. Further information can be obtained from the factory, if necessary.

I/O	Para-meter	Data Type	Description
Inputs	Setpoint	R4	Analog value that represents the nominal value the block maintains when in Auto mode. Should be scaled in percent.
	prp_gain	R4	Analog value that defines proportional action. Should be scaled in percent.
	rev_act	L1	A logic 1 on this input causes a decrease in the output value while a 0 produces an increase.
	integ_tc	R4	Integral time constant; defines the integral action of the block. Expressed in seconds.
	input	R4	Analog input that represents the feedback value. Should be scaled in percent.
	deriv_tc	R4	Analog constant that defines derivative action of the block. Expressed in seconds.
	deriv_db	R4	Analog constant that is added to the sum of proportional, integral, and derivative values. Should be scaled in percent.
	bias	R4	Analog constant that is added to the sum of proportional, integral, and derivative values. Should be scaled in percent.
	limits[2]	R4	Two element array that contains minimum and maximum output limits. The first element is the minimum limit, and the second element is the maximum limit. Both should be scaled in percent.
	man_stpt	R4	Analog value that is passed directly to the output when the man_sel input reads 1. Should be scaled in percent.
	man_sel	L1	Logic input that determines if the man_stpt value is passed to the output. If this input reads 0, the output will equal the sum of the proportional, integral, and derivative actions, and the bias value.
Outputs	out	R4	Analog value that represents either the man_stpt value (man_sel 1), or, the sum of the proportional, integral, and derivative actions, and the bias value (man_sel 0). Should be scaled in percent.
	int_comp	R4	Double word variable that stores the incremental change and accumulative total of integral action. Should be scaled in percent.
	prev_In	R4	3 element array containing the three previous measured values. Should be scaled in percent.

XPLAG00 -- Proportional Plus Lag Control (Ver. 00)

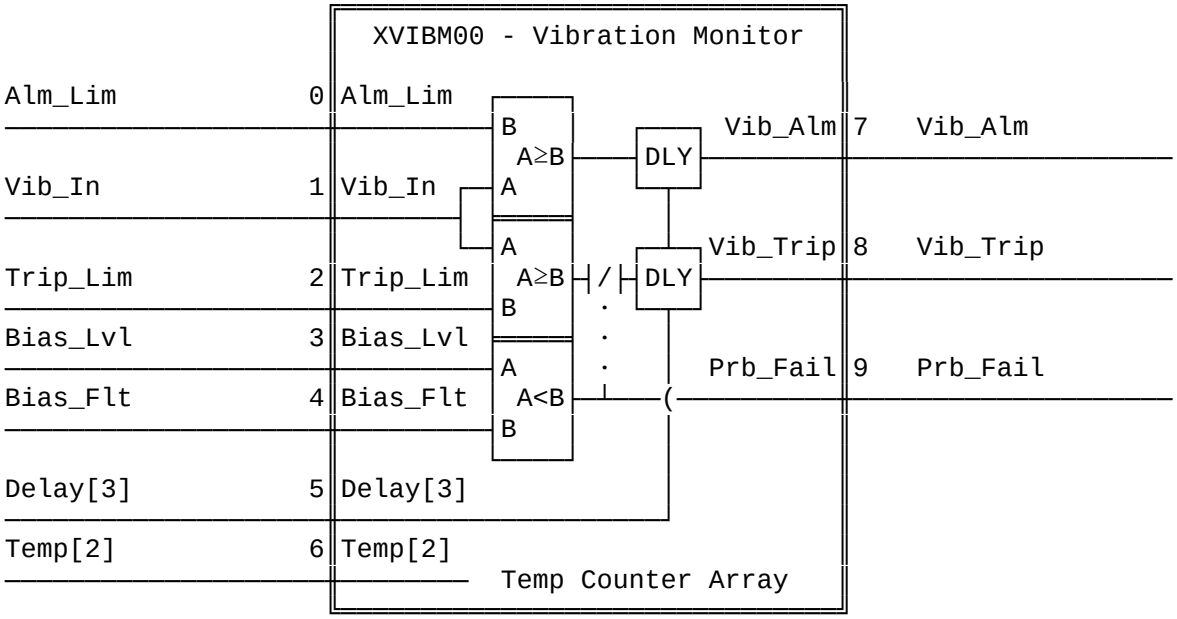


When the change reference input reads false, the Proportional Plus Lag (Ver 00) block implements a function that adjusts the analog output to reflect the analog reference value according to the proportional action over a period of time specified by the lag constant. The block begins by reading the analog feedback value and subtracting it from analog reference co
nstant; this operation generates an error value. The error is multiplied by the gain constant to define the block's proportional action.

For system tuning purposes, the XPLAG block multiplies the gain by the time (lag) constant. This functionality allows the gain to be adjusted without changing the crossover frequency (gain = 1). Note 1: An extremely high gain value will in effect cause the block to simply execute an integral function. Note 2: A logic 1 reset input will disable the time Lag function of the block. The positive or negative control action of the block is defined by the reverse action input. A logic TRUE on this input causes the sign of the output to reflect the sign of the error value while a FALSE reading will produce a signed output that is the inverse of the error value. When the logic input change reference is TRUE, the reference value is updated based on the requested output value, and the output will equal the requested output value. Note: If the output reaches a value equal to either the maximum or minimum limit constants, it is clamped to that respective value.

I/O	Para-meter	Data Type	Description
Inputs	Max_Lim	R4	Analog constant that determines the highest value the output can be adjusted to.
	Min_Lim	R4	Analog constant that determines the lowest value the output can be adjusted to.
	Bias	R4	Analog constant added to the error value after it has been multiplied by the gain.
	Out_Req	R4	Analog value that the output will reflect when the Chg_Ref input reads True.
	Rev_Act	L1	Logical input that determines the positive or negative action of the block. A logic TRUE implements an increasing action while a FALSE signal effects the reverse.
	Chg_Ref	L1	A logic TRUE Chg_Ref input will cause the reference value to be updated (based on the Out_Req) and the Output to be altered to equal the Out_Req value.
	Refernce	R4	Analog value from which the error and proportional action are derived.
	Feedback	R4	Analog input that is subtracted from the reference value to generate an error value.
	gain	R4	Analog constant that is multiplied by the error value in order to define proportional action of the block.
	lag	R4	Analog constant that determines the amount of time it will take the block to implement a new Output.
	reset	L1	A logic 1 on this input will cause the lag function to be disabled.
Outputs	Output	R4	Analog value that is adjusted according to proportional action over a period of time specified by the time lag constant.

XVIBM00 -- Vibration Monitor

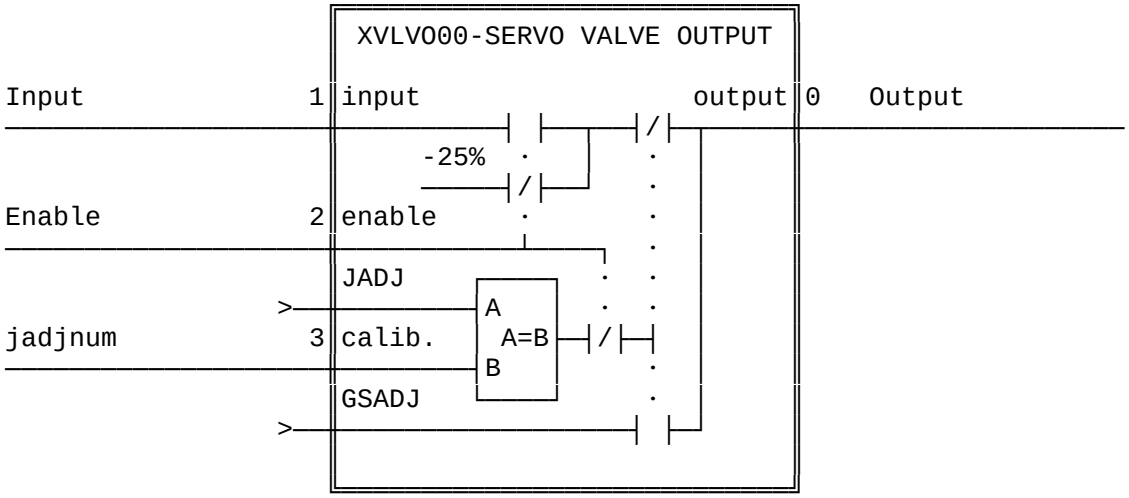


The Vibration Monitor block reads analog vibration and logical probe failure inputs. The vibration-input value is compared to the alarm limit and trip limit analog constants to determine whether they equal or exceed them. When the vibration input value equals or exceeds either of these constants for a period of time specified by a respective delay[3] constant value (alarm, trip), a logic 1 is passed to a corresponding output. The alarm and trip time constants are saved in the temp[2] temporary storage location. These values are replaced by the probe delay constant if the block receives a logic 1 on the probe fail input. This replacement will continue until the probe fail input transitions back to 0.

If the vibration input value is still above either the alarm or trip limits when the transition occurs, the corresponding counter in memory will begin counting down from the probe delay value. The probe delay constant is normally larger than the alarm or trip delay values and should allow time for the vibration signal to return to a nominal level. If the vibration remains equal to or above an alarm or trip limit after the probe delay time period has run down, the corresponding delay constant is reinstated in memory and begins to be counted down. If that time allotment runs out, a logic 1 is passed to the corresponding output.

I/O	Para-meter	Data Type	Description
Inputs	Vib_In	R4	Analog value that is compared to the alarm and trip inputs.
	Alm_Lim	R4	Analog constant that represents the maximum value the vibration input may reach before a logic 1 is passed to the alarm output.
	Trip_Lim	R4	Analog constant that represents the maximum value the vibration input may reach before a logic 1 is passed to the trip output.
	Prb_Fail	L1	Logic input that reads 1 when a probe failure occurs.
	Delay[3]	F4	Analog inputs (alarm, trip, probe fail) that determine the amount of time an alarm state is allowed to exist before corresponding alarm is generated.
Outputs	Temp[2]	F4	Temporary storage location where alarm and trip delay values are saved. If the probe fail input reads 1, these values are replaced by the probe fail delay value.
	Vib_Alm	L1	Logic output that reads 1 when the vibration value exceeds the alarm limit for longer than the period of time specified by the vibration alarm delay constant.
	Vib_Trip	L1	Logic output that reads 1 when the vibration value exceeds the trip limit for longer than the period of time specified by the vibration trip delay constant.

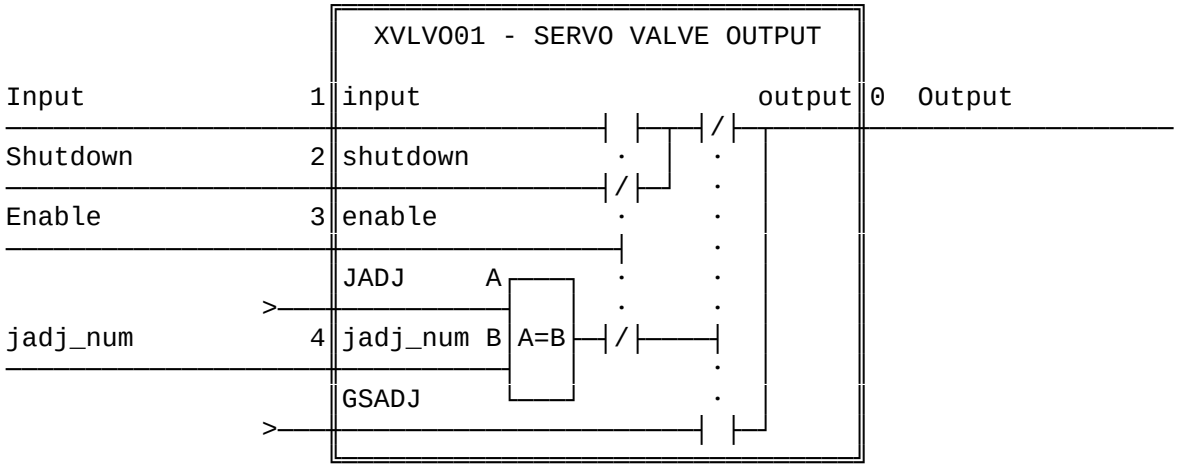
XVLVO00 -- Valve Output Block



The XVLV00 Servo Valve Output block executes a function that passes analog valve control information. If the enable input reads 0, the block will direct the valve to maintain a -25% bias. When this input reads logic 1 the input reference data is passed directly to the output. A logic 0 enable input will also permit the block to execute a manual output for calibration, if required. Once enabled, the block will output the value GSADJ for calibration, when it receives JADJ and calibration inputs that match (A=B). Respectively, these values represent system variables and calibration points that correspond to specific valves. When a match occurs, the GSADJ valve adjust input value is passed directly to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	Logic input that allows the block to pass Input information or execute a calibration function.
	Input	R4	Analog value that represents a valve reference position.
	jadjnum	F4	Analog system variable that corresponds to a specific valve.
Outputs	Output	R4	Analog servo valve reference point command.

XVLVO01 -- Valve Output Block



The XVLVO01 Servo Valve Output block executes a function that passes analog valve control information. If the enable input reads 0, the block will pass to the valve the shutdown analog value (unlike XVLVO00, this function permits customization of the valve "shutdown" bias). When this input reads 1, input reference data is passed directly to the output. A logic 1 enable input permits the block to execute a manual output for calibration if required. The block will output the value GSADJ for calibration when it receives JADJ and calibration inputs that match (A=B). Respectively, these values represent system variables and calibration points that correspond to specific valves. When a match occurs, the GSADJ valve adjust input value is passed directly to the output.

I/O	Parameter	Data Type	Description
Inputs	Enable	L1	Logic input that allows the block to pass Input information or execute a calibration function.
	Input	R4	Analog value that represents a valve reference position.
	jadjnum	F4	Analog system variable that corresponds to a specific valve.
	Shutdown	R4	Analog constant value that will be passed to the valve when the enable input reads 0.
Outputs	Output	R4	Analog servo valve reference point command.

Appendix G I/O Configurator Screens

Introduction

This appendix uses `Courier` font to show the screens as they appear in the I/O Configurator. **`Bold type`** highlights data entry fields. *`Italics`* such as *`(1)`* refer to notes in the text below the screen. They do not appear on the actual screen.

Caution

The values on the screen are examples only and may not be the same in an operating system.

Do not use these values in an actual site I/O Configuration.

This appendix is presented as follows:

I/O Cross-Reference

The tables below map the various I/O channels from their hardware signal names in F:\UNITn\IO.ASG to the applicable I/O Configurator screens and signal flow diagrams.

Milliamp Outputs

Quantity	IO.ASG hardware signal names	IO Configurator screen	Signal Flow Diagram
2	Q1_MAO_REF1…2	R1 TCQA screen 2	Figure D-21
2	Q1_MAO_REF3…4	R1 TCQE screen 5	Figure D-7
2	Q2_MAO_REF1…2	R2 TCQA screen 2	Figure D-21
2	Q3_MAO_REF1…2	R3 TCQA screen 2	Figure D-21
16	R5_MAO_REF01…16	none, not configurable	Figure D-36

Voltage Inputs

Quantity	IO.ASG hardware signal names	IO Configurator screen	Signal Flow Diagram
4	Q1TCQA_V dc1…4	R1 TCQA screen 3	Figure D-25
4	Q3TCQA_V dc1…4	R3 TCQA screen 3	Figure D-25

Thermocouples

Quantity	IO.ASG hardware signal names	IO Configurator screen	Signal Flow Diagram
15	Q1_TCQA_TC01…15	R1 TCQA screen 4	Figure D-17
15	Q2_TCQA_TC01…15	R2 TCQA screen 4	Figure D-17
15	Q3_TCQA_TC01…15	R3 TCQA screen 4	Figure D-17
42	R5TCCA_TC01…42	R5 TCCA screen 2	Figure D-30,31,32

Pulse Rate Inputs

Quantity	IO.ASG Hardware Signal Names	IO ConfiguratorScreen	Signal Flow Diagram
2	Q1STCA_FRQ05…06	R1 STCA screen 2	Figure D-19
1	Q1STCA_FRQ07	R1 STCA screen 2	Figure D-26
2	Q1TCQA_FREQ1…2	R1 TCQA screens 5-6	Figures D-19,48
		R1 TCEA-X screen 4	
		R1 TCEA-Y screen 4	
2	Q1TCQA_FREQ3…4	R1 TCQA screen 5	Figure D-19
2	Q1TCQE_FREQ1…2	R1 TCQE screen 7	Figures D-5,48
		R1 TCEA-X screens 5-6	
		R1 TCEA-Y screens 5-6	
2	Q1TCQE_FREQ3…4	R1 TCQE screen 7	Figure D-5

Pulse Rate Inputs — Coninued

4	Q1UCPB_FRQ08…11	R1 UCPB screen 3	Figure D-20
2	Q2STCA_FRQ05…06	R2 STCA screen 2	Figure D-19
4	Q2TCQA_FREQ1…4	R2 TCQA screen 5	Figure D-19
2	Q2UCPB_FRQ08…09	R2 UCPB screen 3	Figure D-20
2	Q3STCA_FRQ05…06	R3 STCA screen 2	Figure D-19
1	Q3STCA_FRQ07	R3 STCA screen 2	Figure D-26
4	Q3TCQA_FREQ1…4	R3 TCQA screen 5	Figure D-19
4	Q3UCPB_FRQ08…11	R3 UCPB screen 3	Figure D-20
2	none	R1 TCEA-Z screens 4-6	Figure D-48

Seismic (Velocity) Vibration Inputs

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
12	Q1TCQA_VIB01…12	R1 TCQA screen 7	Figure D-24
12	Q3TCQA_VIB01…12	R3 TCQA screen 7	Figure D-24

Milliamp Inputs

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
15	Q1TCQA_MAI01…15	R1 TCQA screens 8-9	Figure D-12
15	Q2TCQA_MAI01…15	R2 TCQA screens 8-9	Figure D-12
15	Q3TCQA_MAI01…15	R3 TCQA screens 8-9	Figure D-12
14	R5TCCA_MAI01…14	R5 TCCA screens 4-5	Figure D-27
22	R5TCCB_MAI01…22	R5 TCCB screens 3-5	Figure D-28
1	Q1STCA_MAI17	R1 STCA screen 3	Figure D-26
1	Q3STCA_MAI17	R3 STCA screen 3	Figure D-26

Proximity Sensors

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
8	Q1TCQE_VPRX1…8, Q1TCQE_PRX01…08	R1 TCQE screens 2-3	Figure D-9
2	Q1TCQE_PRX09…10	R1 TCQE screen 4	Figure D-10
1	Q1TCQE_PRX11	R1 TCQE screen 4	Figure D-11

Accelerometers:

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
3	Q1TCQE_HPVB1…3, Q1TCQE_IPVB1…3, Q1TCQE_LPVB1…3	R1 TCQE screens 6,2	Figure D-8

RTDs

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
4	Q1TCQE_RTD01…04	R1 TCQE screen 8	Figure D-4
30	R5TCCA_RTD01…30	R5 TCCA screen 3	Figures D-33,34
14	R5TCCB_RTD01…14	R5 TCCB screen 2	Figure D-35

Contact Inputs

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
96	Q11_CI01…96	R1 TCDA screens 2-3	Figures D-41,42
96	R51_CI01…96	R5 TCDA screens 2-3	Figures D-41,42

Megawatt Inputs

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
1	Q1UCPB_MAI16	R1 UCPB screen 2	Figure D-18
1	Q2UCPB_MAI16	R2 UCPB screen 2	Figure D-18
1	Q3UCPB_MAI16	R3 UCPB screen 2	Figure D-18

Flame Detectors

Quantity	IO.ASG Hardware Signal Names	IO Configurator Screen	Signal Flow Diagram
8	L28FDA…H	TCEA-X screen 3, TCEA-Y screen 3, TCEA-Z screen 3	Figure D-49

I/O Board Arrangement

The I/O configuration screens are arranged within the I/O Configurator in this hierarchy:

Core	I/O Board
R1	STCA
	UCPB
	TCQA
	TCQE
	TCDA
	TCEA-X
	TCEA-Y
	TCEA-Z
R2, R3	STCA
	UCPB
	TCQA
R2, R3	STCA
	UCPB
	TCQA
R5	STCA
	UCPB
	TCCA
	TCCB
	TCDA

Each I/O board shown has several associated screens. These screens are duplicated if the I/O board is used more than once in the controller.

The following sections show the sample screens for each I/O board type, with a description of the screen following.

Note Numbers in the format (1) are used as callouts on the sample screen. The description for that callout is below the screen.

TCQA

The TCQA board is a multifunctional board located in the <R1>, <R2>, and <R3> cores in location two. The TCQA board defines the following functions:

- Position mA (mA) outputs
- Voltage inputs
- Thermocouple inputs
- Pulse rate inputs
- Vibration inputs
- Milliamp inputs
- Vibration circuit diagnostics
- Bus undervoltage and ground monitoring

For more information on the above subjects, see Chapters 6 and 7.

```
                TCQA Board Definition - Socket 1 - Screen 1/10


                    EPROM Revision Information:

                         Major Rev:   B (1)

                         Minor Rev:   B (1)
```

(1) These are the major and minor revision levels for the EPROM on the board. These should match the label on the EPROM and the information in F:\UNITn\PANEL.CFG.

```
                TCQA Board Definition - Socket 1 - Screen 2/10

                    Position Milli-Amp Output Configuration

Milli-Amp Output 1:

   Output used (enables output and basic diagn.):             NO (1)
   Current suicide enable (YES for TMR, NO for Simplex):      NO (2)
   CDB variable full scale value:       128 (3)
   Minimum ( 4 mA/ 40 mA) CDB value:    0.0 (4)
   Maximum (20 mA/200 mA) CDB value:    100.0 (4)


Milli-Amp Output 2:

   Output used (enables output and basic diagn.):             NO
   Current suicide enable (YES for TMR, NO for Simplex):      NO
   CDB variable full scale value:       128
   Minimum ( 4 mA/ 40 mA) CDB value:    0.0
   Maximum (20 mA/200 mA) CDB value:    100.0
```

This screen configures two mA output channels that land on the TBQC terminal board as shown in signal diagram D-21. Hardware signal names are Qn_MAO_REF1…2. These channels typically drive control devices. Jumpers on the TBQC terminal board select the maximum current output range of either 20 mA or 200 mA.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) Setting this to YES enables a suicide function in which the output current is forced to zero if actual output differs from the reference by 25% of full scale. Recommended setting: NO.

(3) This is the full scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an output current that is too low or too high, usually by some power of 2.

(4) These are the control signal values corresponding to the minimum and maximum signal currents. For numerical reasons, if the maximum and minimum have the same sign, their ratio (max/min) must be greater than 1.61 or less than 0.11.

```
            TCQA Board Definition - Socket 1 - Screen 3/10

                          Voltage Input


                    Signal      Full Scale    Min (0v)     Max (10v)
                    in use      CDB value     CDB value    CDB value
                    -------     ----------    ---------    ---------
Signal  1:             NO (1)      2048 (2)      0.0 (3)      500.0 (3)
Signal  2:             NO          128           0.0          100.0

Signal  3:             NO          128           0.0          100.0
Signal  4:             NO          128           0.0          100.0
```

This screen applies to the <R1> and <R3> cores only. The <R2> screen has no purpose. This screen configures 4 voltage/current inputs that land on the TBQB terminal board as shown in signal diagram D-25. Hardware signal names in IO.ASG are QnTCQA_V dc1…4. Hardware jumpers on the TBQB terminal board select the voltage or current option. Note that the TCQA board in <R1> is connected to the TBQB board in <R2>, while the TCQA board in <R3> is connected to the TBQB board in <R3>.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) This is the full scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an input value that is too low or too high, usually by some power of 2.

(3) These are the control signal values corresponding to the minimum and maximum signal levels.

```
            TCQA Board Definition - Socket 1 - Screen 4/10

                 Thermocouple Type Selection


TC  1:  - (1)     TC  5:  -         TC  9:   -         TC 13:   K
TC  2:  -         TC  6:  -         TC 10:   -         TC 14:   -
TC  3:  -         TC  7:  -         TC 11:   -         TC 15:   -
TC  4:  -         TC  8:  -         TC 12:   K

       Valid types:    K, J, E, T, - (not used)


Cold Junction Out of Range Detection Enable:       YES (2)
Value returned when Cold Junction is Out of Range: 100.0  °C (3)
```

This screen configures 15 thermocouple channels on the TCQA board. The <R1>, <R2>, and <R3> channels all land on the <R1> TBQA terminal board as shown in signal diagram D-17. Hardware signal names in IO.ASG are Qn_TCQA_TC01…15.

(1) This sets the type of thermocouple connected. If not used (-), there will be no associated diagnostic alarms.

(2) Setting this to YES enables failure detection of the cold junction circuitry.

(3) This is the value use for the cold junction temperature in case a circuit failure is detected. This is typically set to 100 ºC to make the failure obvious.

```
              TCQA Board Definition - Socket 1 - Screen 5/10

                           Pulse Rate Definition

                Gain Scaling Base   Max Pulse Rate  Application Type
                  (power of 2)       (100% rating)    (see notes)
                 -----------------   -------------  ----------------

Pulse rate 1:      8192   (1)          7491   (2)      speed (3)

Pulse rate 2:      8192                7491            speed

Pulse rate 3:      8192                3980             fuel

Pulse rate 4:      8192                3980             fuel

  Notes:
     Valid Application Types (speed, fuel, pmg, -----)
```

This screen configures 4 pulse rate inputs that land on the QTBA terminal board as shown in signal diagrams D-19. Hardware signal names in IO.ASG are QnTCQA_FREQ1…4. Note that the first 2 channels in <R1> are jumpered to the <P> core PTBA terminal board.

(1) This is the maximum frequency that the channel will read. It is typically set to the lowest power of 2 that exceeds the maximum input frequency.

(2) This is the frequency corresponding to 100% speed.

(3) This selects the algorithm used in processing the input signal. Choices are:

- speed = speed sensor applications
- fuel = fuel flow divider applications
- pmg = permanent magnet generator (a type of speed input)
- ----- = not used.

```
            TCQA Board Definition - Socket 1 - Screen 6/10

                   Miscellaneous Pulse Rate Data


      Enable ACCEL calculations                        YES (1)
       (requires Enable pulse rate calculation to be Y)

      Enable pulse rate calculation                    YES (1)
       (must be Y if ACCEL is Y)

      Enable HP shaft overspeed protection             YES (2)

      Enable PS3 stall protection                      YES (3)
```

(1) Setting these to YES enables over-acceleration/deceleration protection. These should be set to YES unless there is specific information to the contrary.

(2) Setting this to YES enables primary overspeed protection. This should be set to YES unless there is specific information to the contrary.

(3) Sett ing this to YES enables high-speed compressor stall detection, using the first 2 mA input channels on the TCQA board (screen 5). This should be set to YES for the <R1> core and NO for the <R2> and <R3> cores, unless there is specific information to the contrary.

```
            TCQA Board Definition - Socket 1 - Screen 7/10

                       Vibration Definitions

                    Transducer used       Vibration Sensitivity
                                        (0.05 to 0.50 V peak / ips peak)
                    ---------------     --------------------------------
Transducer  1:             NO (1)             0.15 (2)
Transducer  2:             NO                 0.15
Transducer  3:             NO                 0.15
Transducer  4:             NO                 0.15
Transducer  5:             NO                 0.15
Transducer  6:             NO                 0.15
Transducer  7:             NO                 0.15
Transducer  8:             NO                 0.15
Transducer  9:             NO                 0.15
Transducer 10:             NO                 0.15
Transducer 11:             NO                 0.15
Transducer 12:             NO                 0.15
```

This screen applies to the <R1> and <R3> cores only. The <R2> screen has no purpose. This screen configures 12 seismic (velocity) vibration input channels that land on the TBQB terminal board as shown in signal diagram D-24. Hardware signal names are QnTCQA_VIB01…12 in IO.ASG. Note that the TCQA board in <R1> is connected to the TBQB board in <R2>, while the TCQA board in <R3> is connected to the TBQB board in <R3>.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) This is the sensitivity of the transducer expressed in V/(in/sec).

TCQA Board Definition - Socket 1 - Screen 8/10

Milliamp Input Definitions 1 - 8

	Signal in use	Low Input Diagn	High Input Diagn	Full Scale CDB value	Minimum (4mA) CDB value	Maximum (20mA) CDB value
Signal 1:	**YES***(1)*	**YES***(2)*	**YES***(2)*	**2048***(3)*	**0.0***(4)*	**500.0***(4)*
Signal 2:	**YES**	**YES**	**YES**	**2048**	**0.0**	**500.0**
Signal 3:	**YES**	**YES**	**YES**	**32**	**0.0**	**20.0**
Signal 4:	**YES**	**NO**	**YES**	**32**	**0.0**	**25.0**
Signal 5:	**NO**	**NO**	**NO**	**128**	**0.0**	**100.0**
Signal 6:	**YES**	**YES**	**YES**	**256**	**0.0**	**50.0**
Signal 7:	**NO**	**NO**	**NO**	**128**	**0.0**	**100.0**
Signal 8:	**YES**	**YES**	**YES**	**2**	**0.5**	**1.0**

TCQA Board Definition - Socket 1 - Screen 9/10

Milliamp Input Definitions 9 - 15

	Signal in use	Low Input Diagn	High Input Diagn	Full Scale CDB value	Minimum (4mA) CDB value	Maximum (20mA) CDB value
Signal 9:	**YES**	**YES**	**YES**	**2048**	**700.0**	**1200.0**
Signal 10:	**YES**	**YES**	**YES**	**1024**	**0.0**	**1000.0**
Signal 11:	**NO**	**NO**	**NO**	**128**	**0.0**	**100.0**
Signal 12:	**YES**	**YES**	**YES**	**4**	**0.5**	**2.5**
Signal 13:	**YES**	**YES**	**YES**	**8**	**0.0**	**5.0**
Signal 14:	**YES**	**YES**	**YES**	**8**	**0.0**	**5.0**
Signal 15:	**NO**	**NO**	**NO**	**128**	**0.0**	**100.0**

These two screens configure 15 mA inputs that land on the TBQC terminal board as shown in signal diagram D-12. Hardware signal names are QnTCQA_MAI01…15 in IO.ASG. Note that the first 2 channels in <R1> are reserved for compressor discharge pressure (PS3) sensor inputs. This is mandatory for the stall protection function enabled on screen 6. The full scale values for those 2 channels must be 2048.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) Setting these to YES enables the low and high signal level diagnostic alarms.

(3) This is the full scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an input value that is too low or too high, usually by some power of 2.

(4) These are the control signal values corresponding to the minimum and maximum signal levels.

```
            TCQA Board Definition - Socket 1 - Screen 10/10

                    Miscellaneous Values

Seismic Vibr. Xdcr. Open  Ckt. (0 to 3V dc):    1.0 (1)
    <       V = 30R / (40000+R)    {eg,  1V=1379ê }     >
    < Xdcr Resistance = 40000*V/(30-V) {eg,  1379ê=1V } >


125 V dc Over  Voltage Limit (0 to 145 V dc):    140.0 (2)

125 V dc Under Voltage Limit (0 to 125 V dc):    105.0 (3)

125 V dc Bus Ground Fault    (0 to  65 V dc):    31.23 (4)
    {voltage at which ground fault is indicated}

P15AD & N15AD Diagnostics enable:     YES (5)
P15BD & N15BD Diagnostics enable:     YES (5)

Missed Output Packet ShutDown enable: YES (6)
```

(1) This sets the minimum voltage level across the seismic vibration transducer that will indicate a failure. See below for more information.

(2) This is the highest allowable dc Bus value, as measured between the positive and negative buses, before a diagnostic alarm is generated. See below for more information.

(3) This is the lowest allowable dc Bus value, as measured between the positive and negative buses, before a diagnostic alarm is generated. See below for more information.

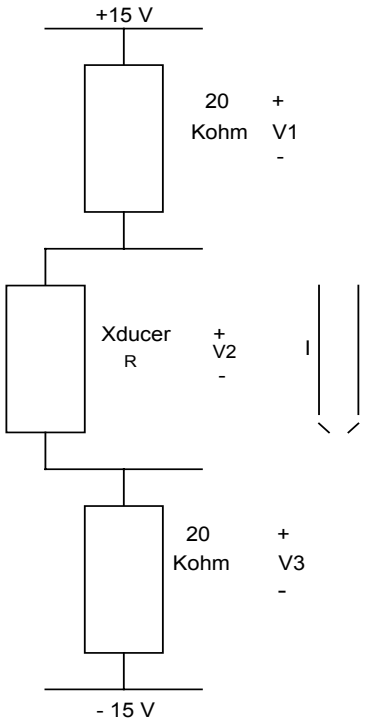
(4) This is the absolute value of the minimum voltage allowable on either the positive or negative bus, measured with respect to ground, before a diagnostic alarm is generated. See below for more information.

(5) These enable diagnostic alarms for the 15 Volt power supplies.

(6) This enables the system to shutdown if an output "packet" is missed The output packet is output data combined into a group or "packet". This data is broadcast over the COREBUS from the Control Engine to the I/O Engines. If one of these output packets is missed, the COREBUS is assumed to have failed and the I/O Engine shuts the unit down. Recommended setting: YES.

Seismic Vibration Transducer Open Circuit Detection

Refer to this sketch:



The voltage V2 is the value being measured. The resistance R is dependent on the type of transducer. In general, any value of R greater than 2 K Ohms indicates a faulty transducer. This typically corresponds to a voltage V2 of approx. 1.43 V.

A small dc current is fed into the circuit to determine a transducer fault condition. The dc current I produces a voltage V2 at the terminal boards. The circuitry measures and compares the voltage to the Seismic Vibration Open Circuit constant. If the measured voltage is greater than the constant, a diagnostic alarm is generated. The actual vibration is the ac component that lies on top of the dc signal from the transducer.

Equations:

$$V_{tot} = V1+V2+V3$$
$$I = V2/R$$
$$V2 = I*R$$
$$V_{tot} = (15-(-15))$$
$$= 30$$
$$V1 = 20{,}000*I$$
$$V3 = 20{,}000*I$$

Work:

$$30 = 20{,}000*I + 20{,}000*I + V2$$
$$30 = 40{,}000*I + V2$$
$$30 = 40{,}000*V2/R + V2$$
$$30*R = 40{,}000*V2 + V2*R$$
$$(30-V2)*R = 40{,}000*V2$$

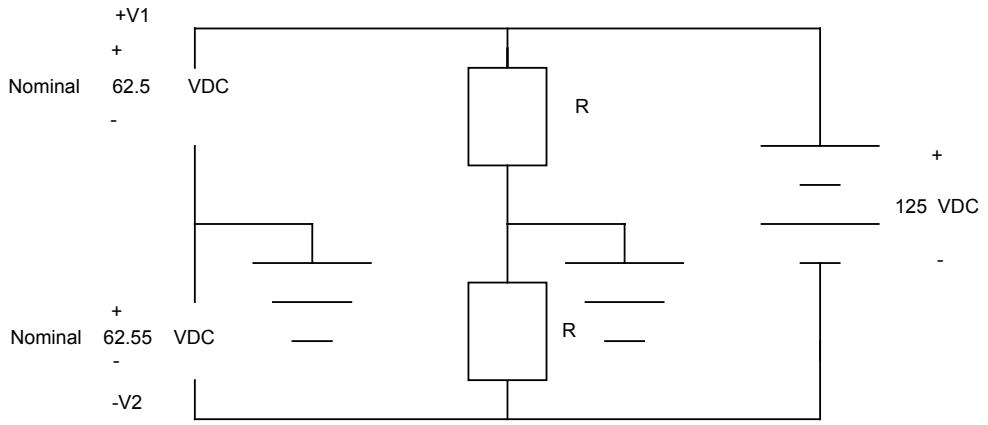
$$R = (40{,}000*V2)/(30-V2)$$

or

$$30*R = (40{,}000+R)*V2$$
$$V2 = (30*R)/(40{,}000+R)$$

Generator Diagnostics

Refer to this sketch:



TCQE

The TCQE board, typically located in the <R1> core in location 3, defines the following functions:

- Proximitor Inputs - Vibration
- Proximitor Inputs - Position
- Proximitor Inputs - Keyphasor
- Milliamp Outputs
- Accelerometer Inputs
- Pulse Rate Inputs
- RTD Inputs

For more information on the above subjects, see Chapters 6 and 7.

```
TCQE Board Definition - Socket 2 - Screen 1/8


 TCQE 196/320 Board Information:

    TCQEP1A 196 firmware:
         Major Rev:        B (1)
         Minor Rev:        B (1)

    TCQEP2A 320 firmware:
         Major Rev:        A (1)
         Minor Rev:        B (1)
```

(1) These are the major and minor revision levels for the EPROMs on the board. These should match the label on the EPROMs and the information in F:\UNITn\PANEL.CFG.

```
              TCQE Board Definition - Socket 2 - Screen 2/8

               Proximitor shaft location and configuration

Prox  1: LP (1)   Prox  2: LP       Prox  3: LP       Prox  4: LP
Prox  5: --       Prox  6: --       Prox  7: --       Prox  8: --



                                 HP rpm      IP rpm      LP rpm
Max CDB scaling value  :          16384 (2)   8192 (2)    8192 (2)


 Notes::    Valid Prox. locations:    IP,  HP,  LP,  -- (not used)
```

This screen, along with the next, configures the 8 vibration proximitor input channels that land on the TBQE terminal board as shown in signal diagram D-9. Hardware signal names are Q1TCQE_VPRX1…8 and Q1TCQE_PRX01…08 in IO.ASG. Proximitors are RF devices that measure the distance between an object and the device itself, such as the distance between the turbine shaft and the proximitor. The device's output is a voltage signal inversely proportional to this distance. The proximitors interpret the voltage's ac component as vibration and changes in the dc component as position changes.

(1) This specifies the shaft that is driving vibrations at the proximitor. The algorithms use this input to select the correct speed and fundamental frequency for processing the signal. Valid choices are:

- **IP** = Intermediate Shaft
- **HP** = High Pressure Shaft
- **LP** = Low Pressure Shaft (Power Turbine)
- **--** = Not Used

(2) These are the full scale values of the speed signals used in the vibration signal processing. The speed signals are defined in IO.ASG with hardware names Q1_HPVIBRREF, Q1_IPVIBRREF, and Q1_LPVIBRREF. The full scale values entered on the screen must match the scale types assigned in IO.ASG (see IOSCALE.DAT for the full scale value of the scale type). A mismatch between these two will produce an input value that is too low or too high, usually by some power of 2. Note that the Control Sequence Program must copy the correct speed values to the signals assigned in IO.ASG.

```
                TCQE Board Definition - Socket 2 - Screen 3/8

       Proximitors 1 thru 8   :-  Peak to Peak Vibration & Position

                  Vibration              Position             Position
              Transducer Sensitivity Transducer Sensitivity     Offset
               (0 to 35.747 V/mil)   (0 to 185.856 V/mil)   (0 to 2048 mils)
              ---------------------- ---------------------- ----------------
Proximitor 1:       0.2 (1)                0.2 (2)               0.0 (3)
Proximitor 2:       0.2                    0.2                   0.0
Proximitor 3:       0.2                    0.2                   0.0
Proximitor 4:       0.2                    0.2                   0.0

Proximitor 5:       0.                     0.                    0.0
Proximitor 6:       0.                     0.                    0.0
Proximitor 7:       0.                     0.                    0.0
Proximitor 8:       0.                     0.                    0.0

Proximitor 1 thru 8 diag. low  limit: (0 to 18 v)     2.002  (4)
Proximitor 1 thru 8 diag. high limit: (0 to 18 v)     17.002 (4)
```

See the previous screen for general information.

(1) This sets the sensitivity of the vibration signal (the ac component), expressed in V/mil. Typical values are:

- Generic Vib/Position Probes - .2 Volts/mil
- Differential Expansion - .1 Volts/mil

(2) This sets the sensitivity of the position signal (the dc component), expressed in V/mil. Typical values are the same as above.

(3) This specifies the starting distance between the proximitor and the object being measured. A 45 mil distance from the object is the ideal conditions for installation of the proximitor. However, this is not always possible or exact due to installation methods. The position offset constant “zeroes” this measurement.

(4) Proximitors may have a non-linear range that is within their operating range. The low and high limits detect any devices that fall outside of the linear range as failed devices. For example, the Bently Nevada proximitors have an operating range of 0 to 20 Volts, but are linear only from 2 to 16 Volts. The low and high limits would detect devices that are reading below 2 Volts or above 16 Volts as a non-linear, failed device.

```
                TCQE Board Definition - Socket 2 - Screen 4/8

           Proximitor Position and Keyphasor Configuration

Position Inputs:      Transducer Sensitivity      Position Offset
                       (0 to 185.856 V/mil)       (0 to 2048 mils)
                      ----------------------      ----------------
    Proximitor   9:        0. (1)                      0.0 (2)
    Proximitor  10:        0.                         0.0

Keyphasor Input:      Transducer Sensitivity      Position Offset
                       (0 to 185.856 V/mil)       (0 to 2048 mils)
                      ----------------------      ----------------
    Proximitor  11:        0.2                         0.0

    Proximitor 9 and 10 diag. low  limit: (0 to 18v)     2.002  (3)
    Proximitor 9 and 10 diag. high limit: (0 to 18v)     17.002 (3)
    Proximitor 11 diagnostic low  limit : (0 to 18v)     2.002  (3)
    Proximitor 11 diagnostic high limit : (0 to 18v)     17.002 (3)
```

This screen configures the 2 position proximitor input channels and the 1 key phasor input channel that land on the TBQE terminal board as shown in signal diagrams D-10 and D-11. Hardware signal names are Q1TCQE_PRX09…11 in IO.ASG. Key phasor inputs are a special proximitor input application. A key phasor senses a notch cut in the turbine shaft. The leading edge of the notch is defined as zero degrees. The phase information is used by algorithms in the controller to perform Fast Fourier Transforms.

(1) This indicates the sensitivity of the transducer, expressed in V/mil.

(2) This specifies the starting distance between the proximitor and the object being measured. A 45 mil distance from the object is the ideal conditions for installation of the proximitor. However, this is not always possible or exact due to installation methods. The position offset constant zeroes this measurement.

(3) Proximitors may have a non-linear range that is within their operating range. The low and high limits detect any devices that fall outside of the linear range as failed devices. For example, the Bently Nevada proximitors have an operating range of 0 to 20 Volts, but are linear only from 2 to 16 Volts. The low and high limits would detect devices that are reading below 2 Volts or above 16 Volts as a non-linear, failed device.

```
                TCQE Board Definition - Socket 2 - Screen 5/8

              Position Milli-Amp Output Configuration

Milli-Amp Output 1:

   Output used (enables output and basic diagnostics):       YES (1)
   Current suicide enable (YES for TMR, NO for Simplex):      NO (2)
   CDB variable full scale value:       16384 (3)
   Minimum ( 4 mA/ 40 mA) CDB value:    0.0     (4)
   Maximum (20 mA/200 mA) CDB value:    11999.9 (4)


Milli-Amp Output 2:

   Output used (enables output and basic diagnostics):      YES
   Current suicide enable (YES for TMR, NO for Simplex):      NO
   CDB variable full scale value:       8192
   Minimum ( 4 mA/ 40 mA) CDB value:    0.0
   Maximum (20 mA/200 mA) CDB value:    4999.9
```

This screen configures two mA output channels that land on the TBQE terminal board as shown in signal diagram D-7. Hardware signal names are Q1_MAO_REF3…4 in IO.ASG. These channels typically drive control devices. Jumpers on the TBQE terminal board select the maximum current output range of either 20 mA or 200 mA.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) Setting this to YES enables a suicide function in which the output current is forced to zero if actual output differs from the reference by 25% of full scale. Recommended setting: NO.

(3) This is the full-scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an output current that is too low or too high, usually by some power of 2.

(4) These are the control signal values corresponding to the minimum and maximum signal currents. For numerical reasons, if the maximum and minimum have the same sign, their ratio (max/min) must be greater than 1.61 or less than 0.11.

```
                TCQE Board Definition - Socket 2 - Screen 6/8

                      LM Vibration Inputs

Accelerometer Inputs:     Sensitivity range (0 to 0.5882 V/ips peak)

                                    ---HP---        ---IP---        ---LP---
Transducer 1 - Used:                  YES (1)          NO              YES
             - Sensitivity:        0.4 (2)         0.4             0.4
Transducer 2 - Used:                  YES              NO              YES
             - Sensitivity:        0.4             0.4             0.4
Transducer 3 - Used:                     NO            NO                 NO
             - Sensitivity:        0.4             0.4             0.4

Transducer    Diagnostic low  limit : (0 to 12v)     0.0  (3)
Transducer    Diagnostic high limit : (0 to 12v)     12.0 (3)

Transducer 1 dc bias voltage - input conversion scaling factor: 32.0 (4)
Transducer 2 dc bias voltage - input conversion scaling factor: 32.0
Transducer 3 dc bias voltage - input conversion scaling factor: 16.0
```

This screen configures 3 accelerometer input channels that land on the TBQE terminal board as shown in signal diagram D-8. Because each accelerometer can pick up vibrations generated by any shaft in the engine, each channel has 3 associate hardware signal names in IO.ASG: Q1TCQE_HPVB1…3, Q1TCQE_IPVB1…3, and Q1TCQE_LPVB1…3.

(1) Setting this to YES enables the channel to pick up signals from the corresponding shaft. If NO, there will be no associated diagnostic alarms.

(2) This indicates the transducer sensitivity in volts/ips of vibration. The value should be the same for all 3 shafts.

(3) These set the voltage levels for which diagnostic alarms will be generated.

(4) These are the full scale values for the probe dc bias voltage signals. This must match the scale type of the signal assigned in IO.ASG (hardware signal names: Q1TCQE_PRB12…14). See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce a bias signal that is too low or too high, usually by some power of 2.

Note that the accelerometer signal processing uses the same shaft speed signals set up for the proximitors on screen 2.

```
                TCQE Board Definition - Socket 2 - Screen 7/8

                            Pulse Rate Definitions

                Input Freq Range Base Max Pulse Rate  Application Type
                    (power of 2)       (100% rating)    (see notes)
                  -----------------   --------------  ----------------

Pulse rate 1&2:       8192 (1)            2880 (2)        speed (3)

Pulse rate 3&4:       8192                2880            speed


          Notes:
             Valid Application Types (speed, fuel, pmg, -----)
             Pulse rate inputs 1 & 2 are TTL inputs
             Pulse rate inputs 3 & 4 are MPU inputs
```

This screen configures 2 pulse rate inputs that land on the <P> core PTBA terminal board, and 2 that land on the <R1> TBQE terminal board, as shown on signal diagram D-5. Hardware signal names in IO.ASG are Q1TCQE_FREQ1…4.

(1) This is the maximum frequency that the channel will read. It is typically set to the lowest power of 2 that exceeds the maximum input frequency.

(2) This is the frequency corresponding to 100% speed.

(3) This selects the algorithm used in processing the input signal. Choices are:

- speed = speed sensor applications
- fuel = fuel flow divider applications
- pmg = permanent magnet generator (a type of speed input)
- ----- = not used.

```
        TCQE Board Definition - Socket 2 - Screen 8/8

            RTD Type Selection
                                        Type Description:(at 0øC)
                                        -------------------------
RTD  1:LM200 (1)                        DIN   - 100 ê Platinum
                                                à = 0.00385
RTD  2:LM200                            PURE  - 100 ê Platinum
                                                à = 0.003926
RTD  3:LM200                            SAMA  - 98.129 ê Platinum
                                                à = 0.00385
RTD  4:LM200                            USIND - 100 ê Platinum
                                                à = 0.00391
                                        N120  - 120 ê Nickel

                                        LM200 - 200 ê Platinum
                                                à = 0.00391
                                        ----  - not used
```

This screen configures 4 RTD channels that land on TBQE terminal board as shown in signal diagram D-4. Hardware signal names in IO.ASG are Q1TCQE_RTD01…04. These channels may also be used to interface to chip detectors.

(1) This is the RTD type. RTD choices are shown above. For chip detectors, the appropriate entry is ohms. With this setting the channel will report the measured resistance in Ω. The signal assigned in IO.ASG must have the scale type OHMS, which must have a full scale value of 512 in IOSCALE.DAT.

TCDA

The TCDA digital I/O boards are located in the <Q11> core and the <R51> core in location 1 of both. Each core has one TCDA board. The TCDA boards are the interface for contact inputs and relay outputs. The I/O Configurator sets two aspects of the TCDA contact inputs:

- Inversion masks
- Change cell masks

For more information on the above subjects, see Chapters 6 and 7.

```
        TCDA Board Definition - Socket 4 - Screen 1/3


           EPROM Revision Information:

                Major Rev:   C (1)

                Minor Rev:   G (1)
```

(1) These are the major and minor revision levels for the EPROM on the board. These should match the label on the EPROM and the information in F:\UNITn\PANEL.CFG.

TCDA Board Definition - Socket 4 - Screen 2/3

Contact Input Assignments - DTBA points 1 thru 92
& DTBB points 1 thru 4

Contact Inputs:	1-10			11-20			21-30			31-40			41-48		
	DTBA Pnt	Inv Msk (1)	Chg Det (2)	DTBA Pnt	Inv Msk	Chg Det	DTBA Pnt	Inv Msk	Chg Det	DTBA Pnt	Inv Msk	Chg Det	DTBA Pnt	Inv Msk	Chg Det
CI x1:	1	**0**	**0**	21	**0**	**0**	41	**0**	**0**	61	**0**	**0**	81	**0**	**0**
CI x2:	3	**0**	**0**	23	**0**	**0**	43	**0**	**0**	63	**0**	**0**	83	**0**	**0**
CI x3:	5	**0**	**0**	25	**0**	**0**	45	**0**	**0**	65	**0**	**0**	85	**0**	**0**
CI x4:	7	**0**	**0**	27	**0**	**0**	47	**0**	**0**	67	**0**	**0**	87	**0**	**0**
CI x5:	9	**0**	**0**	29	**0**	**0**	49	**0**	**0**	69	**0**	**0**	89	**0**	**0**
CI x6:	11	**0**	**0**	31	**0**	**0**	51	**0**	**0**	71	**0**	**0**	91	**0**	**0**
CI x7:	13	**0**	**0**	33	**0**	**0**	53	**0**	**0**	73	**0**	**0**	DTBB1	**1**	**0**
CI x8:	15	**0**	**0**	35	**0**	**0**	55	**0**	**0**	75	**0**	**0**	DTBB3	**1**	**0**
CI x9:	17	**0**	**0**	37	**0**	**0**	57	**0**	**0**	77	**0**	**0**			
CI x0:	19	**0**	**0**	39	**0**	**0**	59	**0**	**0**	79	**0**	**0**			

TCDA Board Definition - Socket 4 - Screen 3/3

Contact Input Assignments - DTBB points 5 thru 100

Contact Inputs:	49-60			61-70			71-80			81-90			91-96		
	DTBB Pnt	Inv Msk	Chg Det	DTBB Pnt	Inv Msk	Chg Det	DTBB Pnt	Inv Msk	Chg Det	DTBB Pnt	Inv Msk	Chg Det	DTBB Pnt	Inv Msk	Chg Det
CI49:	5	**1**	**0**												
CI50:	7	**1**	**0**												
CIx1:	9	**0**	**0**	29	**0**	**0**	49	**0**	**0**	69	**0**	**0**	89	**0**	**0**
CIx2:	11	**0**	**0**	31	**0**	**0**	51	**0**	**0**	71	**0**	**0**	91	**0**	**0**
CIx3:	13	**0**	**0**	33	**0**	**0**	53	**0**	**0**	73	**0**	**0**	93	**0**	**0**
CIx4:	15	**0**	**0**	35	**0**	**0**	55	**0**	**0**	75	**0**	**0**	95	**0**	**0**
CIx5:	17	**1**	**0**	37	**0**	**0**	57	**0**	**0**	77	**0**	**0**	97	**0**	**0**
CIx6:	19	**1**	**0**	39	**0**	**0**	59	**0**	**0**	79	**0**	**0**	99	**0**	**0**
CIx7:	21	**0**	**0**	41	**0**	**0**	61	**0**	**0**	81	**0**	**0**			
CIx8:	23	**0**	**0**	43	**0**	**0**	63	**0**	**0**	83	**0**	**0**			
CIx9:	25	**0**	**0**	45	**0**	**0**	65	**0**	**0**	85	**0**	**0**			
CIx0:	27	**0**	**0**	47	**0**	**0**	67	**0**	**0**	87	**0**	**0**			

These two screens configure the contact inputs that land on the DTBA and DTBB terminal boards as shown in signal diagrams D-41 and D-42. Hardware signal names in IO.ASG are Q11_CI01…96 and R51_CI01…96. The top of the screen provides information about what terminal board the contact inputs are landed on and the contact input number (1 through 48 on screen 2 and 49 through 96 on screen 3). The second column indicates the terminal board screws for each contact input. For example, contact input number 63, located across the top of screen 3, would count down on the column to the DTBB screw number three rows down (inputs 61, 62, to 63). The corresponding terminal board screws would be 33 and 34.

(1) Setting this to *1* enables an inversion of the input. When so enabled, an open contact (circuit) produces a *1* software signal. This is the default for fail-safe tripping and alarming. The scale type for the assigned signal in IO.ASG can be set to CIM_I as a reminder of the inversion, but the scale type has no effect itself.

(2) Setting this to *1* enables a change detection (or SOE) on the contact input.

UCPB

The UCPB board is a daughter board located in the <R1>, <R2>, <R3>, and <R5> cores in location 1. It is mounted on the STCA board. The UCPB board in the <R5> core has no configurable I/O channels. The UCPB board defines the following functions:

- Megawatt input
- Pulse rate inputs

For more information on the above subjects, see Chapters 6 and 7.

```
              UCPB Board Definition - Socket 12 - Screen 1/4


               EPROM Revision Information:

                     Major Rev:   C (1)

                     Minor Rev:   B (1)
```

(1) These are the major and minor revision levels for the EPROM on the board. These should match the label on the EPROM and the information in F:\UNITn\PANEL.CFG.

```
              UCPB Board Definition - Socket 12 - Screen 2/4

              MegaWatt Input

MEGAWATT INPUT (Q_Q_MAI16) :

       Offset  (0 to   3 volts)  :  0.0 (1)

       Gain    (0 to 256 MW/volt):  40.0 (2) (for 512 MW input scaling)

       Used    (yes or no)       :   NO (3)
```

This screen configures the megawatt transducer input that lands on the QTBA terminal board as shown in signal diagram D-18. Hardware signal names in IO.ASG are QnUCPB_MAI16. The megawatt input can either be a current or a voltage input. Hardware jumpers on the QTBA terminal board select the current or voltage option.

(1) This indicates the voltage reading corresponding to 0 MW. If the channel is configured as a current input, the hardware jumper enables a resistor that draws 5 V at the maximum input current (1 mA or 20 mA). For a 0-1 mA input, the screen entry should be 0 V. For a 4-20 mA input, the screen entry should be:

(4 mA / 20 mA) * 5 V = 1 V

(2) This indicates the gain of the signal in MW/V. For a 0-1 mA input the voltage range is 5 V. For a 4-20 mA input the voltage range is 4 V. Note that the channel assumes a full scale value of 512 MW. This must match the scale type of the signal assigned in IO.ASG. See IOSCALE.DAT for the full scale value of the as-

signed scale type (usually MWATT).

```
               UCPB Board Definition - Socket 12 - Screen 3/4

                     Frequency Inputs

TTL 1 INPUT: Pulse rate range limit (power of 2):               256 (1)
             Pulses/sec at 100 % rated input (% input scaling):  16  (2)
                   [or at 50 #/sec flow (#/sec input scaling)]

TTL 2 INPUT: Pulse rate range limit (power of 2):               256
             Pulses/sec at 100 % rated input (% input scaling):  16
                   [or at 50 #/sec flow (#/sec input scaling)]

IP1 INPUT:   Pulse rate range limit (power of 2):               256
             Pulses/sec at 100 % rated input (% input scaling):  16


IP2 INPUT:   Pulse rate range limit (power of 2):               256
             Pulses/sec at 100 % rated input (% input scaling):  16
```

For the <R1> and <R3> cores, this screen configures 4 pulse rate input channels – two that land on the QTBA terminal board and two that land on the TBQB terminal board -- as shown in signal diagram D-20. Hardware signal names in IO.ASG are QnUCPB_FRQ08…11. For the <R2> core, this screen configures only the first 2 channels. The latter two channels do not exist.

(1) This is the maximum frequency that the channel will read. It is typically set to the lowest power of 2 that exceeds the maximum input frequency.

(2) This is the frequency corresponding to 100% speed.

These channels are typically not used for LM applications.

STCA

The STCA board is located in the <R1>, <R2>, <R3>, and <R5> cores in location 1. The STCA board in the <R5> core has no configurable I/O channels. The STCA board defines the following functions:

- Pulse rate inputs
- Compressor stall inputs (CPD inputs)
- Synch check

For more information on the above subjects, see Chapters 6 and 7.

```
              STCA Board Definition - Socket 13 - Screen 1/4


          STCA 196/320 EPROM Revision Information:

             STCA 196 firmware:
                  Major Rev:    A (1)
                  Minor Rev:    B (1)

             STCA 320 firmware:
                  Prom Page Select:    0 (1)
```

(1) These are the major and minor revision levels for the EPROMs on the board. These should match the label on the EPROMs and the information in F:\UNITn\PANEL.CFG.

```
              STCA Board Definition - Socket 13 - Screen 2/4

                     Pulse Rate Definitions


  PR5   INPUT:  Input Frequency Range Base (power of 2):     4096 (3)
  (1)           Pulses/second at rated input (see note 1):   2553 (4)

  PR6   INPUT:  Input Frequency Range Base (power of 2):     4096
  (1)           Pulses/second at rated input (see note 1):   2553

  PR7   INPUT:  Input Frequency Range Base (power of 2):     4096
  (2)           Pulses/second at rated input (see note 1):   2250


Note 1: Rated input is pul/sec for 100 % rated input (with 128% input scaling)
```

This screen configures up to 3 pulse rate input channels.

(1) These two channels are available for the <R1>, <R2>, and <R3> cores. Hardware signal names are QnSTCA_FRQ05…06 in IO.ASG. They land on the QTBA terminal board as shown on signal diagram D-19.

(2) This channel is available for the <R1> and <R3> cores only. Hardware signal name is QnSTCA_FRQ07 in IO.ASG. It lands on the TBQB terminal board as shown on signal diagram D-26.

(3) This is the maximum frequency that the channel will read. It is typically set to the lowest power of 2 that exceeds the maximum input frequency.

(4) This is the frequency corresponding to 100% speed.

Note that the signals assigned to these channels in IO.ASG must have a PCT scale type (with a full scale value of 128). These channels are typically not used for LM applications.

```
              STCA Board Definition - Socket 13 - Screen 3/4

                     CPD  Definitions

CPD transducer - offset                        (volts):   -0.0204
CPD transducer - gain                      (psi/volt):   41.0
CPD transducer - Max CDB value           (power of 2):   2048

CPD pressure low limit - alarm and
   compressor stall detection disable (0 to 512 psi):   12.5

CPD drop threshold gain                       (0 to 1):   0.87
CPD drop threshold intercept         (0 to 1024 psi):   3.4

CPD rate threshold clamp         (0 to 4096 psi/sec):   100.0
CPD rate threshold gain                (0 to 8 /sec):   4.0001
CPD rate threshold intercept          (0 to 512 psi):   25.0
```

This screen configures a special analog input channel that lands on the TBQB terminal board as shown on signal diagram D-26. This channel is typically not used for LM applications.

```
              STCA Board Definition - Socket 13 - Screen 4/4

                   Miscellaneous Definitions

 Bus PT secondary volts at rated (100%) primary volts (60 to 140 V) 115.0
 Generator PT sec volts at rated (100%) primary volts (60 to 140 V) 115.0

 Nominal Bus Frequency            (44 to 64):       60

 Sync Minimum Voltage           (10 to 128%):       50.0
 Amplitude Diff Limit             (0 to 50%):       10.0

 Phase Diff Limit              (0 to 30 deg):       10.0
 Frequency Diff Limit         (0 to 0.33 hz):       0.30
```

This screen configures the bus and generator voltage signals that land on the PTBA terminal board as shown on signal diagram D-50. These signals are typically used for the Synch Check function and are application specific.

TCEA

The TCEA boards are located in the <P1> core in locations 1, 3, and 5. The I/O Configuration is done via the <R1> core's I/O Configurator screens. The I/O Configuration settings on all three TCEA boards must be identical, unless there is specific information to the contrary. The TCEA boards define the following functions:

- Generator Breaker Close inputs
- Flame Detect inputs
- Emergency Overspeed inputs

For more information on the above subjects, see Chapters 6 and 7.

```
            TCEA-X Board Definition - Socket 15 - Screen 1/6

                 EPROM Revision Information:

                      Major Rev:   A (1)

                      Minor Rev:   D (1)
```

(1) These are the major and minor revision levels for the EPROM on the board. These should match the label on the EPROM and the information in F:\UNITn\PANEL.CFG.

```
            TCEA-X Board Definition - Socket 15 - Screen 2/6

                    Generator Breaker Definitions

Gen Breaker 1 close time:                (1) 5    cycles (0 - 255)

Gen Breaker 1 close time diagnostic enable?    NO (2)

Gen Breaker 2 close time:                    5    cycles (0 - 255)

Gen Breaker 2 close time diagnostic enable?    NO

Breaker adaptive adjustment limit:       (3) 3    cycles (0 - 255)

Breaker self adapt correction enable?        YES (4)

Gen Panel 125 vdc voltage diagnostic enable?   NO (5)
```

The TCEA boards perform the automatic synchronizing function and close the breaker if all of the breaker close permissives are met.

(1) These define the number of cycles required between the time the breaker closure is initialized from the Mark V LM controller to the time the breaker actually closes. The constant is specified in cycles, keeping it independent of the turbine/generator set frequency. The constant is necessary for breaker closure to occur at approximately zero phase difference between the generator and the system bus for a zero current flow through the breaker at closure time. The value is dependent on breaker type.

(2) These enable the breaker close time diagnostic function.

(3) The specifies the maximum allowable adaptive adjustment to the breaker close time. When the adaptive adjustment function is enabled, the controller calculates the actual breaker closure time and adjusts the assumed value accordingly. The adjustments are made in increments of one. For example, the above values set the close time at 5 cycles. If the actual required time becomes 8 cycles, the controller adjusts the 5 to an 8, taking three closures to make this change. If the time required becomes a 9, the controller does not make another adjustment, but leaves it at 8 and will generate a diagnostic alarm.

(4) This enables the breaker closure time adaptive adjustment described above.

(5) This enables the monitoring of the generator breaker close potential and an asso-

ciated diagnostic alarm.

```
            TCEA-X Board Definition - Socket 15 - Screen 3/6

             Flame Detect Threshold Values

                      Detection Level A     Detection Level B
                      Values (0 to 255)     Values (0 to 255)
                      ----------------      -----------------
   Flame detect 1:          2 (1)                 4 (2)
   Flame detect 2:          2                     4
   Flame detect 3:          2                     4
   Flame detect 4:          2                     4

   Flame detect 5:          2                     4
   Flame detect 6:          2                     4
   Flame detect 7:          2                     4
   Flame detect 8:          2                     4

                    Detection level values are flame detector pulses
                    during the 1/16 second sample period.
```

This screen configures the 8 flame detector channels that land on PTBA terminal board as shown on signal diagram D-49. Hardware signal names are L28FDA…H in IO.ASG.

(1) This is the minimum number of pulses received in 1/16th of a second that will indicate a detected flame. A value of 2 in this field is equivalent to a 32 Hz signal from the flame detectors. Normal operation produces a 300 Hz signal, or about 18 pulses per 1/16th of a second.

(2) This is a higher threshold level that is not used in LM applications. Set it equal or higher than the previous entries.

```
            TCEA-X Board Definition - Socket 15 - Screen 4/6

       Configuration Constants

Trip Board Id             (ext, fpt, gas, med, large):        gas (1)
 ( ext=TCTE  fpt=TCTF  gas=TCTG  med=TCTS  large=TCTL )
System Configuration                  (LM, SMX, ---):       LM (2)
Trip Anticipation Enabled?         <large steam only>:      NO (3)

HP input frequency for 100 percent rated speed:            7491 (4)

HP input frequency for overspeed trip setting:             8090 (5)

HP Overspeed Trip Board Jumper Positions (derived from trip frequency):
     J21   J20      J19   J18   J17   J16      J15   J14    J13   J12
      0     1        1     1     1     1        1     0      0     1 (6)

System Configuration Board Jumper Positions (derived from Sys Config):
                    J29   J28
                     0     1 (7)
```

This screen configures the emergency overspeed settings for the high pressure shaft (HP).

(1) This identifies the trip board type used by the system. For LM applications, this is typically the TCTG board. The trip board connects to the TCEA board and configures it with fixed ID jumpers. The constant must match the trip board type.

(2) This sets the application type. The system configuration corresponds to hardware jumper settings. If the hardware jumper settings do not match the system configuration, a diagnostic alarm is generated. The correct setting is “LM”.

(3) This enables the monitoring of acceleration in large steam turbine applications. This should be set to NO in LM applications.

(4) This specifies the 100% rated speed in frequency. The frequency of the pulses from the shaft speed sensors depend on the number of teeth on the feedback wheel as well as the shaft RPM. If the above system uses a 60 tooth feedback wheel and 100% rated speed is 3600 RPM, the 100% rated frequency would be 3600 Hz (1Hz = 1 RPM).

(5) This specifies the frequency at which to initiate an emergency overspeed trip.

(6) These settings are calculated by the I/O Configurator based on the entry for item 5. They are not manually entered. These are the required hardware jumper settings on the TCEA boards. If the hardware jumpers do not match, the board will not boot up completely (to “A7”).

(7) These settings are calculated by the I/O Configurator based on the entry for item 2. They are not manually entered. These are the required hardware jumper settings on the TCEA boards. If the hardware jumpers do not match, the board will not boot up completely (to “A7”).

```
            TCEA-X Board Definition - Socket 15 - Screen 5/6

               LP Configuration Constants


LP input frequency for 100 percent rated speed:            2880 (1)

LP input frequency for Overspeed Trip Setting:             3240 (2)
   (0 = NOT USED; Single shaft, LP trip disabled)

HP % speed at which to check for LP shaft turning:         70.0 (3)




LP Overspeed Trip Board Jumper Positions (derived from trip frequency):
     J27   J26      J25   J24   J23   J22      J11   J10   J9    J8
      0     0        1     1     0     0        1     0     1     0 (4)
```

This screen configures the emergency overspeed settings for the low pressure shaft (LP).

(1) This specifies the 100% rated speed in frequency. The frequency of the pulses from the shaft speed sensors depend on the number of teeth on the feedback wheel as well as the shaft RPM. If the above system uses a 60 tooth feedback wheel and 100% rated speed is 3600 RPM, the 100% rated frequency would be 3600 Hz (1Hz = 1 RPM).

(2) This specifies the frequency at which to initiate an emergency overspeed trip.

(3) This specifies the HP shaft speed (%) at which the LP shaft should be turning. If it is not turning at this speed, a trip and alarm will occur.

(4) These settings are calculated by the I/O Configurator based on the entry for item 2. They are not manually entered. These are the required hardware jumper settings on the TCEA boards. If the hardware jumpers do not match, the board will not boot up completely (to "A7").

```
            TCEA-X Board Definition - Socket 15 - Screen 6/6

               LP Acceleration Protection
                (applicable to GAS only)

Enable LP Acceleration protection:  NO (1)
(used in GAS Turbine System ONLY)

Number of LP speed interrupts between acceleration checks: 6 (2)
             (each interrupt represents 8 teeth passing)

Number of LP speed interrupts for speed calculation: 9 (3)

Minimum LP speed (in Hz) to enable protection: 5680 (4)

LP Acceleration Limit (in hz/sec): 1280 (5)
```

This screen enables the LP acceleration protection function.

(1) Setting this to YES enables the function.

(2) This specifies the maximum number of interrupts (groups of 8 pulses) between acceleration checks. The recommended value for LM applications is 6.

(3) This specifies the number of interrupts (groups of 8 pulses) between speed calculations. The recommended value for LM applications is 9.

(4) This is the minimum LP speed (Hz) for which the protection function is enabled.

(5) This is the acceleration limit in Hz/sec.

See Chapter 7 for more information.

TCCA

The TCCA board is located in the <R5> core location 2. It is the "Turbine Control <R5> Micro Application Board A". The TCCA configuration defines the following functions:

- Thermocouple inputs
- RTD inputs
- Milliamp inputs
- Shaft voltage and current monitoring

For more information on the above subjects, see Chapters 6 and 7.

```
                TCCA Board Definition - Socket 1 - Screen 1/7


                   EPROM Revision Information:

                        Major Rev:   A (1)

                        Minor Rev:   D (2)
```

(1) These are the major and minor revision levels for the EPROM on the board. These should match the label on the EPROM and the information in F:\UNITn\PANEL.CFG.

```
                TCCA Board Definition - Socket 1 - Screen 2/7

                        Thermocouple Type Selection

TC  1:  - (1)  TC 10:  -      TC 19:  -       TC 28:  -      TC 37:  -
TC  2:  -      TC 11:  -      TC 20:  -       TC 29:  -      TC 38:  -
TC  3:  -      TC 12:  -      TC 21:  -       TC 30:  -      TC 39:  -

TC  4:  -      TC 13:  -      TC 22:  -       TC 31:  -      TC 40:  -
TC  5:  -      TC 14:  -      TC 23:  -       TC 32:  -      TC 41:  -
TC  6:  -      TC 15:  -      TC 24:  -       TC 33:  -      TC 42:  -

TC  7:  -      TC 16:  -      TC 25:  -       TC 34:  -
TC  8:  -      TC 17:  -      TC 26:  -       TC 35:  -
TC  9:  -      TC 18:  -      TC 27:  -       TC 36:  -


                        Valid types:    K, J, E, T
                          not used :    -
```

This screen configures 42 thermocouple channels that land on the <R5> TBQA terminal board as shown in signal diagrams D-30, D-31, and D-32. Hardware signal names in IO.ASG are R5TCCA_TC01…42.

(2) This sets the type of thermocouple connected. If not used (-), there will be no associated diagnostic alarms.

```
              TCCA Board Definition - Socket 1 - Screen 3/7

                   RTD Type Selection
       (1)                                      Type Description:(at 0øC)
RTD  1:-----   RTD 11:  DIN   RTD 21: ohms     -------------------------
RTD  2:-----   RTD 12:  DIN   RTD 22: ohms     CU10  - 9.035 ê Copper
                                                      (10 ê at 25ø C)
RTD  3:-----   RTD 13:  DIN   RTD 23:-----     DIN   - 100 ê Platinum,
RTD  4:  DIN   RTD 14:  DIN   RTD 24:-----                à = 0.00385
                                               PURE  - 100 ê Platinum,
RTD  5:  DIN   RTD 15:  DIN   RTD 25:-----                à = 0.003926
RTD  6:  DIN   RTD 16:  DIN   RTD 26:-----     SAMA  - 98.129 ê Platinum,
                                                        à = 0.00385
RTD  7:  DIN   RTD 17:  DIN   RTD 27:-----     USIND - 100 ê Platinum,
RTD  8:  DIN   RTD 18:  DIN   RTD 28:-----                à = 0.00391
                                               N120  - 120 ê Nickel
RTD  9:  DIN   RTD 19:  DIN   RTD 29:-----
RTD 10:  DIN   RTD 20: ohms   RTD 30:-----     LM200 - 200 ê Platinum
                                                        à = 0.00391
                                               ----  - not used
```

This screen configures 30 RTD channels that land on TBCA terminal board as shown in signal diagrams D-33 and D-34. Hardware signal names in IO.ASG are R5TCCA_RTD01…30. These channels may also be used to interface to chip detectors.

(1) This is the RTD type. RTD choices are shown above. For chip detectors, the appropriate entry is “ohms”. With this setting the channel will report the measured resistance in Ω. The signal assigned in IO.ASG must have the scale type OHMS, which must have a full scale value of 512 in IOSCALE.DAT.

TCCA Board Definition - Socket 1 - Screen 4/7

Milliamp Input Definitions 1 - 8

	Signal in use	CDB value Full Scale	CDB value at 4 mA	CDB value at 20 mA	Enable Low diag	Enable High diag
Signal 1:	**YES** *(1)*	**256** *(2)*	**0.0** *(3)*	**150.0** *(3)*	**YES** *(4)*	**YES** *(4)*
Signal 2:	**YES**	**256**	**0.0**	**200.0**	**YES**	**YES**
Signal 3:	**NO**	**512**	**0.0**	**100.0**	**NO**	**NO**
Signal 4:	**NO**	**512**	**0.0**	**100.0**	**NO**	**NO**
Signal 5:	**NO**	**1024**	**0.0**	**1000.0**	**NO**	**NO**
Signal 6:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 7:	**YES**	**512**	**0.0**	**65.0**	**YES**	**YES**
Signal 8:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**

TCCA Board Definition - Socket 1 - Screen 5/7

Milliamp Input Definitions 9 - 14

	Signal in use	CDB value Full Scale	CDB value at 4 mA	CDB value at 20 mA	Enable Low diag	Enable High diag
Signal 9:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 10:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 11:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 12:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 13:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**
Signal 14:	**NO**	**128**	**0.0**	**100.0**	**NO**	**NO**

These two screens configure the 14 mA inputs that land on the CTBA terminal board as shown in signal diagram D-34. Hardware signal names in IO.ASG are R5TCCA_MAI01…14.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) This is the full scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an input value that is too low or too high, usually by some power of 2.

(3) These are the control signal values corresponding to the minimum and maximum signal levels.

(4) Setting these to YES enables the low and high signal level diagnostic alarms.

```
                TCCA Board Definition - Socket 1 - Screen 6/7

                       Miscellaneous Values


         System Bus Frequency Selection:

               Is this a 50 hz system? (Yes or No):     NO
```

This screen selects the system frequency.

```
                TCCA Board Definition - Socket 1 - Screen 7/7

                  Shaft Voltage Monitor Definitions


     Current Shunt Resistance (0.0005 to 0.125 ohms):    0.005


Shaft current monitor reports the ac rms current through the shunt.

The shaft voltage monitor reports the frequency at which the shaft voltage
exceeds fixed hardware limits.

An ac test will inject signals to the TCCA board circuits and produce 1000Hz
for the voltage monitor frequency and 12 to 20A for the current monitor.

A dc test will inject a dc current into the grounding brushes and the shunt.
The resultant voltages are used to calculate the resistance to ground for each.
```

This screen selects the shunt resistance for the Shaft current monitor function.

TCCB

The TCCB board is located in the <R5> core location 3. It is the "Turbine Control Micro Application Board B". The TCCB configuration defines the following functions:

- RTD inputs
- Milliamp inputs

For more information on the above subjects, see Chapters 6 and 7.

```
              TCCB Board Definition - Socket 2 - Screen 1/7


         TCCB 196/320 EPROM Revision Information: (#B)

            TCCB 196 firmware:
                 Major Rev:    A (1)
                 Minor Rev:    C (1)

            TCCB 320 firmware:
                 Major Rev:    A (1)
                 Minor Rev:    B (1)
```

(5) These are the major and minor revision levels for the EPROMs on the board. These should match the label on the EPROMs and the information in F:\UNITn\PANEL.CFG.

```
              TCCB Board Definition - Socket 2 - Screen 2/7

          RTD Type Selection
                                    Type Description: (at 0øC)
                                    ------------------------------------
RTD 1:-----   RTD  8:----- (1) CU10  - 9.035 ê Copper (10 ê at 25ø C)

RTD 2:-----   RTD  9:-----     DIN   - 100 ê Platinum, à = 0.00385

RTD 3:-----   RTD 10:-----     PURE  - 100 ê Platinum, à = 0.003926

RTD 4:-----   RTD 11:-----     SAMA  - 98.129 ê Platinum, à = 0.00385

RTD 5:-----   RTD 12:-----     USIND - 100 ê Platinum, à = 0.00391

RTD 6:-----   RTD 13:-----     N120  - 120 ê Nickel

RTD 7:-----   RTD 14:-----     LM200 - 200 ê Platinum à = 0.00391

                                    ----  - not used
```

This screen configures 14 RTD channels that land on TBCB terminal board as shown in signal diagram D-35. Hardware signal names in IO.ASG are R5TCCB_RTD01…14. These channels may also be used to interface to chip detectors.

(1) This is the RTD type. RTD choices are shown above. For chip detectors, the appropriate entry is “ohms”. With this setting the channel will report the measured resistance in Ω. The signal assigned in IO.ASG must have the scale type OHMS, which must have a full scale value of 512 in IOSCALE.DAT.

```
                TCCB Board Definition - Socket 2 - Screen 3/7

              Milliamp Input Definitions   1 thru 8  (4 to 20 mA)

              Signal    CDB value    CDB value  CDB value  Enable   Enable
              in use    Full Scale    at 4 mA   at 20 mA   Low diag High diag
              -------   ----------   ---------  ---------  -------- ---------
  Signal  1:     NO (1)   128 (2)     0.0 (3)    100.0 (3)    NO (4)   NO (4)
  Signal  2:     NO       128         0.0        100.0        NO       NO
  Signal  3:     NO       128         0.0        100.0        NO       NO
  Signal  4:     NO       128         0.0        100.0        NO       NO
  Signal  5:     NO       128         0.0        100.0        NO       NO
  Signal  6:     NO       128         0.0        100.0        NO       NO
  Signal  7:     NO       128         0.0        100.0        NO       NO
  Signal  8:     NO       128         0.0        100.0        NO       NO
```

```
                TCCB Board Definition - Socket 2 - Screen 4/7

              Milliamp Input Definitions   9 thru 14  (4 to 20 mA)


              Signal    CDB value    CDB value  CDB value  Enable   Enable
              in use    Full Scale    at 4 mA   at 20 mA   Low diag High diag
              -------   ----------   ---------  ---------  -------- ---------
  Signal  9:     NO       128         0.0        100.0        NO       NO
  Signal 10:     NO       128         0.0        100.0        NO       NO
  Signal 11:     NO       128         0.0        100.0        NO       NO
  Signal 12:     NO       128         0.0        100.0        NO       NO
  Signal 13:     NO       128         0.0        100.0        NO       NO
  Signal 14:     NO       128         0.0        100.0        NO       NO
```

```
                TCCB Board Definition - Socket 2 - Screen 5/7

    Milliamp Input Definitions  15 thru 22  (4 to 20 mA) or (0 to 1 mA)

              Signal    CDB value    CDB value  CDB value  Enable   Enable
              in use    Full Scale    at 4 mA   at 20 mA   Low diag High diag
-------   ----------   ---------  ---------  -------- ---------
  Signal 15:     NO       128         0.0        100.0        NO       NO
  Signal 16:     NO       128         0.0        100.0        NO       NO
  Signal 17:     NO       128         0.0        100.0        NO       NO
  Signal 18:     NO       128         0.0        100.0        NO       NO
  Signal 19:     NO       128         0.0        100.0        NO       NO
  Signal 20:     NO       128         0.0        100.0        NO       NO
  Signal 21:     NO       128         0.0        100.0        NO       NO
  Signal 22:     NO       128         0.0        100.0        NO       NO
```

These three screens configure the 22 mA inputs that land on the TCCB terminal board as shown in signal diagram D-28. Hardware signal names in IO.ASG are R5TCCB_MAI01…22.

(1) Setting this to YES enables the channel. If NO, there will be no associated diagnostic alarms.

(2) This is the full scale value of the signal assigned to the channel. This must match the scale type of the signal assigned to the channel. See IO.ASG for the assigned signal name and scale type. See IOSCALE.DAT for the full scale value of the scale type. A mismatch between these two will produce an input value that is too

low or too high, usually by some power of 2

(3) These are the control signal values corresponding to the minimum and maximum signal levels.

(4) Setting these to YES enables the low and high signal-level diagnostic alarms.

```
              TCCB Board Definition - Socket 2 - Screen 6/7

               Generator Configuration Information


Nominal Bus Frequency                    (0 to 64 hz):    60.0

Bus Voltage (at 115 VRMS PT out   :      0 to 256KV):    51.64

Gen Voltage (at 115 VRMS PT out   :      0 to 256KV):    51.64

Gen Current (at 5 AMPS RMS CT out : 0 to 32768 amps):    1834.3

Power                                ( 0 to 2048 MW):    47.36
       Power = Gen Voltage * Gen Current
```

This screen configures the system to what type of generator it has. These settings are application specific. The **Power** setting correlates to the equation below the setting.

```
              TCCB Board Definition - Socket 2 - Screen 7/7

                     Miscellaneous Values
                  (applies only to 1st TCCB)

     System Frequency is 50 Hertz:  NO

     Voltage Phase Shift (-60 to 60 deg): 0.0
```

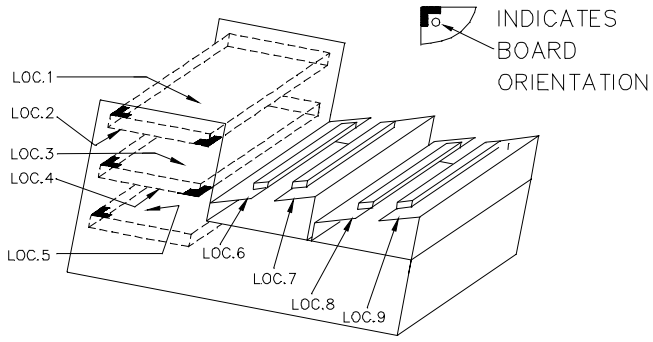
This screen sets the system frequency and the voltage phase shift value.

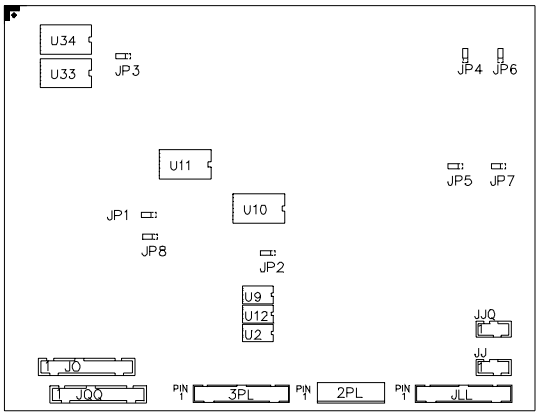
Appendix H Core Diagrams

Introduction

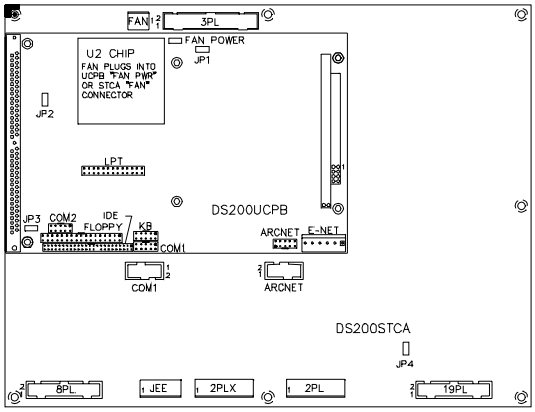
The following drawings are reproductions of the hardware diagrams normally found in the plastic pockets, on the inside of the door in each core of the Mark V LM Panel. They provide the user with a "roadmap" for each circuit card and terminal board installed in a Mark V LM Panel. The general position of connectors and hardware jumpers are provided to help the user during installation or panel modifications.

These drawings are presented as follows:

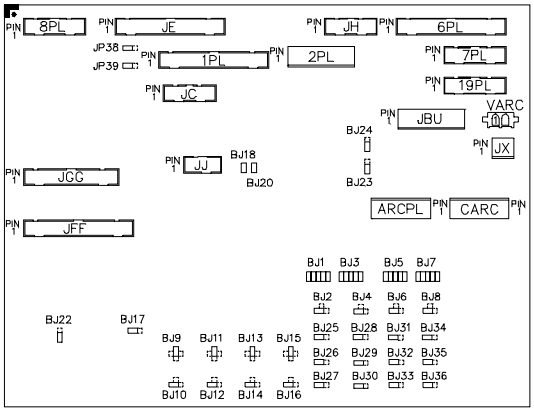




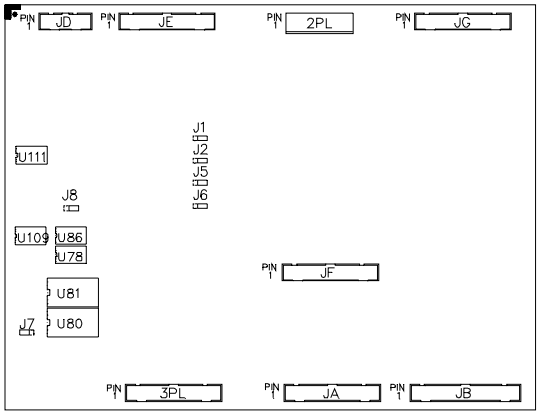
TCQEG#A LOC. 3



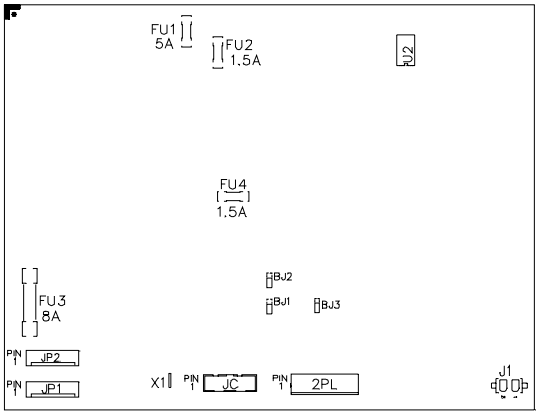
TMIAP#A LOC. 1



TCQCG#B LOC. 4

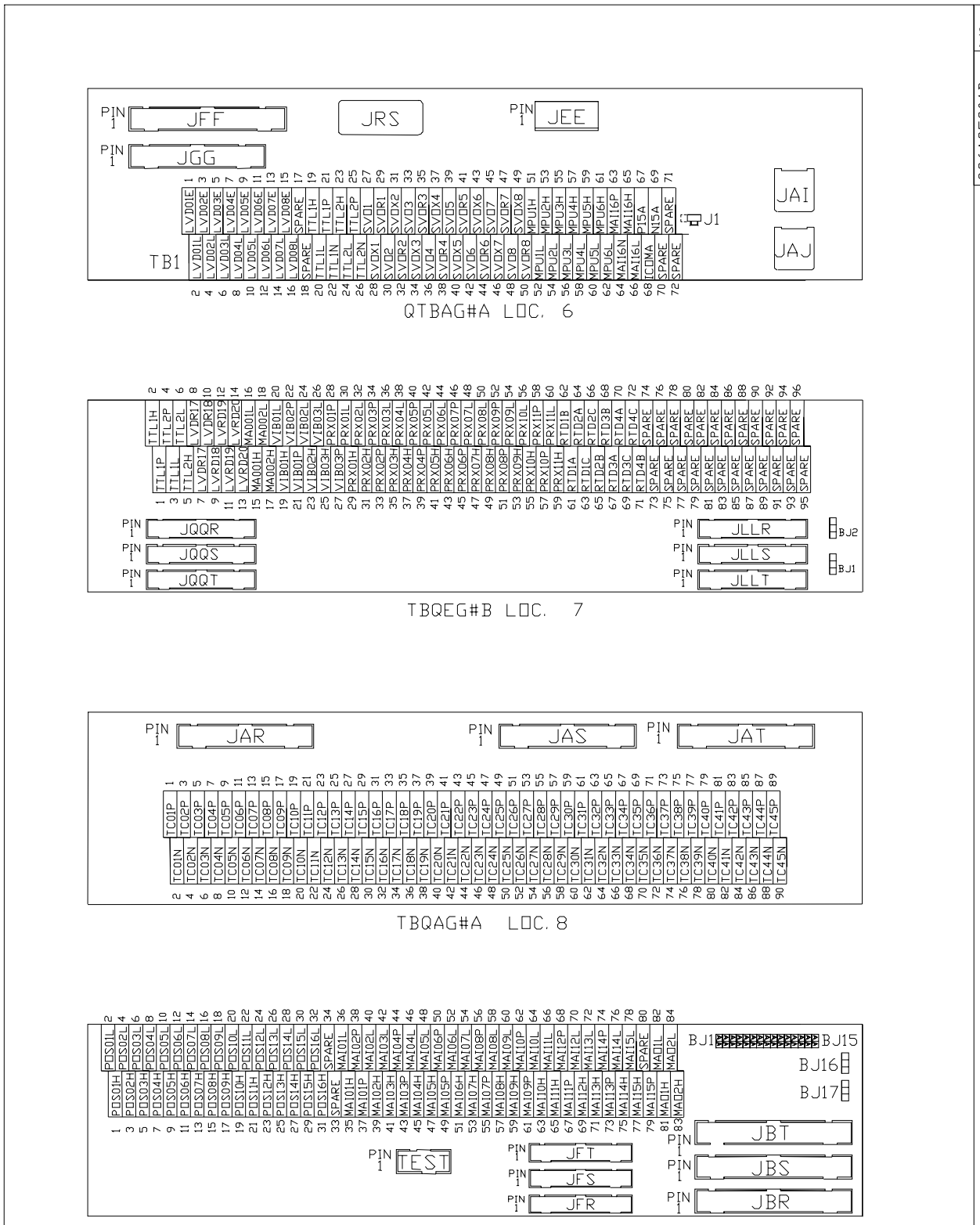


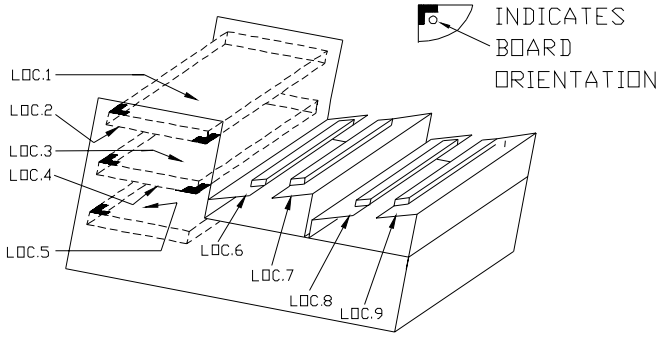
TCQAG#B LOC. 2



TCPSG#A LOC. 5

REV.3	REV.2	REV.1 10-24-95 JRW	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R1> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REQN.		336A3580AB SH. NO. 1 CONT. ON SH. 2
REV.6	MADE BY J.R. WALTON		I.C. NO.		

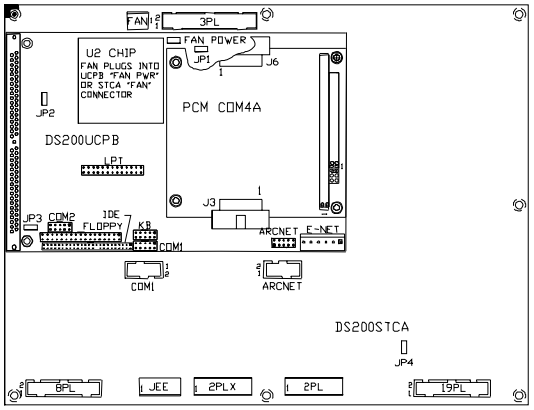

SH. NO. 2
336A3580AB
CONT. ON SH. FNL
PIN 1 JFF
JRS
PIN 1 JEE
PIN 1 JGG
JAI
JAJ
J1
TB1
QTBAG#A LOC. 6
JQQR
JQQS
JQQT
JLLR
JLLS
JLLT
BJ2
BJ1
TBQEG#B LOC. 7
JAR
JAS
JAT
TBQAG#A LOC. 8
BJ1
BJ15
BJ16
BJ17
JBT
JBS
JBR
TEST
JFT
JFS
JFR
TBQCG#A LOC. 9
REV.3
REV.4
REV.5
REV.2
REV.1 12-20-95 JRW
ISSUED 06-22-95
MADE BY J.R. WALTON
PRINTS TO
ENGINEER J.R. WALTON
FIRST MADE FOR REGN.
I.C. NO.
GENERAL ELECTRIC COMPANY
GE DRIVE SYSTEMS
SALEM, VA. U.S.A.
TITLE <R1> CORE MKV+
336A3580AB
CONT. ON SH. FNL
SH. NO. 2



SH. NO. 1

336A3580AN

CONT. ON SH. 2



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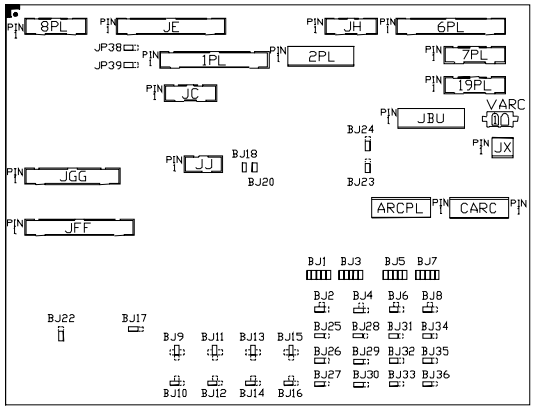
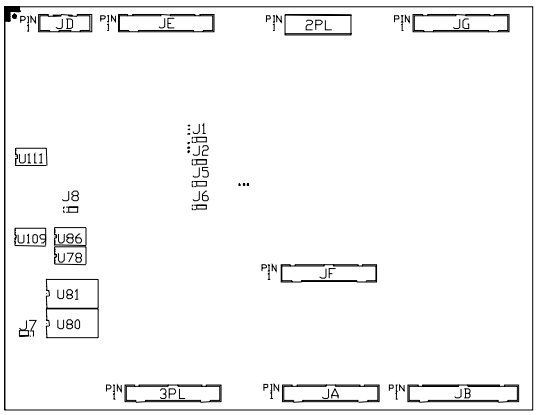
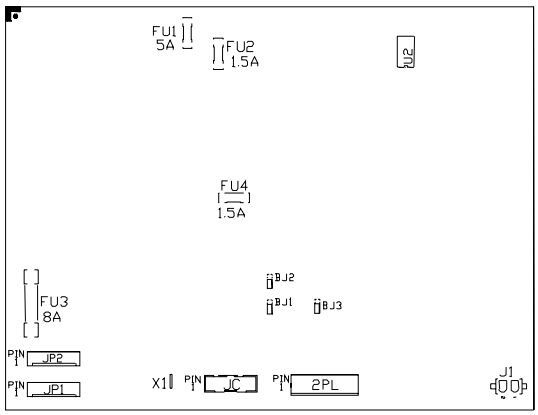


TCQCG#B LOC. 4

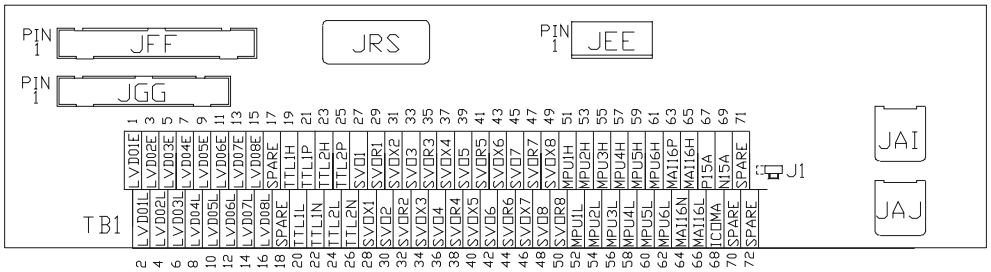


TCQAG#B LOC. 2

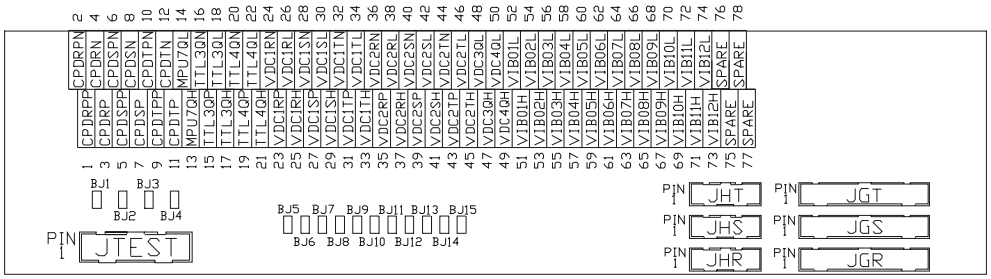


TCPSG#A LOC. 5

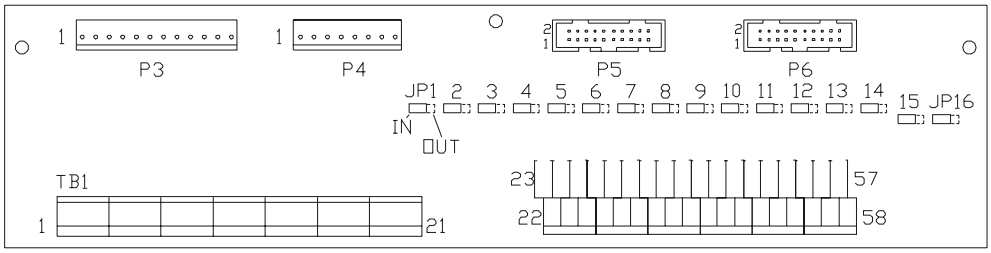
REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R2> CORE MKV LM
REV.4	ISSUED 08-21-96	PRINTS TO	FIRST MADE FOR REQN.		336A3580AN SH. NO. 1
REV.5	MADE BY J.R. WALTON		IC. NO.		CONT. ON SH. 2



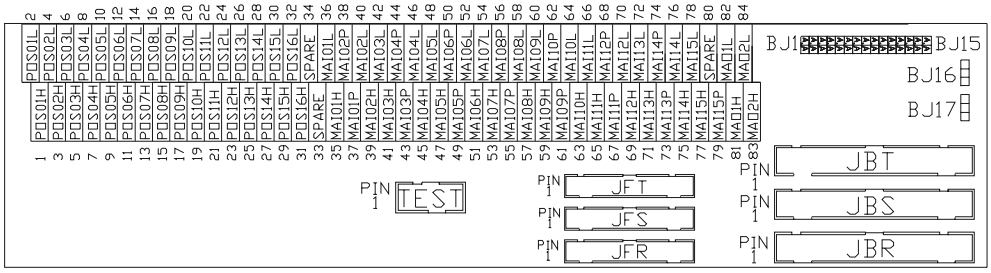
QTBAG#A LOC. 6



TBQBG#A LOC. 7

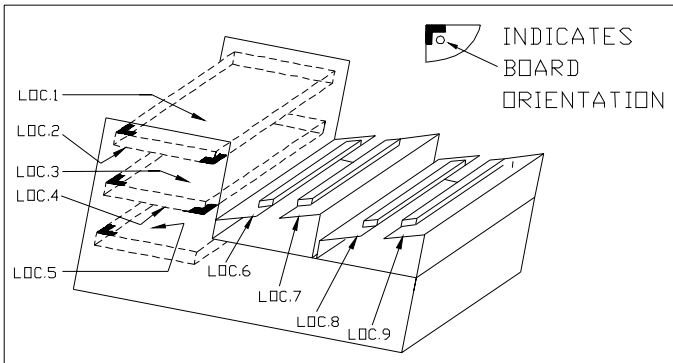


TBSAG#A LOC. 8



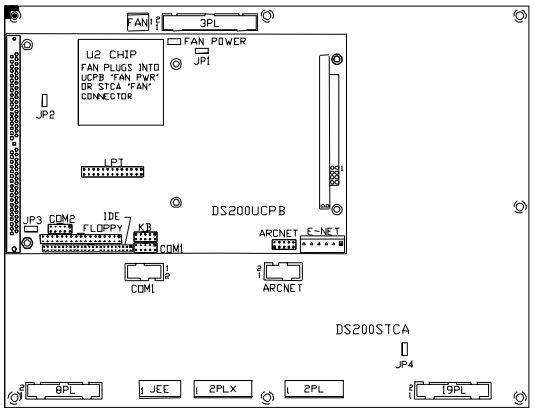
TBQCG#A LOC. 9

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R2> CORE MKV LM
REV.4	ISSUED 08-21-96	PRINTS TO	FIRST MADE FOR REQN.		336A3580AN SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. FNL

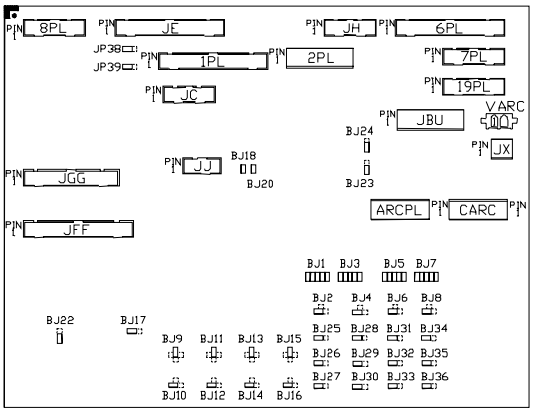


SH. NO. 1

336A3580AF
CONT. ON SH. 2



TMIAP#A LOC. 1



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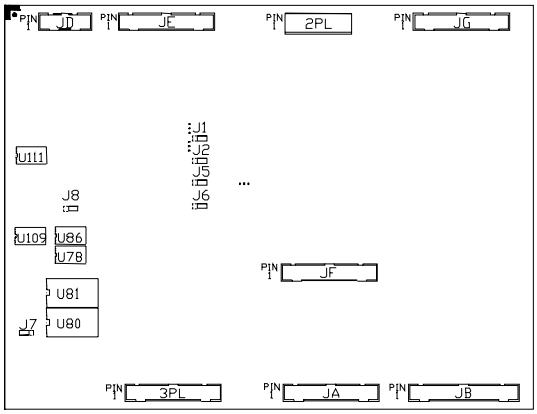
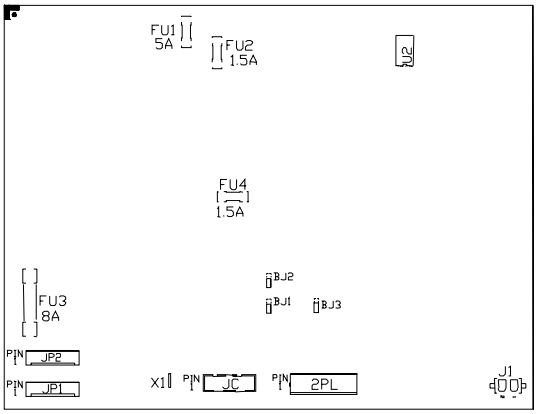
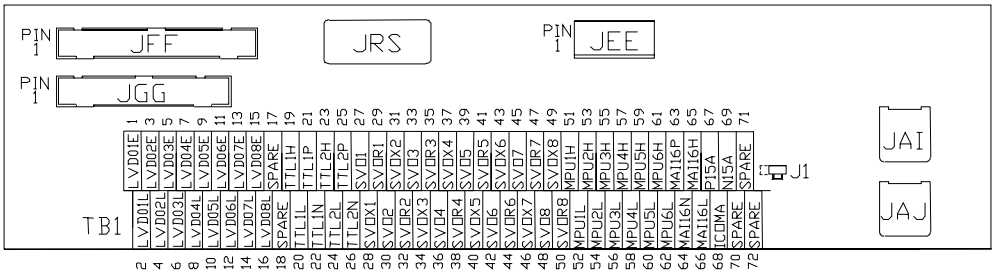


TCQAG#B LOC. 2

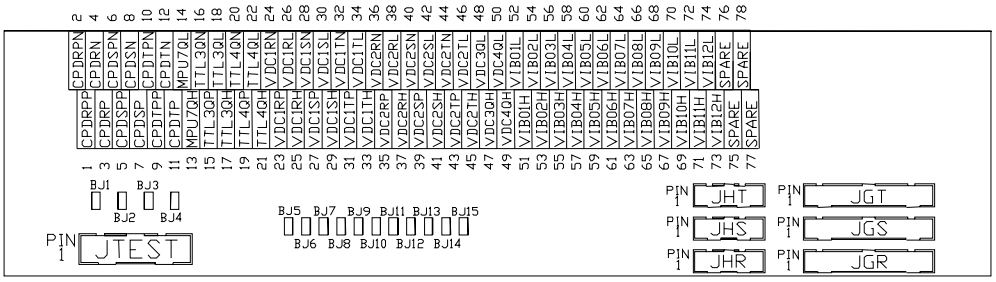


TCPSG#A LOC. 5

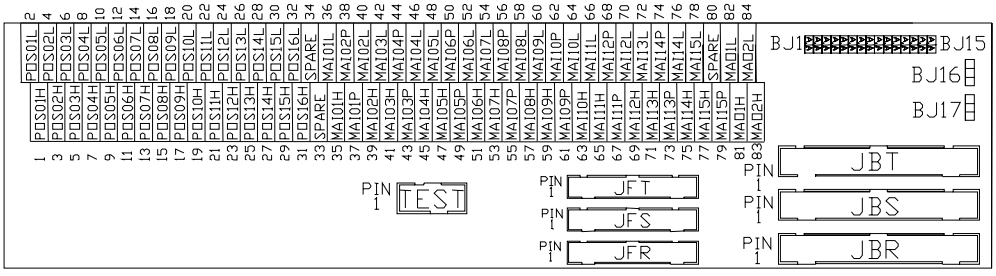
REV.3	REV.2	REV.1 10-24-95 JRW	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R3> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR RECON.		336A3580AF SH. NO. 1 CONT. ON SH. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		



QTBAG#A LOC. 6



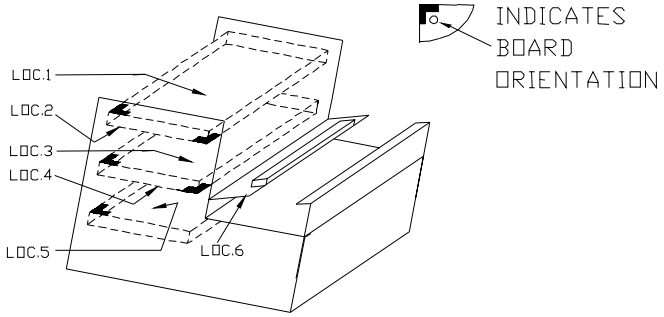
TBQBG#A LOC. 7



TBQCG#A LOC. 9

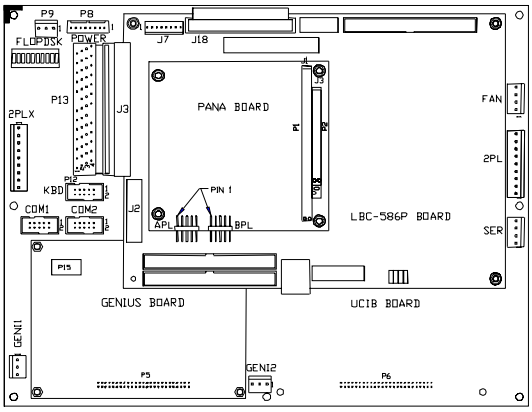
REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R3> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REQN.		336A3580AF SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. FNL

SH. NO. 2
336A3580AF
CONT. ON SH. FNL

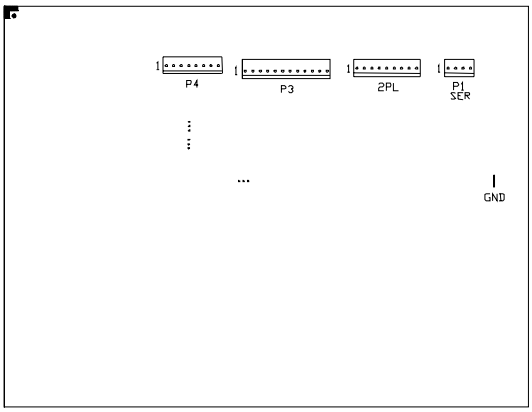


SH. NO. 1

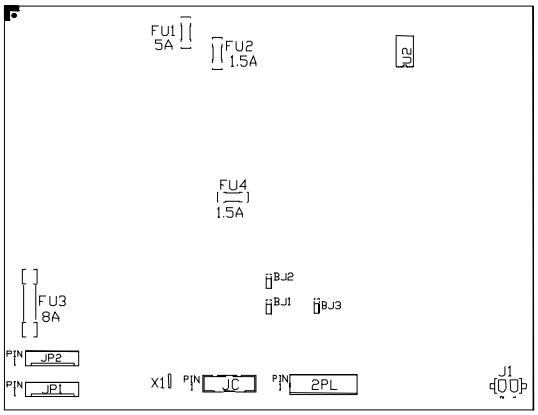
336A3580AT
CONT. ON SH. 2



TMCBP#A LOC. 1



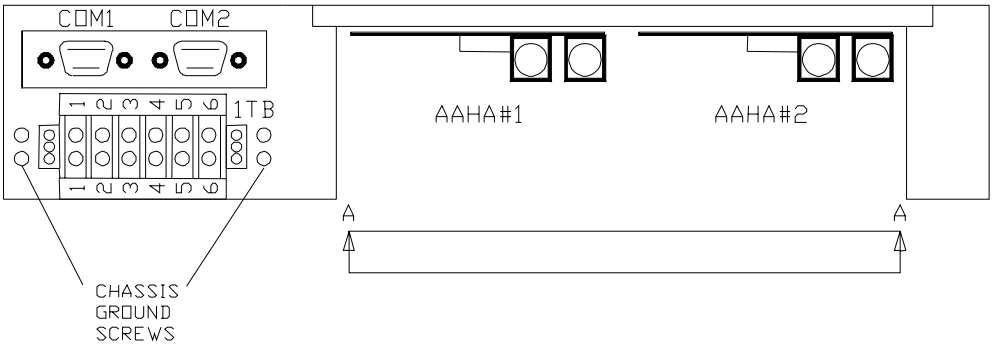
TCSAG#A LOC. 2

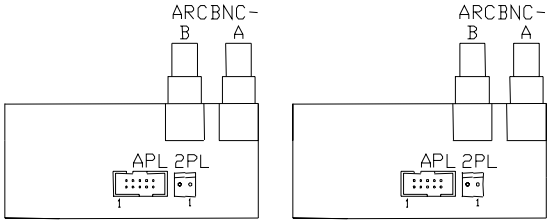


TCPSG#A LOC. 5

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA U.S.A.	TITLE <R> CORE MKV LM
REV.4	ISSUED 12-18-97	PRINTS TO	FIRST MADE FOR REGN.		336A3580AT SH. NO. 1
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. 2

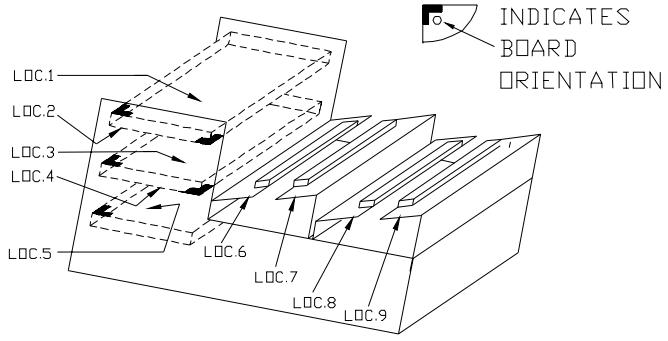
LOC. 6

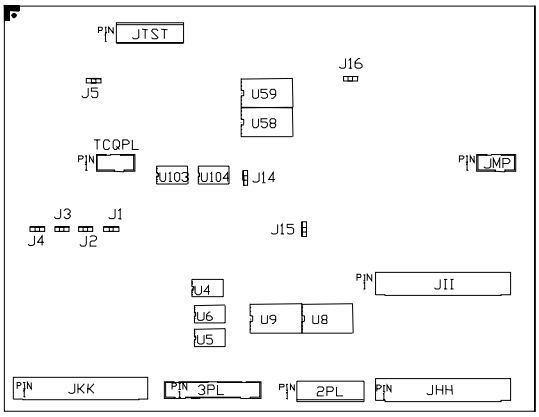




VIEW "AA"

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R> CORE MKV+
REV.4	ISSUED 12-18-97	PRINTS TO	FIRST MADE FOR REQN.		336A3580AT CONT. ON SH. FNL / SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		





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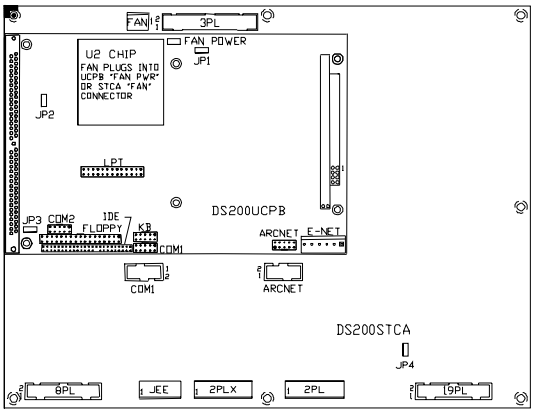
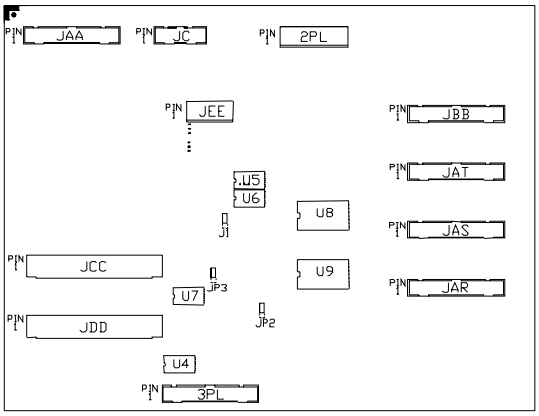


TMIAP#A LOC. 1



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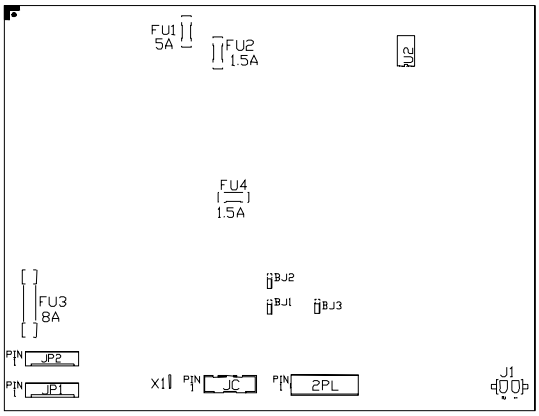
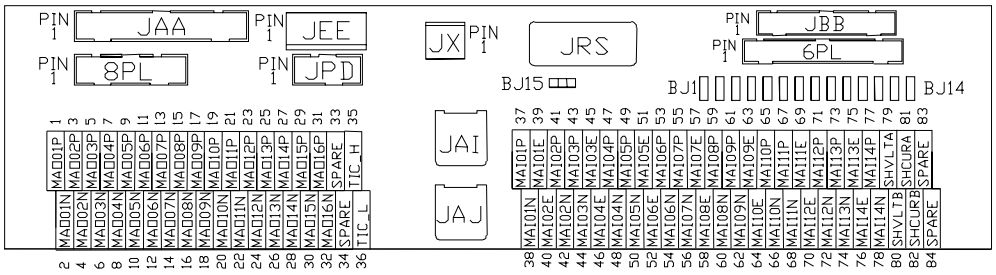


TCPSG#A LOC. 5

REV.3	REV.2	REV.1 10-24-95 JRW	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R5> CORE MKV+	
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REGN.		336A3580AC CONT. ON SH. 2	SH. NO. 1
REV.5	MADE BY J.R. WALTON		I.C. NO.			



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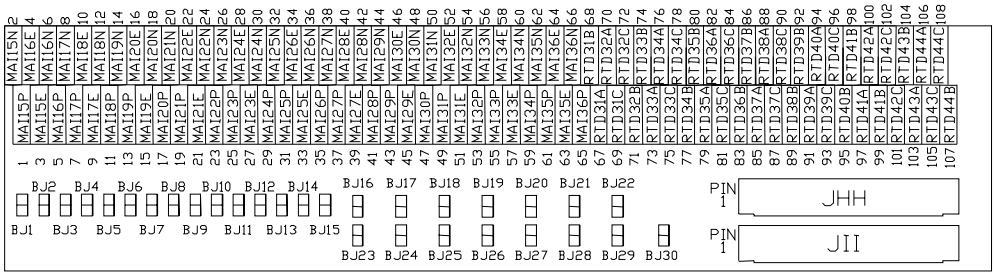
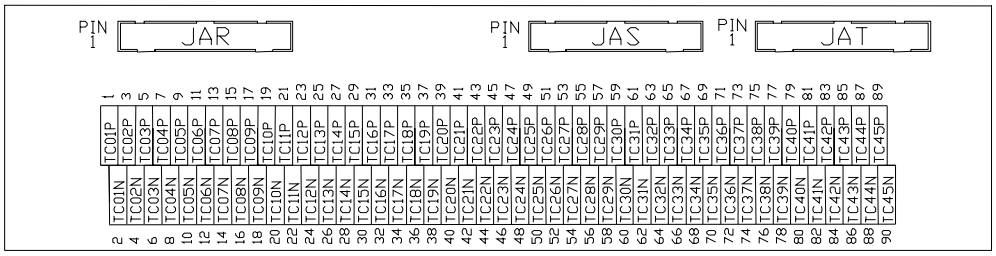
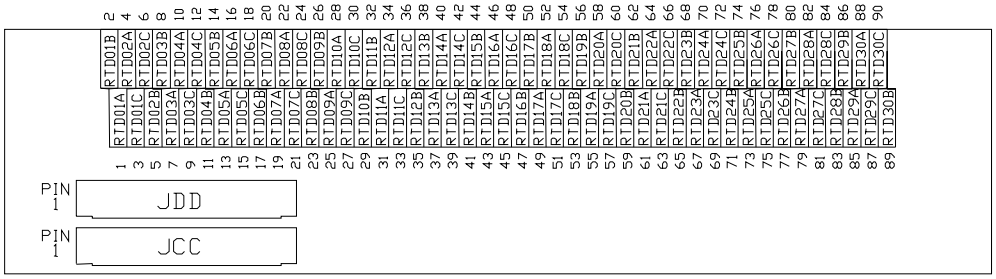


TBCBG#A LOC. 7



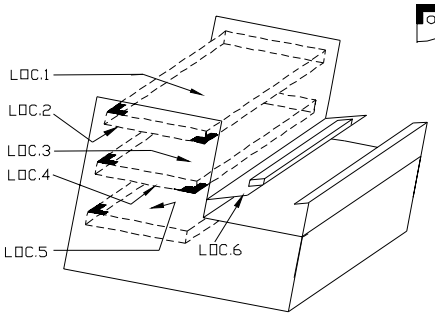
TBQAG#A LOC. 8



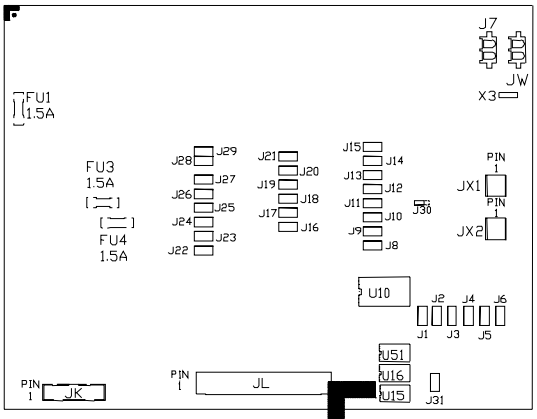
TBCAG#A LOC. 9

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <R5> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR RCQN.		336A3580AC SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. FNL

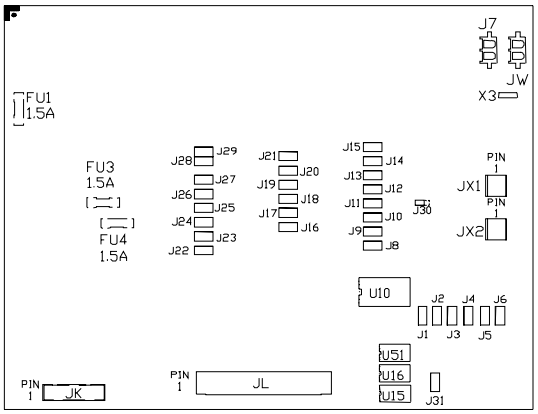
336A3580AC SH. NO. 2 CONT. ON SH. FNL



INDICATES BOARD ORIENTATION



TCEAG#B LOC.3



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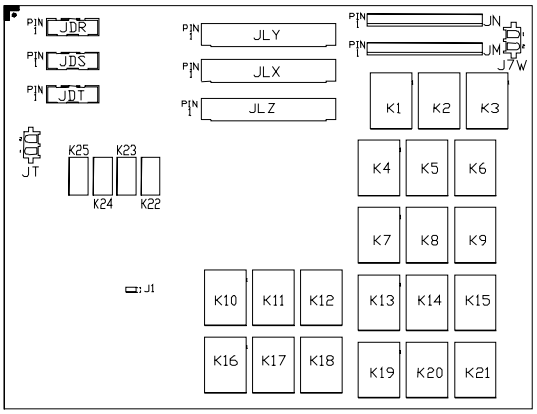

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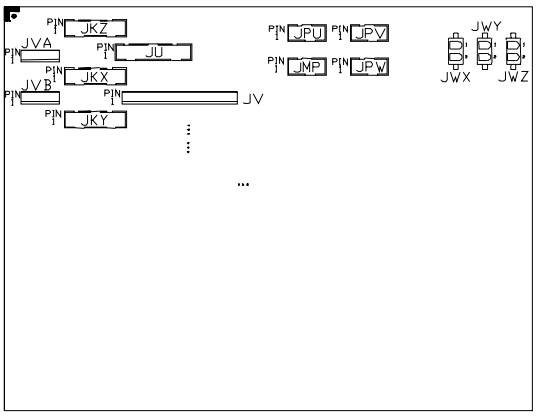

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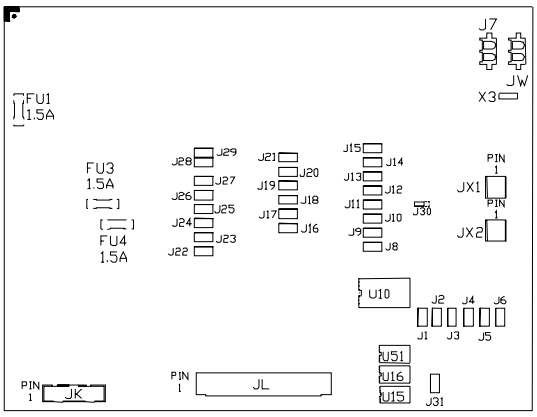
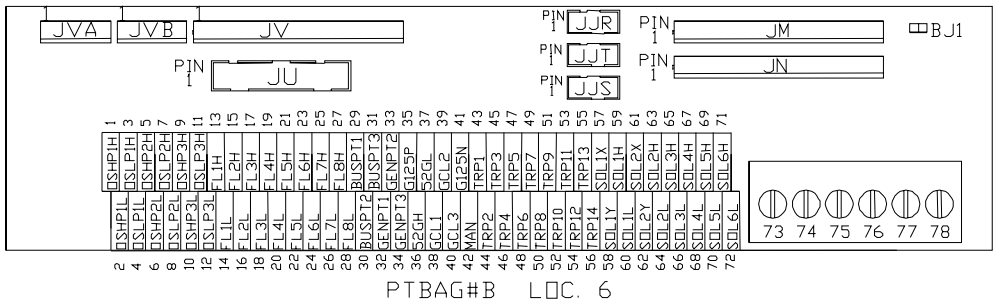


TCEAG#B LOC.5

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <P1> CORE MKV+
REV.4	ISSUED 01-14-97	PRINTS TO	FIRST MADE FOR REQN.		336A3580AS SH. NO. 1 CONT. ON SH. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		

336A3580AS SH. NO. 1 CONT. ON SH. 2

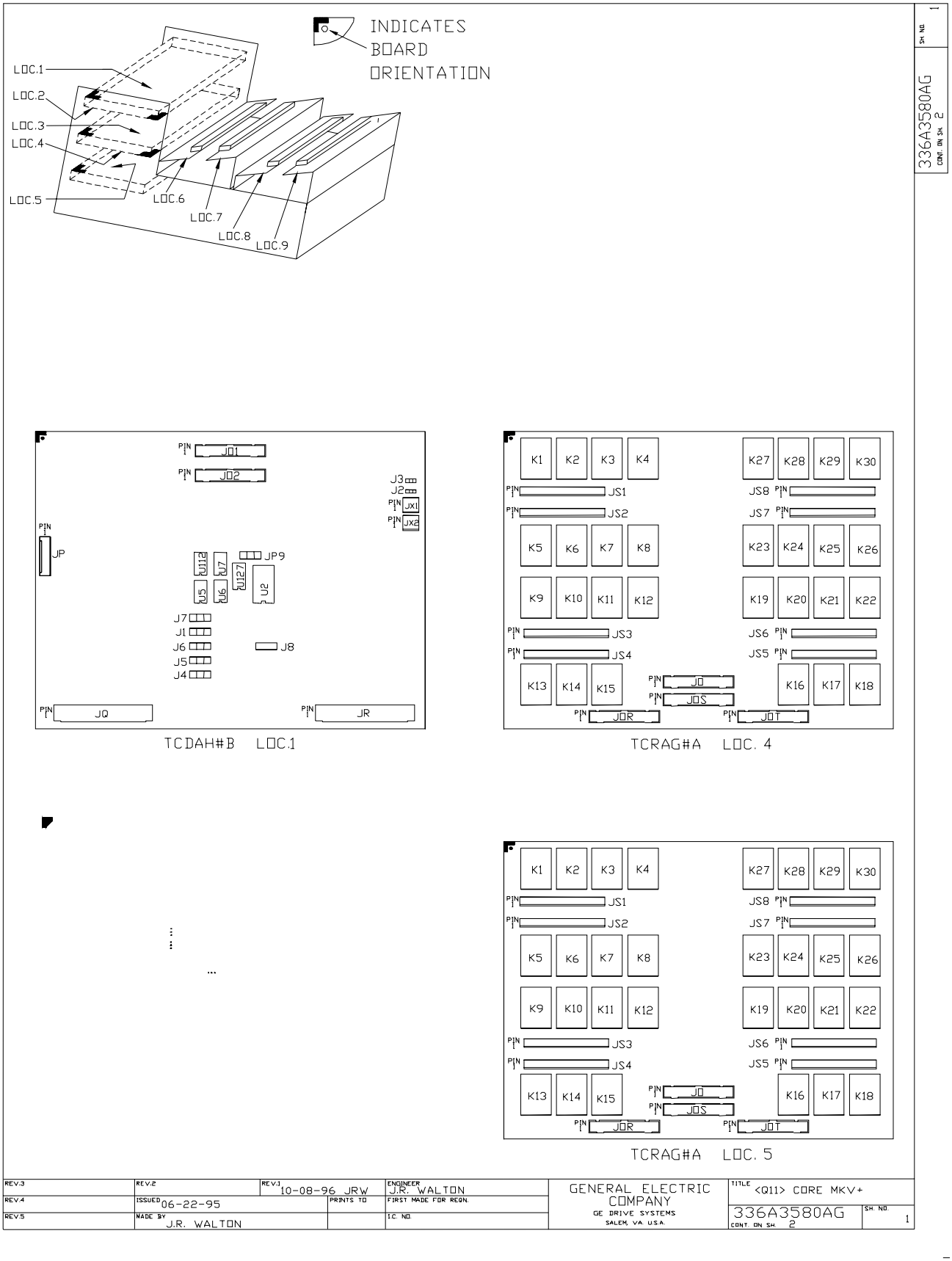


PTBAG#B LOC. 6

SH. NO 2

336A3580AS
CONT. ON SH. FNL

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <P1> CORE MKV+	
REV.4	ISSUED 01-14-97	PRINTS TO	FIRST MADE FOR REQN.		336A3580AS CONT. ON SH. FNL	SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.			


INDICATES
BOARD
ORIENTATION
LOC.1
LOC.2
LOC.3
LOC.4
LOC.5
LOC.6
LOC.7
LOC.8
LOC.9
SH. NO. 1
336A3580AG
CONT. ON SH. 2
PIN
JD1
JD2
J3
J2
JX1
JX2
JP
JP9
U112
U7
U5
U6
U127
U2
J7
J1
J6
J5
J4
J8
JQ
JR
TCDAH#B LOC.1
K1
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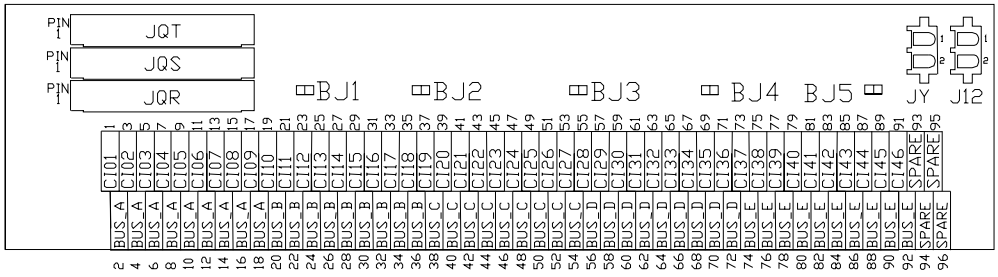
K14
K15
JD
JDS
K16
K17
K18
JDR
JDT
TCRAG#A LOC. 4
TCRAG#A LOC. 5
REV.3
REV.2
REV.1 10-08-96 JRW
ENGINEER J.R. WALTON
REV.4
ISSUED 06-22-95
PRINTS TO
FIRST MADE FOR REGN.
REV.5
MADE BY J.R. WALTON
I.C. NO.
GENERAL ELECTRIC COMPANY
GE DRIVE SYSTEMS
SALEM, VA U.S.A.
TITLE <Q11> CORE MKV+
336A3580AG
CONT. ON SH. 2
SH. NO. 1



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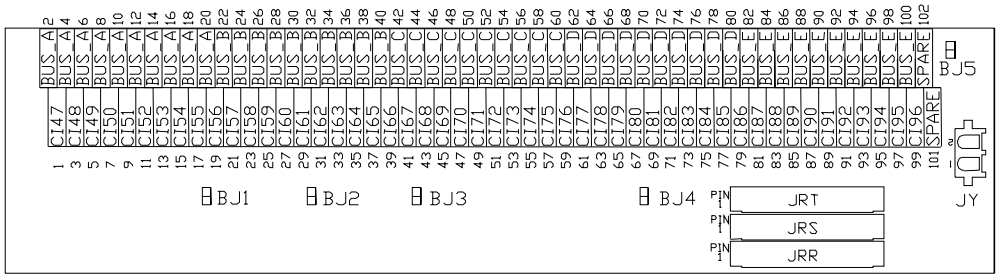

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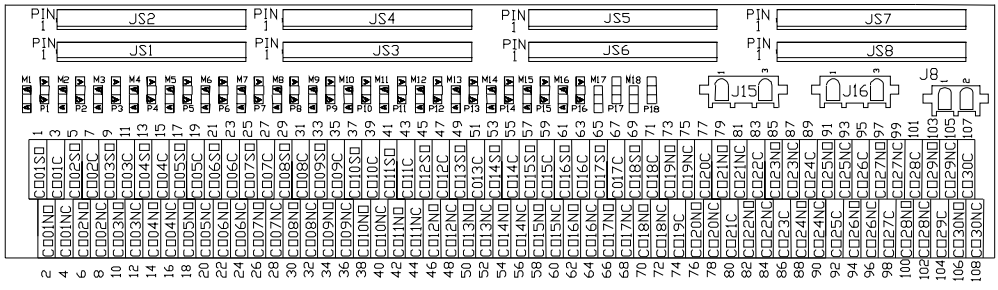

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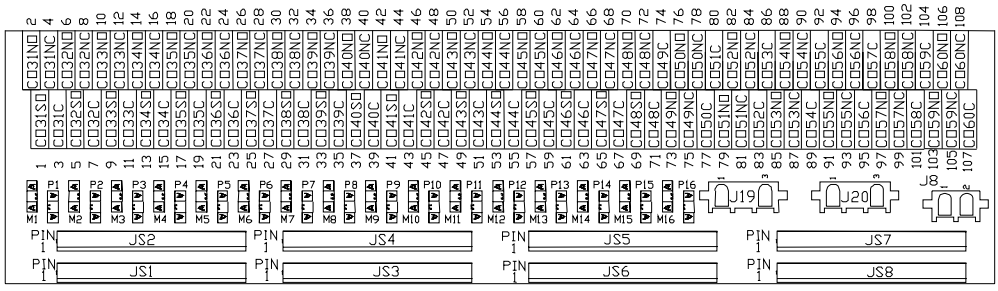
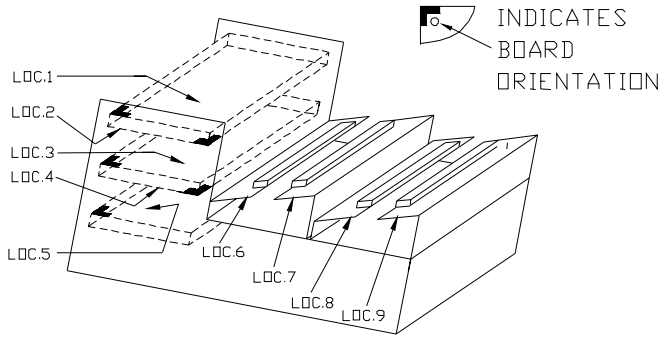


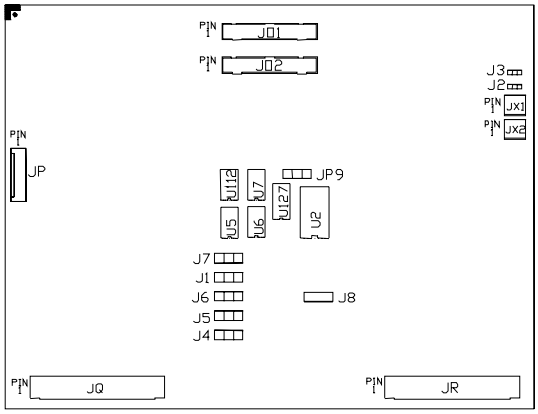
DTBDG#A LOC. 9

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <Q11> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REQN.		336A3580AG SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. FNL

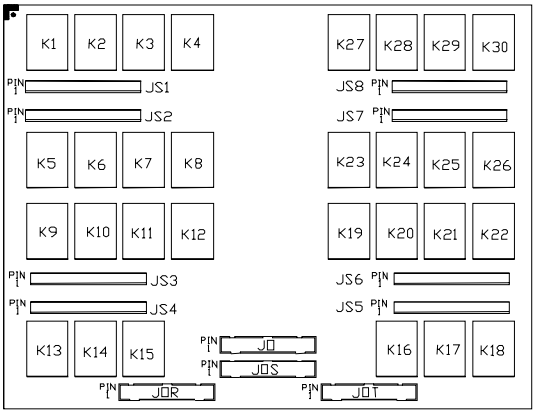


SH. NO. 1

336A3580AH
CONF. ON SH. 2



TCDAH#B LOC.1



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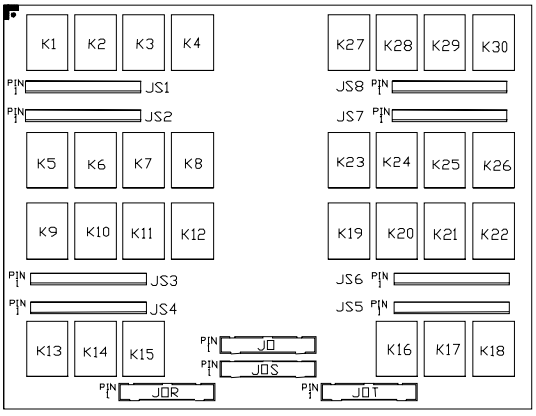
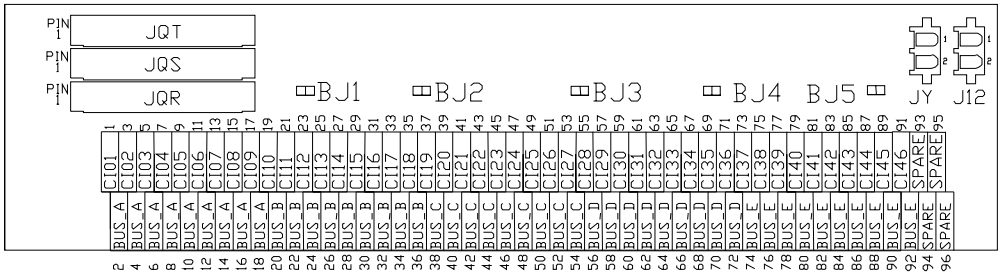


TCRAG#A LOC. 5

REV.3	REV.2	REV.1 10-08-96 JRW	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA. U.S.A.	TITLE <Q51> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REGN.		336A3580AH SH. NO. 1 CONT. ON SH. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		



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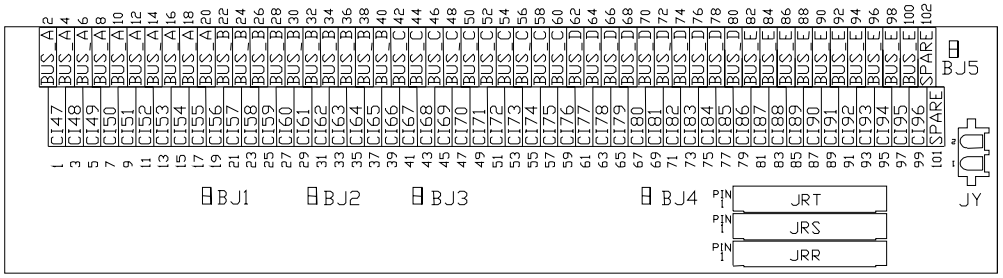

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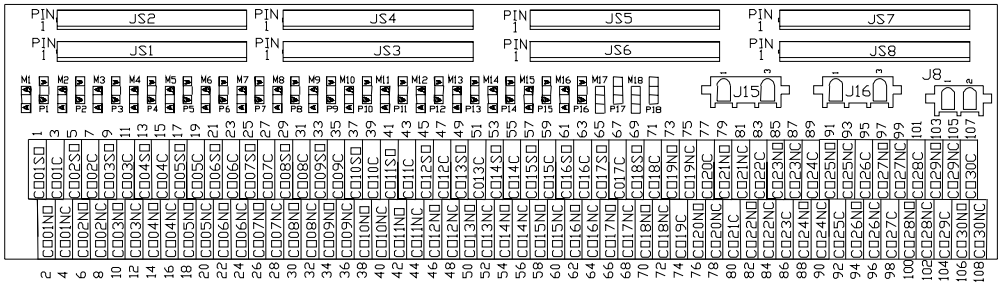

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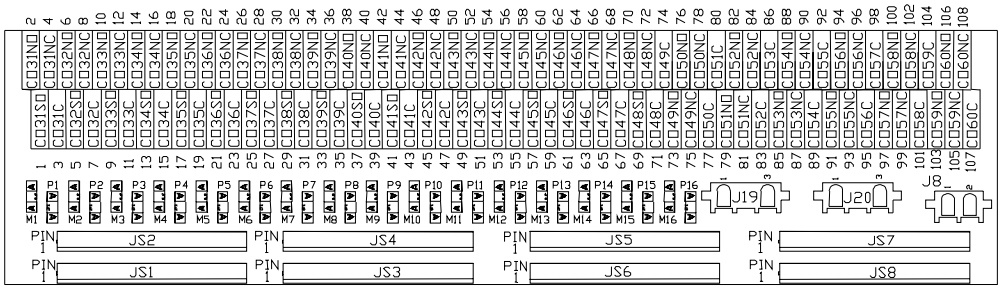

DTBDG#A LOC. 9

REV.3	REV.2	REV.1	ENGINEER J.R. WALTON	GENERAL ELECTRIC COMPANY GE DRIVE SYSTEMS SALEM, VA U.S.A.	TITLE <Q51> CORE MKV+
REV.4	ISSUED 06-22-95	PRINTS TO	FIRST MADE FOR REGN.		336A3580AH SH. NO. 2
REV.5	MADE BY J.R. WALTON		I.C. NO.		CONT. ON SH. FNL

Notes

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