TMR Processor (T8110B)

Figure 5-3: TMR Processor

Figure 5-3 shows the front panel of the TMR processor with status and diagnostic indicator LEDs, a reset button and a maintenance enable keyswitch.

The TMR processor is a fault tolerant design based on a TMR architecture arranged in a lock-step configuration. The module contains three processor **fault containment regions** (FCR), each containing a Motorola Power PC series processor and its associated memory. Each processor FCR has voted two-out-of-three (2oo3) read access to the other two processor FCRs memory systems to eliminate divergent operation.

The module's three processors store and execute the application program, scan and update the I/O modules and detect system faults. Each processor executes the application program independently, but in lock-step synchronization with the other two. Should one of the processors diverge, additional mechanisms allow the failed processor to re-synchronize with the other two.

The front panel comprises a fault containment region containing non-critical simplex functions separate from the other FCRs. These include the diagnostics port and maintenance enable keyswitch mounted on the front panel of the processor. Other functions within the front panel FCR are the serial communications drivers and the IRIG-B interface.

Each of the processor and FCRs derive their internal voltages from dual redundant +24V dc power supplied via the module connector from the controller chassis backplane.

The voter circuits read the input data from the inter-module bus and carry out a continuous 2oo3 vote of the data. The voting and fault detection circuits enable the module to identify and isolate transient, intermittent and permanent faults as they occur. All faults are recorded in the systems fault history. Permanent faults are also annunciated by an LED on the module front panel.